**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT |
| Number of I/O | 66 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 14x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-FQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl25z64vlk4 |

| Field | Description | Values |
|---|---|---|
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• FT = 48 QFN (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm)<br>• LK = 80 LQFP (12 mm x 12 mm) |
| CC | Maximum CPU frequency (MHz) | • 4 = 48 MHz |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 2.4 Example

This is an example part number:

MKL25Z64VLK4

# 3 Terminology and guidelines

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

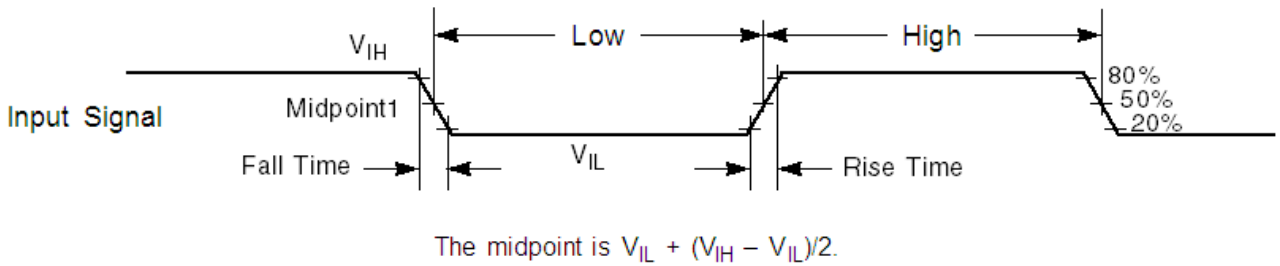



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assumes:

1. output pins
   - have $C_L$=30pF loads,
   - are slew rate disabled, and
   - are normal drive strength

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} – V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{SS} – V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{IH}$ | Input high voltage | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0.7 × $V_{DD}$ | — | V | |
| | • 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | 0.75 × $V_{DD}$ | — | V | |
| $V_{IL}$ | Input low voltage | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | — | 0.35 × $V_{DD}$ | V | |
| | • 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | — | 0.3 × $V_{DD}$ | V | |

*Table continues on the next page...*

**Table 1. Voltage and current operating requirements (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HYS}$ | Input hysteresis | 0.06 × $V_{DD}$ | — | V | |
| $I_{ICDIO}$ | Digital pin negative DC injection current — single pin<br>• $V_{IN}$ < $V_{SS}$-0.3V | -5 | — | mA | 1 |
| $I_{ICAIO}$ | Analog[2] pin DC injection current — single pin<br>• $V_{IN}$ < $V_{SS}$-0.3V (Negative current injection)<br>• $V_{IN}$ > $V_{DD}$+0.3V (Positive current injection) | <br>-5<br>— | <br>—<br>+5 | mA | 3 |
| $I_{ICcont}$ | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins<br>• Negative current injection<br>• Positive current injection | <br>-25<br>— | <br>—<br>+25 | mA | |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | |

1. All digital I/O pins are internally clamped to $V_{SS}$ through a ESD protection diode. There is no diode connection to $V_{DD}$. If $V_{IN}$ greater than $V_{DIO\_MIN}$ (=$V_{SS}$-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=($V_{DIO\_MIN}$-$V_{IN}$)/|$I_{IC}$|.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
3. All analog pins are internally clamped to $V_{SS}$ and $V_{DD}$ through ESD protection diodes. If $V_{IN}$ is greater than $V_{AIO\_MIN}$ (=$V_{SS}$-0.3V) and $V_{IN}$ is less than $V_{AIO\_MAX}$(=$V_{DD}$+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=($V_{AIO\_MIN}$-$V_{IN}$)/|$I_{IC}$|. The positive injection current limiting resistor is calcualted as R=($V_{IN}$-$V_{AIO\_MAX}$)/|$I_{IC}$|. Select the larger of these two calculated resistances.

## 5.2.2 LVD and POR operating requirements

**Table 2. $V_{DD}$ supply LVD and POR operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |

*Table continues on the next page...*

**Table 2. $V_{DD}$ supply LVD and POR operating requirements (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| $t_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising thresholds are falling threshold + hysteresis voltage

## 5.2.3 Voltage and current operating behaviors

**Table 3. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — Normal drive pad | | | | 1 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -5 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -1.5 mA | $V_{DD}$ – 0.5 | — | V | |
| $V_{OH}$ | Output high voltage — High drive pad | | | | 1 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -18 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -6 mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — Normal drive pad | | | | 1 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 5 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 1.5 mA | — | 0.5 | V | |
| $V_{OL}$ | Output low voltage — High drive pad | | | | 1 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 18 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 6 mA | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) for full temperature range | — | 1 | µA | 2 |
| $I_{IN}$ | Input leakage current (per pin) at 25 °C | — | 0.025 | µA | 2 |
| $I_{IN}$ | Input leakage current (total all pins) for full temperature range | — | 65 | µA | 2 |
| $I_{OZ}$ | Hi-Z (off-state) leakage current (per pin) | — | 1 | µA | |

*Table continues on the next page...*

## 5.2.5 Power consumption operating behaviors

### Table 5. Power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD\_RUNCO\_CM}$ | Run mode current in compute operation - 48 MHz core / 24 MHz flash/ bus disabled, LPTMR running using 4MHz internal reference clock, CoreMark® benchmark code executing from flash<br>• at 3.0 V | — | 6.4 | — | mA | 2 |
| $I_{DD\_RUNCO}$ | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 4.1 | 5.2 | mA | 3 |
| $I_{DD\_RUN}$ | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 5.1 | 6.3 | mA | 3 |
| $I_{DD\_RUN}$ | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash<br>• at 3.0 V<br>• at 25 °C<br>• at 125 °C | <br><br>—<br>— | <br><br>6.4<br>6.8 | <br><br>7.8<br>8.3 | <br><br>mA<br>mA | 3, 4, |
| $I_{DD\_WAIT}$ | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 3.7 | 5.0 | mA | 3 |
| $I_{DD\_WAIT}$ | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 2.9 | 4.2 | mA | 3 |
| $I_{DD\_PSTOP2}$ | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus<br>• at 3.0 V | — | 2.5 | 3.7 | mA | 3 |
| $I_{DD\_VLPRCO}$ | Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 188 | 570 | µA | 5 |
| $I_{DD\_VLPR}$ | Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 224 | 613 | µA | 5 |

*Table continues on the next page...*

## Table 5. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLPR}$ | Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash<br>• at 3.0 V | — | 300 | 745 | µA | 5, 4 |
| $I_{DD\_VLPW}$ | Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled<br>• at 3.0 V | — | 135 | 496 | µA | 5 |
| $I_{DD\_STOP}$ | Stop mode current at 3.0 V | | | | | |
| | at 25 °C | — | 345 | 490 | | |
| | at 50 °C | — | 357 | 827 | µA | |
| | at 70 °C | — | 392 | 869 | | |
| | at 85 °C | — | 438 | 927 | | |
| | at 105 °C | — | 551 | 1065 | | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current at 3.0 V | | | | | |
| | at 25 °C | — | 4.4 | 16 | | |
| | at 50 °C | — | 10 | 35 | µA | |
| | at 70 °C | — | 20 | 50 | | |
| | at 85 °C | — | 37 | 112 | | |
| | at 105 °C | — | 81 | 201 | | |
| $I_{DD\_LLS}$ | Low leakage stop mode current at 3.0 V | | | | | |
| | at 25 °C | — | 1.9 | 3.7 | µA | |
| | at 50 °C | — | 3.6 | 39 | | |
| | at 70 °C | — | 6.5 | 43 | | |
| | at 85 °C | — | 13 | 49 | | |
| | at 105 °C | — | 30 | 69 | | |
| $I_{DD\_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | | | | | |
| | at 25 °C | — | 1.4 | 3.2 | µA | |
| | at 50 °C | — | 2.5 | 19 | | |
| | at 70 °C | — | 5.1 | 21 | | |
| | at 85 °C | — | 9.2 | 26 | | |
| | at 105 °C | — | 21 | 38 | | |
| $I_{DD\_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0V | | | | | |
| | at 25°C | — | 0.7 | 1.4 | | |
| | at 50°C | — | 1.3 | 13 | µA | |
| | at 70°C | — | 2.3 | 14 | | |
| | at 85°C | — | 5.1 | 17 | | |
| | at 105°C | — | 13 | 25 | | |

*Table continues on the next page...*

## Table 5. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V | — | 381 | 943 | nA | |
| | at 25 °C | — | 956 | 11760 | | |
| | at 50 °C | — | 2370 | 13260 | | |
| | at 70 °C | — | 4800 | 15700 | | |
| | at 85 °C | — | 12410 | 23480 | | |
| | at 105 °C | | | | | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V | — | 176 | 860 | nA | 6 |
| | at 25 °C | — | 760 | 3577 | | |
| | at 50 °C | — | 2120 | 11660 | | |
| | at 70 °C | — | 4500 | 18450 | | |
| | at 85 °C | — | 12130 | 22441 | | |
| | at 105 °C | | | | | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using Keil 4.54 with optimization level 3, optimized for time.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.
6. No brownout

## Table 6. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| $I_{IREFSTEN4MHz}$ | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | µA |
| $I_{IREFSTEN32KHz}$ | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | µA |
| $I_{EREFSTEN4MHz}$ | External 4MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | uA |

*Table continues on the next page...*

**Table 6. Low power mode peripheral adders — typical value (continued)**

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| $I_{ADC}$ | ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 366 | 366 | 366 | 366 | 366 | 366 | µA |

### 5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

2. $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, $f_{OSC}$ = 8 MHz (crystal), $f_{SYS}$ = 48 MHz, $f_{BUS}$ = 48 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

### 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

### 5.2.8 Capacitance attributes

**Table 8. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN\_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN\_D}$ | Input capacitance: digital pins | — | 7 | pF |

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Normal run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 48 | MHz | |
| $f_{BUS}$ | Bus clock | — | 24 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 24 | MHz | |
| $f_{SYS\_USB}$ | System and core clock when Full Speed USB in operation | 20 | — | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 24 | MHz | |
| VLPR mode[1] | | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz | |
| $f_{BUS}$ | Bus clock | — | 1 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 24 | MHz | |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz | |
| $f_{LPTMR\_pin}$ | LPTMR clock | — | 24 | MHz | |

*Table continues on the next page...*

**Table 11. SWD full voltage range electricals (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| J1 | SWD_CLK frequency of operation<br>• Serial wire debug | <br>0 | <br>25 | <br>MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width<br>• Serial wire debug | <br>20 | <br>— | <br>ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

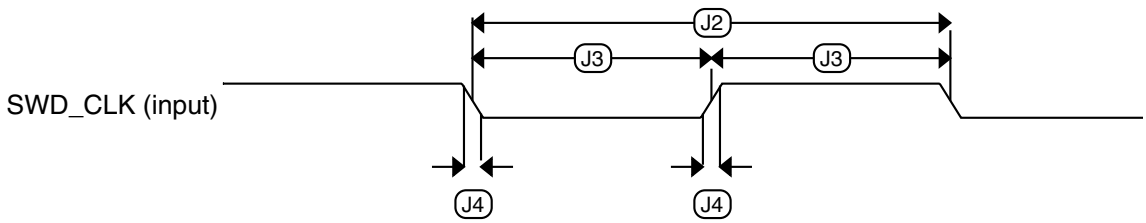



**Figure 4. Serial wire clock input timing**

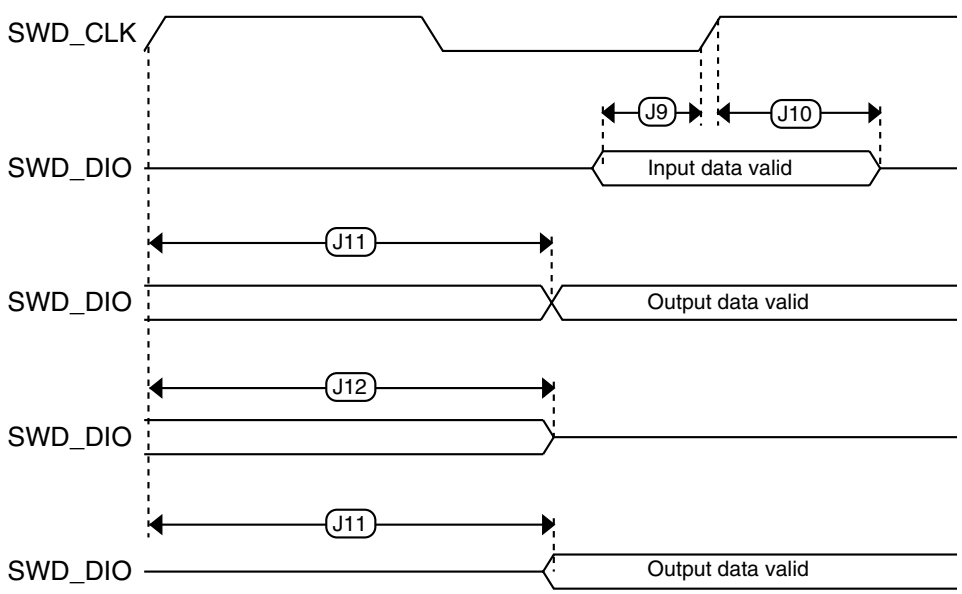



**Figure 5. Serial wire data timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG specifications

**Table 12. MCG specifications**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal $V_{DD}$ and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | | — | +0.5/-0.7 | ± 3 | $\%f_{dco}$ | 1, 2 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C | | — | ± 0.4 | ± 1.5 | $\%f_{dco}$ | 1, 2 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal $V_{DD}$ and 25 °C | | — | 4 | — | MHz | |
| $\Delta f_{intf\_ft}$ | Frequency deviation of internal reference clock (fast clock) over temperature and voltage --- factory trimmed at nominal $V_{DD}$ and 25 °C | | — | +1/-2 | ± 3 | $\%f_{intf\_ft}$ | 2 |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal $V_{DD}$ and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints\_t}$ | — | — | kHz | |
| $f_{loc\_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS = 00) 640 × $f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS = 01) 1280 × $f_{fll\_ref}$ | 40 | 41.94 | 48 | MHz | |

*Table continues on the next page...*

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC electrical specifications

**Table 13. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |

*Table continues on the next page...*

**Table 13. Oscillator DC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$,$C_y$ can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used..
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

**Table 14. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 48 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |

*Table continues on the next page...*

## Table 20. 16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$) (continued)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $E_{IL}$ | Input leakage error | | $I_{In} \times R_{AS}$ | | | mV | $I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | — | 1.715 | — | mV/°C | |
| $V_{TEMP25}$ | Temp sensor voltage | 25 °C | — | 719 | — | mV | |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$ = $V_{DDA}$
2. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/$2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

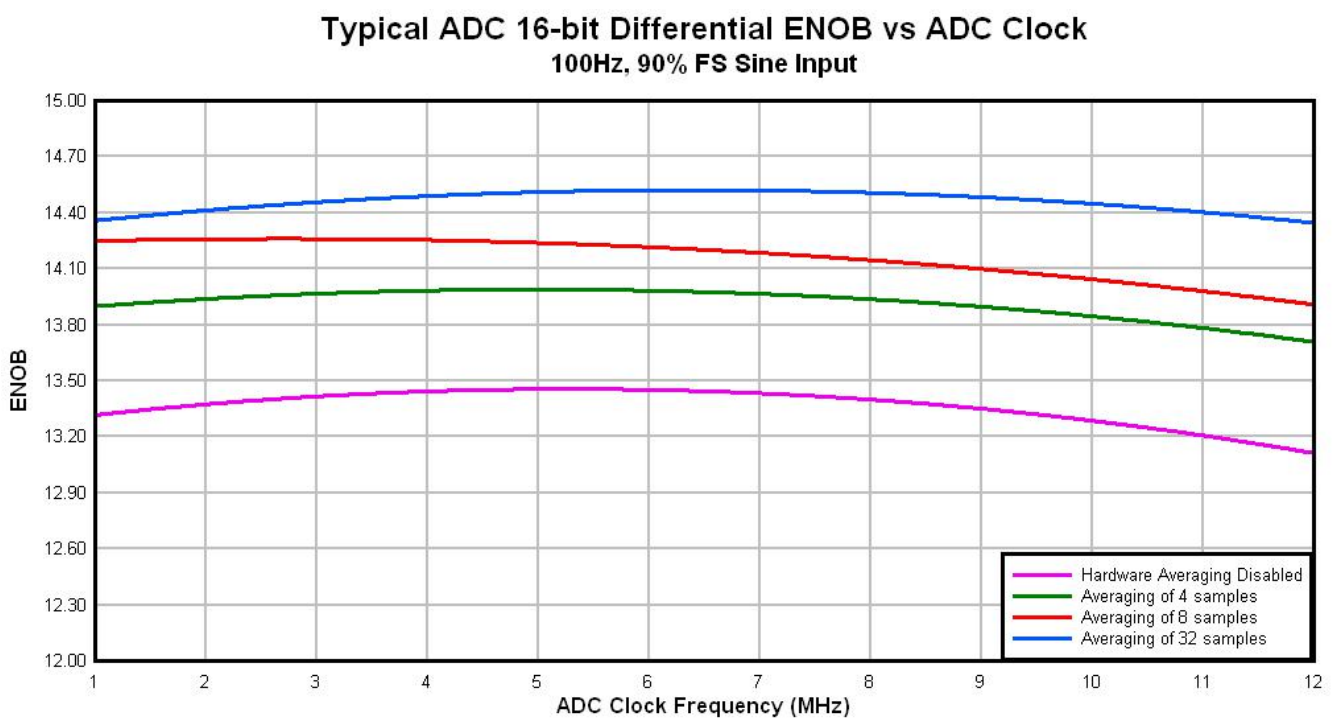



**Figure 7. Typical ENOB vs. ADC_CLK for 16-bit differential mode**

## Table 23. 12-bit DAC operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| SR | Slew rate -80h→ F7Fh→ 80h | | | | V/µs | |
| | • High power ($SP_{HP}$) | 1.2 | 1.7 | — | | |
| | • Low power ($SP_{LP}$) | 0.05 | 0.12 | — | | |
| BW | 3dB bandwidth | | | | kHz | |
| | • High power ($SP_{HP}$) | 550 | — | — | | |
| | • Low power ($SP_{LP}$) | 40 | — | — | | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ − 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

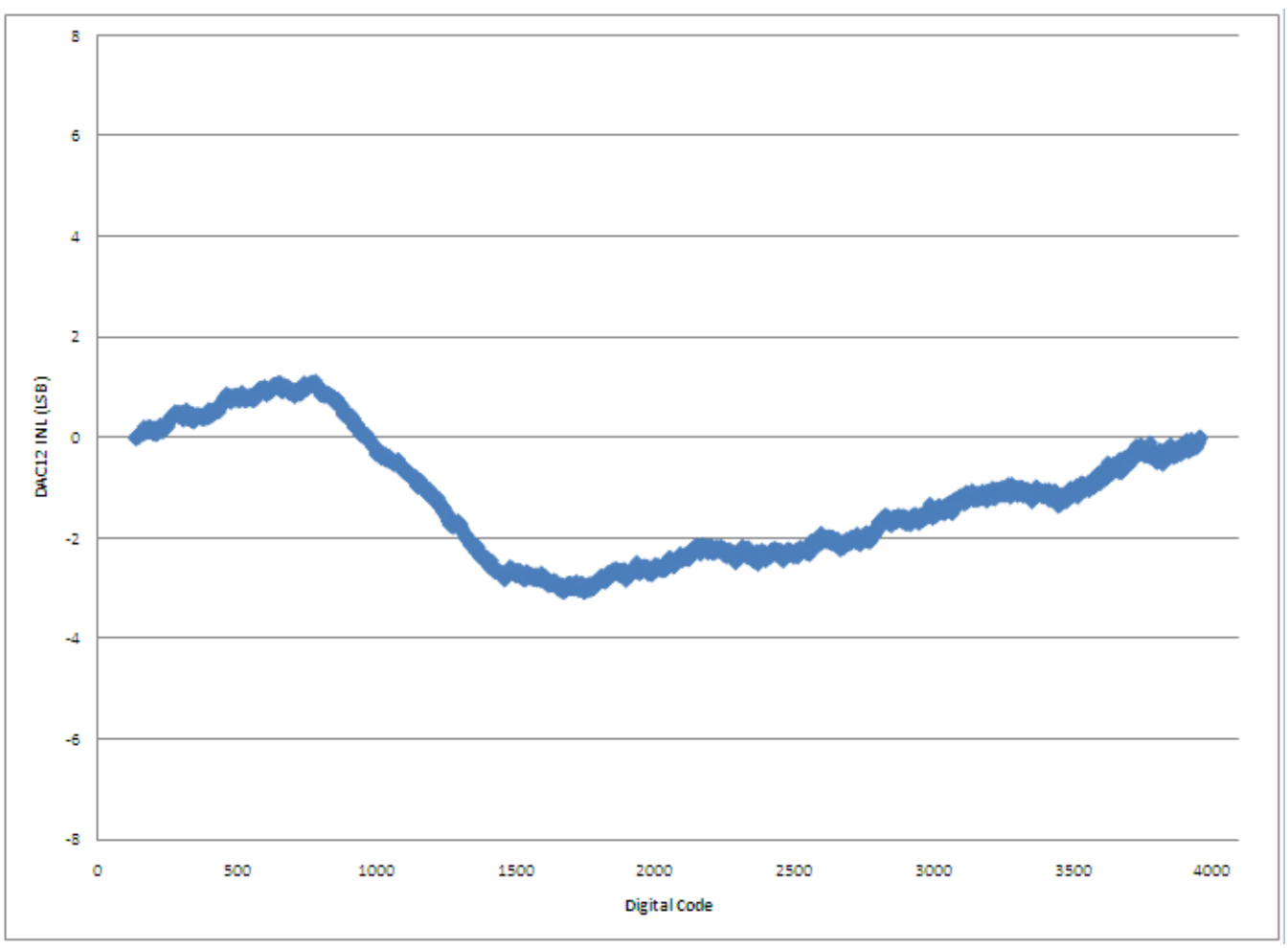
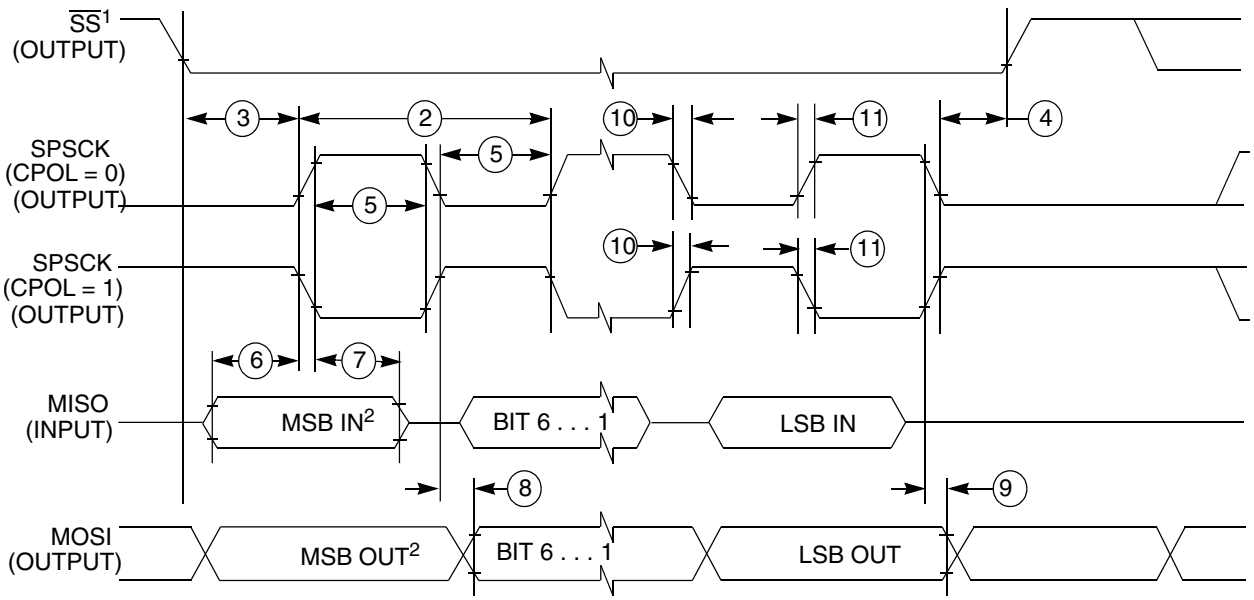
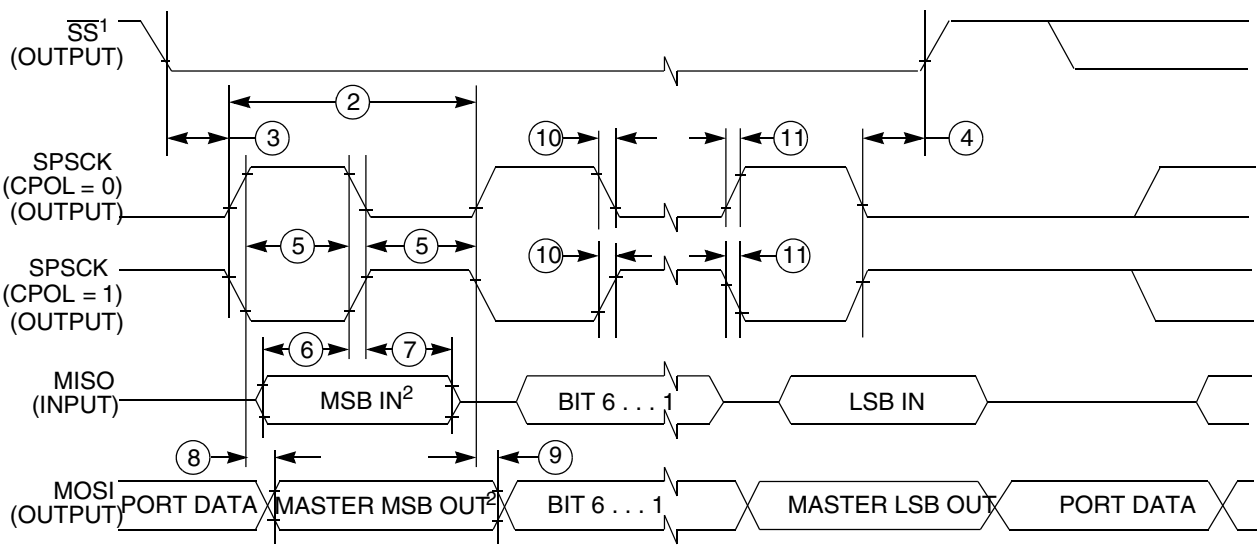



**Figure 11. Typical INL error vs. digital code**




1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 13. SPI master mode timing (CPHA = 0)**




1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA = 1)**

## Table 27. SPI slave mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | — | ns | — |

*Table continues on the next page...*

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

**Table 29. TSI electrical specifications**

| Symbol | Description | Min. | Type | Max | Unit |
|---|---|---|---|---|---|
| TSI_RUNF | Fixed power consumption in run mode | — | 100 | — | µA |
| TSI_RUNV | Variable power consumption in run mode (depends on oscillator's current selection) | 1.0 | — | 128 | µA |
| TSI_EN | Power consumption in enable mode | — | 100 | — | µA |
| TSI_DIS | Power consumption in disable mode | — | 1.2 | — | µA |
| TSI_TEN | TSI analog enable time | — | 66 | — | µs |
| TSI_CREF | TSI reference capacitor | — | 1.0 | — | pF |
| TSI_DVOLT | Voltage variation of VP & VM around nominal values | 0.19 | — | 1.03 | V |

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 32-pin QFN | 98ASA00473D |
| 48-pin QFN | 98ASA00466D |
| 64-pin LQFP | 98ASS23234W |
| 80-pin LQFP | 98ASS23174W |

# 8 Pinout

## 8.1 KL25 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 80 LQFP | 64 LQFP | 48 QFN | 32 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | — | 1 | PTE0 | DISABLED | | PTE0 | | UART1_TX | RTC_CLKOUT | CMP0_OUT | I2C1_SDA | |
| 2 | 2 | — | — | PTE1 | DISABLED | | PTE1 | SPI1_MOSI | UART1_RX | | SPI1_MISO | I2C1_SCL | |
| 3 | — | — | — | PTE2 | DISABLED | | PTE2 | SPI1_SCK | | | | | |
| 4 | — | — | — | PTE3 | DISABLED | | PTE3 | SPI1_MISO | | | SPI1_MOSI | | |
| 5 | — | — | — | PTE4 | DISABLED | | PTE4 | SPI1_PCS0 | | | | | |
| 6 | — | — | — | PTE5 | DISABLED | | PTE5 | | | | | | |
| 7 | 3 | 1 | — | VDD | VDD | VDD | | | | | | | |
| 8 | 4 | 2 | 2 | VSS | VSS | VSS | | | | | | | |
| 9 | 5 | 3 | 3 | USB0_DP | USB0_DP | USB0_DP | | | | | | | |
| 10 | 6 | 4 | 4 | USB0_DM | USB0_DM | USB0_DM | | | | | | | |
| 11 | 7 | 5 | 5 | VOUT33 | VOUT33 | VOUT33 | | | | | | | |
| 12 | 8 | 6 | 6 | VREGIN | VREGIN | VREGIN | | | | | | | |
| 13 | 9 | 7 | — | PTE20 | ADC0_DP0/ ADC0_SE0 | ADC0_DP0/ ADC0_SE0 | PTE20 | | TPM1_CH0 | UART0_TX | | | |
| 14 | 10 | 8 | — | PTE21 | ADC0_DM0/ ADC0_SE4a | ADC0_DM0/ ADC0_SE4a | PTE21 | | TPM1_CH1 | UART0_RX | | | |
| 15 | 11 | — | — | PTE22 | ADC0_DP3/ ADC0_SE3 | ADC0_DP3/ ADC0_SE3 | PTE22 | | TPM2_CH0 | UART2_TX | | | |
| 16 | 12 | — | — | PTE23 | ADC0_DM3/ ADC0_SE7a | ADC0_DM3/ ADC0_SE7a | PTE23 | | TPM2_CH1 | UART2_RX | | | |
| 17 | 13 | 9 | 7 | VDDA | VDDA | VDDA | | | | | | | |
| 18 | 14 | 10 | — | VREFH | VREFH | VREFH | | | | | | | |
| 19 | 15 | 11 | — | VREFL | VREFL | VREFL | | | | | | | |
| 20 | 16 | 12 | 8 | VSSA | VSSA | VSSA | | | | | | | |
| 21 | 17 | 13 | — | PTE29 | CMP0_IN5/ ADC0_SE4b | CMP0_IN5/ ADC0_SE4b | PTE29 | | TPM0_CH2 | TPM_CLKIN0 | | | |
| 22 | 18 | 14 | 9 | PTE30 | DAC0_OUT/ ADC0_SE23/ CMP0_IN4 | DAC0_OUT/ ADC0_SE23/ CMP0_IN4 | PTE30 | | TPM0_CH3 | TPM_CLKIN1 | | | |
| 23 | 19 | — | — | PTE31 | DISABLED | | PTE31 | | TPM0_CH4 | | | | |
| 24 | 20 | 15 | — | PTE24 | DISABLED | | PTE24 | | TPM0_CH0 | | I2C0_SCL | | |
| 25 | 21 | 16 | — | PTE25 | DISABLED | | PTE25 | | TPM0_CH1 | | I2C0_SDA | | |
| 26 | 22 | 17 | 10 | PTA0 | SWD_CLK | TSI0_CH1 | PTA0 | | TPM0_CH5 | | | | SWD_CLK |
| 27 | 23 | 18 | 11 | PTA1 | DISABLED | TSI0_CH2 | PTA1 | UART0_RX | TPM2_CH0 | | | | |
| 28 | 24 | 19 | 12 | PTA2 | DISABLED | TSI0_CH3 | PTA2 | UART0_TX | TPM2_CH1 | | | | |
| 29 | 25 | 20 | 13 | PTA3 | SWD_DIO | TSI0_CH4 | PTA3 | I2C1_SCL | TPM0_CH0 | | | | SWD_DIO |
| 30 | 26 | 21 | 14 | PTA4 | NMI_b | TSI0_CH5 | PTA4 | I2C1_SDA | TPM0_CH1 | | | | NMI_b |
| 31 | 27 | — | — | PTA5 | DISABLED | | PTA5 | USB_CLKIN | TPM0_CH2 | | | | |

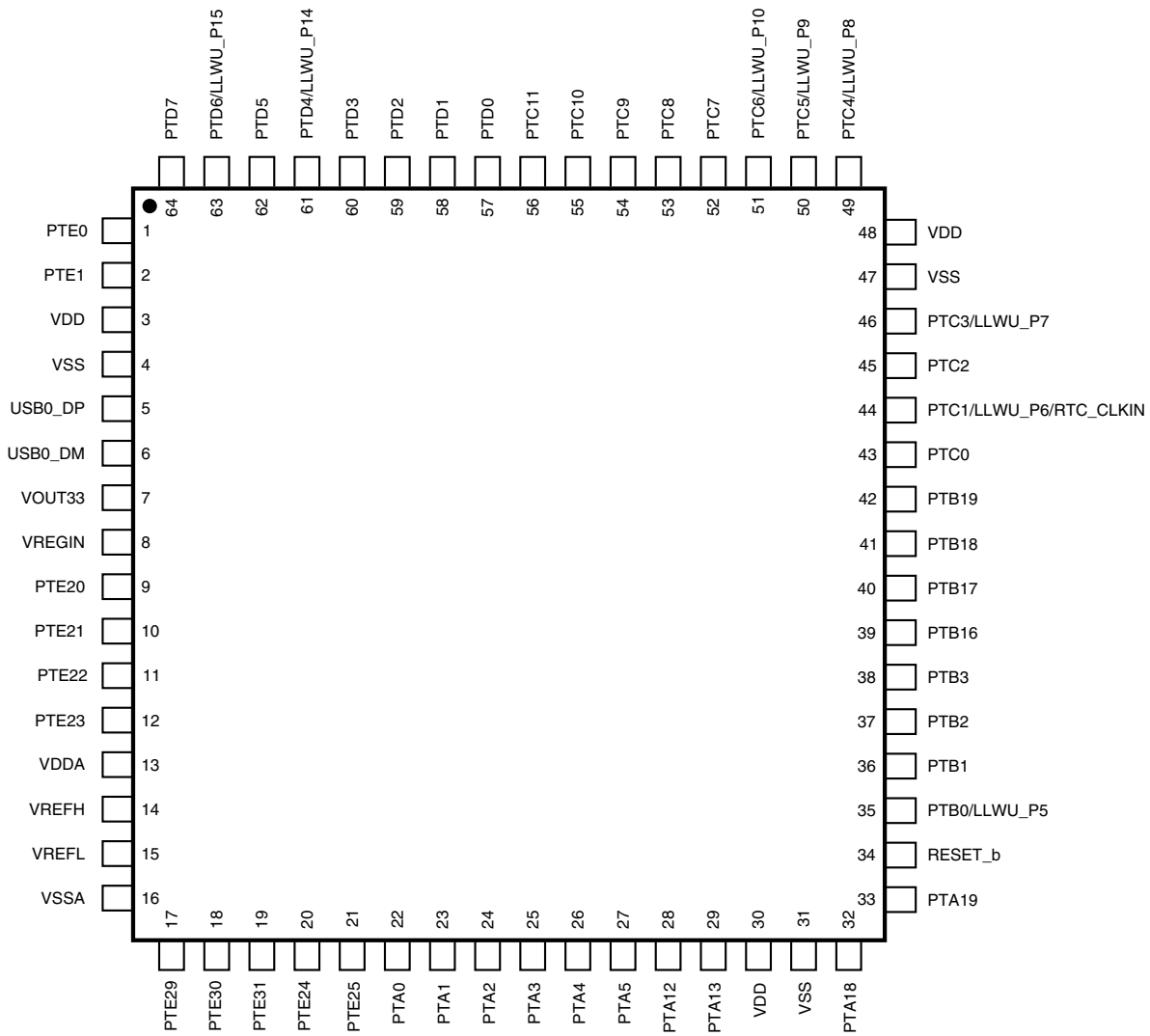



**Figure 18. KL25 64-pin LQFP pinout diagram**