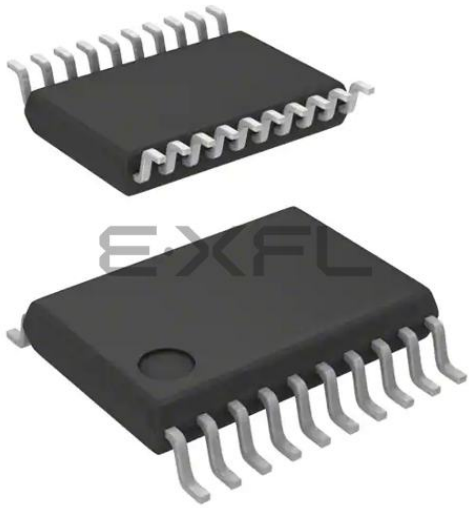

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10267asp-x5

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Figure 2. Minimum Run time definition 19

Table 4. Summary of silicon limitation (continued)

Section	Limitation	Rev 4
Section 2.9: OTG_FS peripheral limitations	Section 2.9.1: Suspend mode robustness marginality after receiving corrupted packet from Host	A
	Section 2.9.2: Bits OTG_FS_GLPMCFG[6:2] are not write-protected in Device mode	P
	Section 2.9.3: L1 exit with simultaneous Device initiated and Host initiated Resume results in minimum Device wake-up time of 3 ms	P
	Section 2.9.4: Data FIFO gets corrupted if the write sequence to the Transmit FIFO is interleaved with other OTGFS register access	A
Section 2.10: SPI limitations	Section 2.10.1: BSY bit may stay high at the end of a data transfer at slave mode	A
Section 2.11: SWPMI peripheral limitations	Section 2.11.1: SUSPENDED mode entry delayed	N
	Section 2.11.2: SUSPENDED mode never entered	P
	Section 2.11.3: SRF flag not set	N
	Section 2.11.4: SWP SUSPENDED mode not supported when STM32L4 is in Stop 0 or Stop 1 mode	N
	Section 2.11.5: SWPMI_IO transceiver bypass mode is not functional	N
Section 2.12: RTC peripheral limitations	Section 2.12.1: Spurious tamper detection when disabling the tamper channel	P
Section 2.13: USART limitations	Section 2.13.1: Start bit detected too soon when sampling for NACK signal from the smartcard	N
	Section 2.13.2: Break request can prevent the Transmission Complete flag (TC) from being set	A
	Section 2.13.3: nRTS is active while RE or UE = 0	A
Section 2.14: COMP peripheral limitations	Section 2.14.1: Comparators propagation delay is longer than expected for input steps higher than 200 mV	N
	Section 2.14.2: Comparators output cannot be configured in open-drain	N
	Section 2.14.3: COMP1 and COMP2 configuration lost with software reset	N
Section 2.15: LPTIM peripheral limitations	Section 2.15.1: Low power timer 1 (LPTIM1) outputs cannot be configured in open-drain	N
Section 2.16: LPUART peripheral limitations	Section 2.16.1: Low power UART1 (LPUART1) outputs cannot be configured in open-drain	N
Section 2.17: TSC peripheral limitations	Section 2.17.1: Inhibited acquisition in short transfer phase configuration	A

1. Fixed on products with date code newer than 609.