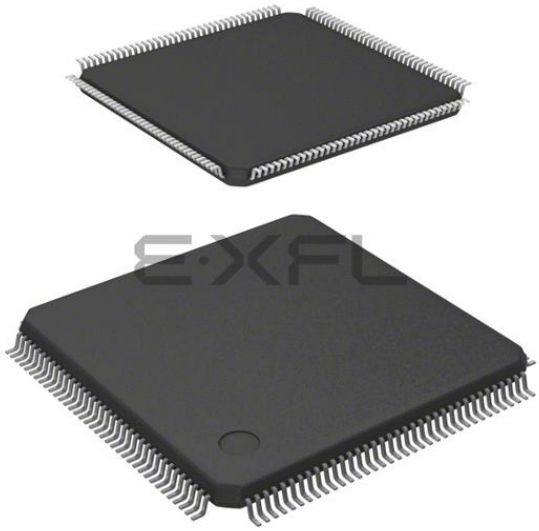

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R5F
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	150
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6j311ejaase1000a

1. Product Lineup

The following table lists the models available in the S6J3110 series.

Table 1-1 Memory Size

	S6J311EyzC*	S6J311DyzC*	S6J311CyzC*	S6J311ByzC*
Flash (Program)	4096K bytes + small sector (8KB x 8)	3072K bytes + small sector (8KB x 8)	2048K bytes + small sector (8KB x 8)	1536K bytes + small sector (8KB x 8)
Flash (Work)	112K bytes			
RAM (TCRAM)	64K bytes			
RAM (System SRAM)	256K bytes	192K bytes	128K bytes	64K bytes
RAM (Backup RAM)	64K bytes			

* y: J/H, z: A/B

Table 1-2 SHE Option

	S6J311xyAC*	S6J311xyBC*
Security (SHE)	ON	OFF

* x: E/D/C/B, y: J/H

3. Pin Description

This section provides a list of the pin functions of the S6J3110 series

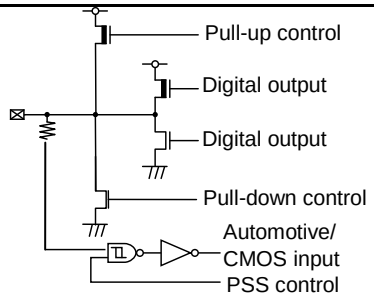
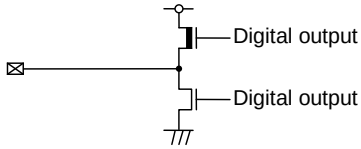
Table 3-1 S6J311xJzC* Pin Functions

* x: E/D/C/B, z: A/B

Pin No. S6J311xJzC	Pin Name	Polarity	I/O Circuit Type	Function
2	P000 SOT2_1	- -	P	General-purpose I/O port Multi-function serial ch.2 serial data output pin (1)
3	P001 SCS20_1	- -	P	General-purpose I/O port Multi-function serial ch.2 chip select 0 I/O pin (1)
4	P002 SCS21_1 TIOA0_1	- - -	P	General-purpose I/O port Multi-function serial ch.2 chip select 1 output pin (1) Base timer ch.0 TIOA output pin (1)
5	P003 SCS22_1	- -	P	General-purpose I/O port Multi-function serial ch.2 chip select 2 output pin (1)
6	P004 SCS23_1 TIOA1_1	- - -	P	General-purpose I/O port Multi-function serial ch.3 chip select 2 output pin (1) Base timer ch.1 TIOA output pin (1)
7	P005 IN6_0 SIN3_0	- - -	P	General-purpose I/O port Input capture ch.6 input pin (0) Multi-function serial ch.3 serial data input pin (0)
8	P006 IN7_0 SOT3_0 SDA3_0	- - - -	P	General-purpose I/O port Input capture ch.7 input pin (0) Multi-function serial ch.3 serial data output pin (0) I^2C bus ch.3 serial data I/O pin
9	P007 IN8_0 SCK18_1 SCK3_0 SCL3_0	- - - - -	P	General-purpose I/O port Input capture ch.8 input pin (0) Multi-function serial ch.18 clock I/O pin (1) Multi-function serial ch.3 clock I/O pin (0) I^2C bus ch.3 serial clock I/O pin
10	P008 IN9_0 SCS180_1 SCS30_0 TIOA0_0	- - - - -	P	General-purpose I/O port Input capture ch.9 input pin (0) Multi-function serial ch.18 chip select 0 I/O pin (1) Multi-function serial ch.3 chip select 0 I/O pin (0) Base timer ch.0 TIOA output pin (0)
11	P009 IN10_0 SIN8_0 TIOA1_0 INT0_1	- - - - -	P	General-purpose I/O port Input capture ch.10 input pin (0) Multi-function serial ch.8 serial data input pin (0) Base timer ch.1 TIOA I/O pin (0) INT0 external interrupt input pin (1)
12	P010 IN11_0 SOT8_0 SDA8_0 TIOA2_0	- - - - -	P	General-purpose I/O port Input capture ch.11 input pin (0) Multi-function serial ch.8 serial data output pin (0) I^2C bus ch.8 serial data I/O pin Base timer ch.2 TIOA output pin (0)
13	P011 SIN18_1 TIOA2_1	- - -	P	General-purpose I/O port Multi-function serial ch.18 serial data input pin (1) Base timer ch.2 TIOA output pin (1)
14	P012 SCK8_0 SCL8_0 TIOA3_0 OUT5_0	- - - - -	P	General-purpose I/O port Multi-function serial ch.8 clock I/O pin (0) I^2C bus ch.8 serial clock I/O pin Base timer ch.3 TIOA I/O pin (0) Output compare ch.5 output pin (0)

Pin No. S6J311xJzC	Pin Name	Polarity	I/O Circuit Type	Function
173	P419 SCS23_0 SOT12_0 SDA12_0 TIOA27_1	- - - - -	Q	General-purpose I/O port Multi-function serial ch.2 chip select 3 output pin (0) Multi-function serial ch.12 serial data output pin (0) I^2C bus ch.12 serial data I/O pin Base timer ch.27 TIOA output pin (1)
174	P420 SCK2_1 SCK12_0 SCL12_0 TRACECLK	- - - - -	Q	General-purpose I/O port Multi-function serial ch.2 clock I/O pin (1) Multi-function serial ch.12 clock I/O pin (0) I^2C bus ch.12 serial clock I/O pin Trace clock
175	P421 SIN2_1 SCS120_0 TRACECTL	- - - -	Q	General-purpose I/O port Multi-function serial ch.2 serial data input pin (1) Multi-function serial ch.12 chip select 0 I/O pin (0) Trace control
52	AVCC0	-	-	Analog power supply pin for AD converter unit 0
103	AVCC1	-	-	Analog power supply pin for AD converter unit 1
53	AVRH0	-	-	Upper-limit reference voltage pin for AD converter unit 0
102	AVRH1	-	-	Upper-limit reference voltage pin for AD converter unit 1
54	AVSS0 AVRL0	- -	-	GND pin for AD converter unit 0 Lower-limit reference voltage pin for AD converter unit 0
101	AVSS1 AVRL1	- -	-	GND pin for AD converter unit 1 Lower-limit reference voltage pin for AD converter unit 1
46	C	-	-	External capacity connection output pin
154				
44	VCC	-	-	Power supply pin
88				
133				
152				
176				
1	VSS	-	-	GND
45				
89				
132				
148				
153				

Pin No. S6J311xHzC	Pin Name	Polarity	I/O Circuit Type	Function
18	P020 SOT0_0 SDA0_0 TIOB1_0 TEXT1_0	- - - - -	P	General-purpose I/O port Multi-function serial ch.0 serial data output pin (0) I²C bus ch.0 serial data I/O pin Base timer ch.1 TIOB input pin (0) Free-run timer 1 clock input pin (0)
19	P021 SCK0_0 SCL0_0 TIOB2_0	- - - -	P	General-purpose I/O port Multi-function serial ch.0 clock I/O pin (0) I²C bus ch.0 serial clock I/O pin Base timer ch.2 TIOB input pin (0)
20	P022 SIN0_0 TIOB3_0 INT3_0	- - - -	P	General-purpose I/O port Multi-function serial ch.0 serial data input pin (0) Base timer ch.3 TIOB input pin (0) INT3 external interrupt input pin (0)
21	P023 SCS0_0 TIOB4_0	- - -	P	General-purpose I/O port Multi-function serial ch.0 chip select I/O pin (0) Base timer ch.4 TIOB input pin (0)
22	P024 TIOB5_0	- -	P	General-purpose I/O port Base timer ch.5 TIOB input pin (0)
23	P027 TIOA4_1 TIOB6_0 INT1_1 TEXT0_1	- - - - -	P	General-purpose I/O port Base timer ch.4 TIOA output pin (1) Base timer ch.6 TIOB input pin (0) INT1 external interrupt input pin (1) Free-run timer 0 clock input pin (1)
24	P028 SIN1_0 TIOB7_0 INT4_0 OUT0_1	- - - - -	P	General-purpose I/O port Multi-function serial ch.1 serial data input pin (0) Base timer ch.7 TIOB input pin (0) INT4 external interrupt input pin (0) Output compare ch.0 output pin (1)
25	P029 SOT1_0 SDA1_0 AN0 OUT1_1	- - - - -	A	General-purpose I/O port Multi-function serial ch.1 serial data output pin (0) I²C bus ch.1 serial data I/O pin ADC analog 0 input pin Output compare ch.1 output pin (1)
26	P030 OUT2_1	- -	P	General-purpose I/O port Output compare ch.2 output pin (1)
27	P031 SCS1_0 AN1 OUT3_1	- - - -	A	General-purpose I/O port Multi-function serial ch.1 chip select I/O pin (0) ADC analog 1 input pin Output compare ch.3 output pin (1)
28	P100 SCK1_0 SCL1_0 AN2 OUT4_1	- - - - -	A	General-purpose I/O port Multi-function serial ch.1 clock I/O pin (0) I²C bus ch.1 serial clock I/O pin ADC analog 2 input pin Output compare ch.4 output pin (1)
29	P101 AN3 OUT5_1	- - -	A	General-purpose I/O port ADC analog 3 input pin Output compare ch.5 output pin (1)
30	P103 AN5 OUT6_1	- - -	A	General-purpose I/O port ADC analog 5 input pin Output compare ch.6 output pin (1)
31	P105 TIOA9_0 OUT7_1	- - -	P	General-purpose I/O port Base timer ch.9 TIOA output pin (0) Output compare ch.7 output pin (1)
32	P106 OUT8_1	- -	P	General-purpose I/O port Output compare ch.8 output pin (1)

Type	Circuit	Overview
Q		− General-purpose I/O port − Output of 1 mA or 2 mA selectable − 50 kΩ with pull-up resistor control − 50 kΩ with pull-down resistor control − Automotive/CMOS hysteresis input selectable
R		− Output of 2 mA

START Address	END Address	Group	Function	PPU No
B480_0000	B480_03FF	CommonPERI #0	M.F.Serial ch.0	176
B480_0400	B480_07FF	CommonPERI #0	M.F.Serial ch.1	177
B480_0800	B480_0BFF	CommonPERI #0	M.F.Serial ch.2	178
B480_0C00	B480_0FFF	CommonPERI #0	M.F.Serial ch.3	179
B480_1000	B480_7FFF		Reserved	-
B480_8000	B480_83FF	CommonPERI #0	BaseTimer ch.0	88
B480_8400	B480_87FF	CommonPERI #0	BaseTimer ch.1	89
B480_8800	B480_8BFF	CommonPERI #0	BaseTimer ch.2	90
B480_8C00	B480_8FFF	CommonPERI #0	BaseTimer ch.3	91
B480_9000	B480_93FF	CommonPERI #0	BaseTimer ch.4	92
B480_9400	B480_97FF	CommonPERI #0	BaseTimer ch.5	93
B480_9800	B480_9BFF	CommonPERI #0	BaseTimer ch.6	94
B480_9C00	B480_9FFF	CommonPERI #0	BaseTimer ch.7	95
B480_A000	B480_A3FF	CommonPERI #0	BaseTimer ch.8	96
B480_A400	B480_A7FF	CommonPERI #0	BaseTimer ch.9	97
B480_A800	B480_ABFF	CommonPERI #0	BaseTimer ch.10	98
B480_AC00	B480_AFFF	CommonPERI #0	BaseTimer ch.11	99
B480_B000	B481_FFFF		Reserved	-
B482_0000	B482_03FF	CommonPERI #0	FRT ch.0	208
B482_0400	B482_07FF	CommonPERI #0	FRT ch.1	209
B482_0800	B482_0BFF	CommonPERI #0	FRT ch.2	210
B482_0C00	B482_0FFF	CommonPERI #0	FRT ch.3	211
B482_1000	B482_13FF	CommonPERI #0	FRT ch.4	212
B482_1400	B482_17FF	CommonPERI #0	FRT ch.5	213
B482_1800	B482_7FFF		Reserved	-
B482_8000	B482_83FF	CommonPERI #0	ICU ch.0 / ch1	224
B482_8400	B482_87FF	CommonPERI #0	ICU ch.2 / ch3	225
B482_8800	B482_8BFF	CommonPERI #0	ICU ch.4 / ch5	226
B482_8C00	B482_8FFF	CommonPERI #0	ICU ch.6 / ch7	227
B482_9000	B482_93FF	CommonPERI #0	ICU ch.8 / ch9	228
B482_9400	B482_97FF	CommonPERI #0	ICU ch.10 / ch11	229
B482_9800	B482_FFFF		Reserved	-
B483_0000	B483_03FF	CommonPERI #0	OCU ch.0 / ch1	240
B483_0400	B483_07FF	CommonPERI #0	OCU ch.2 / ch3	241
B483_0800	B483_0BFF	CommonPERI #0	OCU ch.4 / ch5	242
B483_0C00	B483_0FFF	CommonPERI #0	OCU ch.6 / ch7	243
B483_1000	B483_13FF	CommonPERI #0	OCU ch.8 / ch9	244
B483_1400	B483_17FF	CommonPERI #0	OCU ch.10 / ch11	245
B483_1800	B483_FBFF		Reserved	-
B483_FC00	B483_FFFF		Reserved	-
B484_0000	B484_FFFF	APPS #5	APPS#5 area	-
B485_0000	B489_FFFF		Reserved	-
B48A_0000	B48B_0FFF		Reserved	-
B48B_1000	B48B_FBFF		Reserved	-
B48B_FC00	B48B_FFFF		Reserved	-
B48C_0000	B48F_FFFF		Reserved	-
B490_0000	B490_FFFF	CommonPERI #0	CAN_FD ch0	256
B491_0000	B4BF_FFFF		Reserved	-
B4C0_0000	B4FF_FFFF	Bit RMW alias	Bit RMW alias for CPERI#0(Covers B490_0000 -- B497_FFFF)	-
B500_0000	B5FF_FFFF		Reserved	-
B600_0000	B6FF_FFFF		Reserved	-
B700_0000	B77F_FFFF	Bit RMW alias	Bit RMW alias for CPERI#2 (Covers B470_0000 -- B47F_FFFF)	-
B780_0000	B7BF_FFFF	Bit RMW alias	Bit RMW alias for CPERI#0 (Covers B480_0000 -- B487_FFFF)	-
B7C0_0000	B7FF_FFFF		Reserved	-
B800_0000	FFFE_DFFF		Reserved	-
FFFE_E000	FFFE_FBFC	Error Config	IRC	-
FFFE_FC00	FFFE_FFFF	Error Config	BootROM I/F	20

Table 8-4 S6J311xHzC APPS#5 Area

* x:E/D/C/B, z:A/B

START Address	END Address	Group	Function	PPU No
B484_0000	B484_37FF		Reserved	-
B484_3800	B484_3BFF	APPS #5	BaseTimer ch.12	278
B484_3C00	B484_3FFF	APPS #5	BaseTimer ch.13	279
B484_4000	B484_43FF	APPS #5	BaseTimer ch.14	280
B484_4400	B484_47FF	APPS #5	BaseTimer ch.15	281
B484_4800	B484_4BFF	APPS #5	BaseTimer ch.16	282
B484_4C00	B484_4FFF	APPS #5	BaseTimer ch.17	283
B484_5000	B484_53FF	APPS #5	BaseTimer ch.18	284
B484_5400	B484_57FF	APPS #5	BaseTimer ch.19	285
B484_5800	B484_5BFF	APPS #5	BaseTimer ch.20	286
B484_5C00	B484_5FFF	APPS #5	BaseTimer ch.21	287
B484_6000	B484_63FF	APPS #5	BaseTimer ch.22	288
B484_6400	B484_67FF	APPS #5	BaseTimer ch.23	289
B484_6800	B484_6BFF	APPS #5	BaseTimer ch.24	290
B484_6C00	B484_6FFF	APPS #5	BaseTimer ch.25	291
B484_7000	B484_73FF	APPS #5	BaseTimer ch.26	292
B484_7400	B484_77FF	APPS #5	BaseTimer ch.27	293
B484_7800	B484_7BFF	APPS #5	BaseTimer ch.28	294
B484_7C00	B484_7FFF	APPS #5	BaseTimer ch.29	295
B484_8000	B484_83FF	APPS #5	A/D unit0	296
B484_8400	B484_87FF	APPS #5	A/D unit1 , Partial Wake Up	297
B484_8800	B484_8BFF	APPS #5	A/D analog input control	298
B484_8C00	B484_8FFF		Reserved	-
B484_9000	B484_93FF	APPS #5	Global Timer	300
B484_9400	B484_FFFF		Reserved	-

When MPU attribute of Cortex-R5 is configured as "Normal", store buffer inside Cortex-R5 can operate and write data can be merged. To avoid influence of this data merger, MPU attribute "Device" or "Strongly Ordered" should be used.

MPU attribute "Device" or "Strongly Ordered" must be used for areas below, to avoid this influence.

- *Backup RAM area (BACKUP_RAM) [0E80_0000 ~ 0E87_FFFF]*
- *Peripheral area (Peri area) [B000_0000 ~ B7FF_FFFF]*
- *Error Config area (ERRCFG) [FFFE_E000 ~ FFFE_FFFF]*

MPU attribute "Device" or "Strongly Ordered" is required for accesses to areas below, in particular situation.

- *FLASH Memory (when writing commands)*

SHE OFF product is prohibited to access SHE area (B200_0000 to B20F_FFFF)

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog supply voltage*1, *2	AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	Vcc=AVcc
Analog reference voltage*1	AVRH	V_{SS}-0.3	V_{SS}+6.0	V	AVRH≤AV_{CC}
Input voltage*1	V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage*1	V_{IA}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage*1	V_O	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current	I_{CLAMP}	-	4	mA	*7
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	-	20	mA	*7
"L"-level maximum output current*3	I_{OL1}	-	3.5	mA	When setting is 1 mA*6
	I_{OL2}	-	7	mA	When setting is 2 mA
"L"-level average output current*4	I_{OLAV1}	-	1	mA	When setting is 1 mA*6
	I_{OLAV2}	-	2	mA	When setting is 2 mA
"L"-level total output current*5	ΣI_{OL}	-	40	mA	*6
"H"-level maximum output current*3	I_{OH1}	-	-3.5	mA	When setting is 1 mA*6
	I_{OH2}	-	-7	mA	When setting is 2 mA
"H"-level average output current*4	I_{OHAV1}	-	-1	mA	When setting is 1 mA*6
	I_{OHAV2}	-	-2	mA	When setting is 2 mA
"H"-level total output current*5	ΣI_{OH}	-	-40	mA	*6
Power consumption	P_D	-	2000	mW	*8
Operating temperature	T_A	-40	+105	℃	
Storage temperature	Tstg	-55	+150	℃	

*1: These parameters are based on the condition that VSS=AVSS=0.0V.

*2: AVCC and VCC must be set to the same voltage. It is required that AVCC does not exceed VCC and that the voltage at the analog inputs does not exceed AVCC when the power is switched on.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current X the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Corresponding pins: general-purpose ports

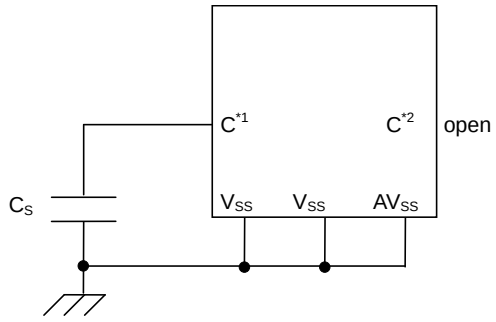
10.2 Recommended Operating Conditions

(V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}	4.5	5.25	V	Recommended operation assurance range
	AV_{CC}	4.5	5.25	V	
	V_{CC}	3.5	5.25	V	Operation assurance range
	AV_{CC}	3.5	5.25	V	
Smoothing capacitor*	C_S	4.7		µF	Tolerance of up to ±40% 154pin(LEP176) / 126pin(LES144) Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than CS as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	See the notes below.

*: For the connections of smoothing capacitor C_S, see the following diagram.

▪ C Pin Connection Diagram



1: 154pin(S6J311xJzC) / 126pin(S6J311xHzC*)
2: 46pin(S6J311xJzC) / 38pin(S6J311xHzC*)
* x: E/D/C/B, z: A/B

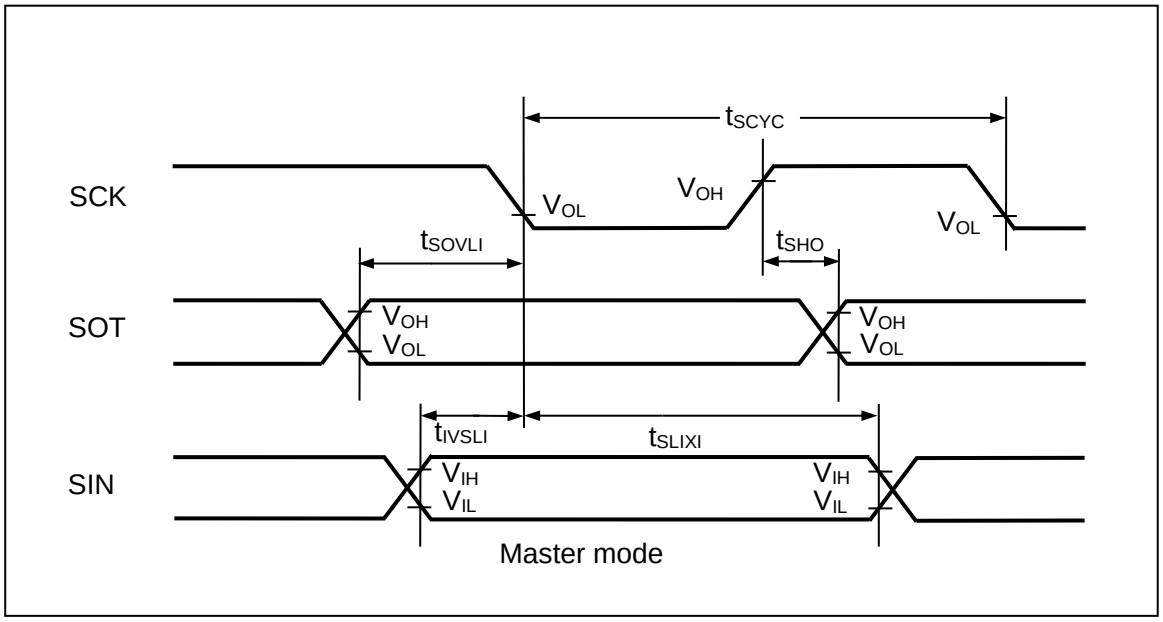
WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

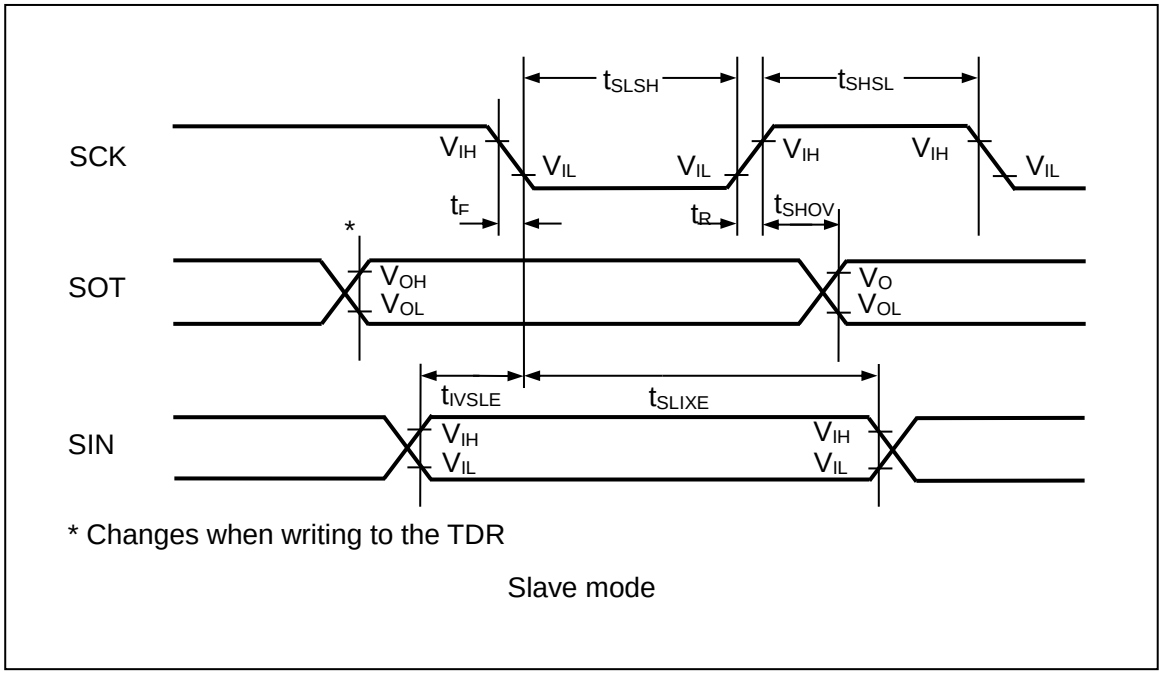
10.3 DC Characteristics

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421	CMOS Schmitt input level selected	0.7×V_{CC}	-	V_{CC}+0.3	V	
	V_{IH2}	P401 to P421	Automotive input level selected	0.8×V_{CC}	-	V_{CC}+0.3	V	
	V_{IH4}	RSTX, NMIX	-	0.7×V_{CC}	-	V_{CC}+0.3	V	
	V_{IH5}	MD	-	0.7×V_{CC}	-	V_{CC}+0.3	V	
	V_{IH6}	TRST, TCK, TDI, TMS	TTL	2.3	-	V_{CC}+0.3	V	
"L" level input voltage	V_{IL1}	P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421	CMOS Schmitt input level selected	Vss-0.3	-	0.3×V_{CC}	V	
	V_{IL2}	P401 to P421	Automotive input level selected	Vss-0.3	-	0.5×V_{CC}	V	
	V_{IL4}	RSTX, NMIX	-	Vss-0.3	-	0.3×V_{CC}	V	
	V_{IL5}	MD	-	Vss-0.3	-	0.3×V_{CC}	V	
	V_{IL6}	TRST, TCK, TDI, TMS	TTL	Vss-0.3	-	0.8	V	



Master mode



* Changes when writing to the TDR

Slave mode

(5-1-5) Serial Chip Select Used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H" (SMR, SCSFR:SCINV=0)
- Serial chip select inactive level "H" (SCSCR, SCSFR:CSLVL=1)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

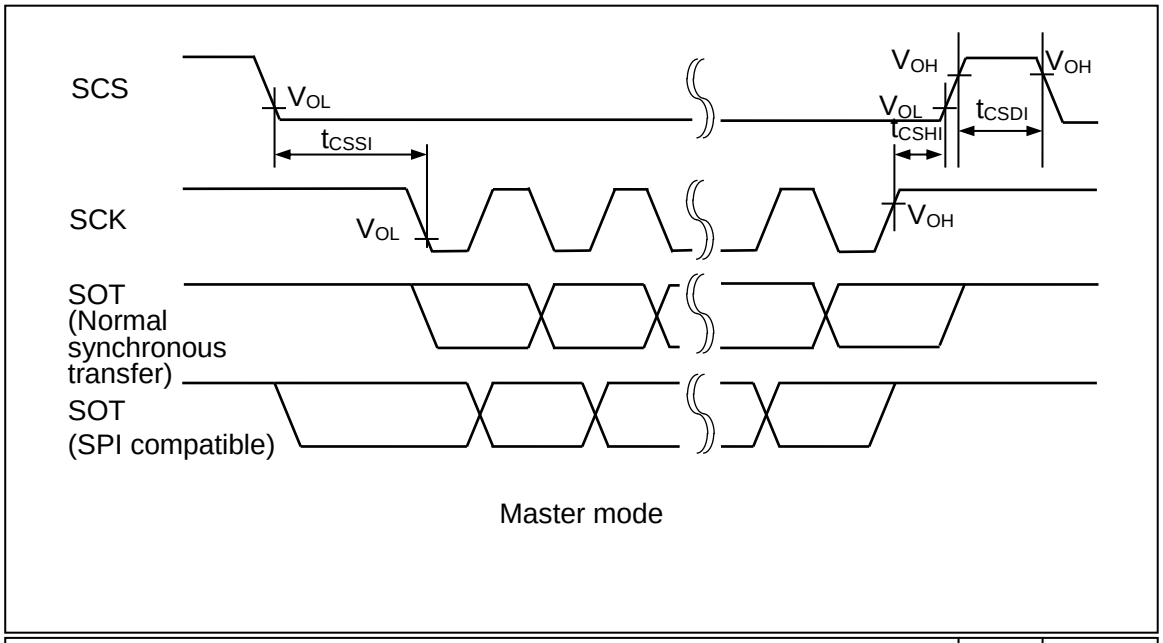
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ →SCK ↓ setup time	t_{CSSI}	SCK0 to SCK21 SCS0x to SCS21x	Master mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	t_{CSSU}*1-50	-	ns	
SCK ↑ →SCS ↑ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS0x to SCS21x		t_{CSDS}*3-50 +5t_{CLK_LCP0A}	-	ns	
SCS ↓ →SCK ↓ setup time	t_{CSSE}	SCK0 to SCK21 SCS0x to SCS21x	Slave mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	3t_{CLK_LCP0A} +30	-	ns	
SCK ↑ →SCS ↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS0x to SCS21x		3t_{CLK_LCP0A} +30	-	ns	
SCS ↓ →SOT delay time	t_{DSE}	SCS0x to SCS21x SOT0 to SOT21		-	50	ns	
SCS ↑ →SOT delay time	t_{DEE}			0	-	ns	
SCK ↓ →SCS ↓ clock switch time	t_{SCC}	SCK0 to SCK21 SCS0x to SCS21x	Master mode round operation (CL=50pF, IOL=-2mA, IOH=2mA), (CL=20pF, IOL=-1mA, IOH=1mA)	3t_{CLK_LCP0A} +0	3t_{CLK_LCP0A} +50	ns	

*1: tCSSU =SCSTR:CSSU[7:0] x serial chip select timing operation clock

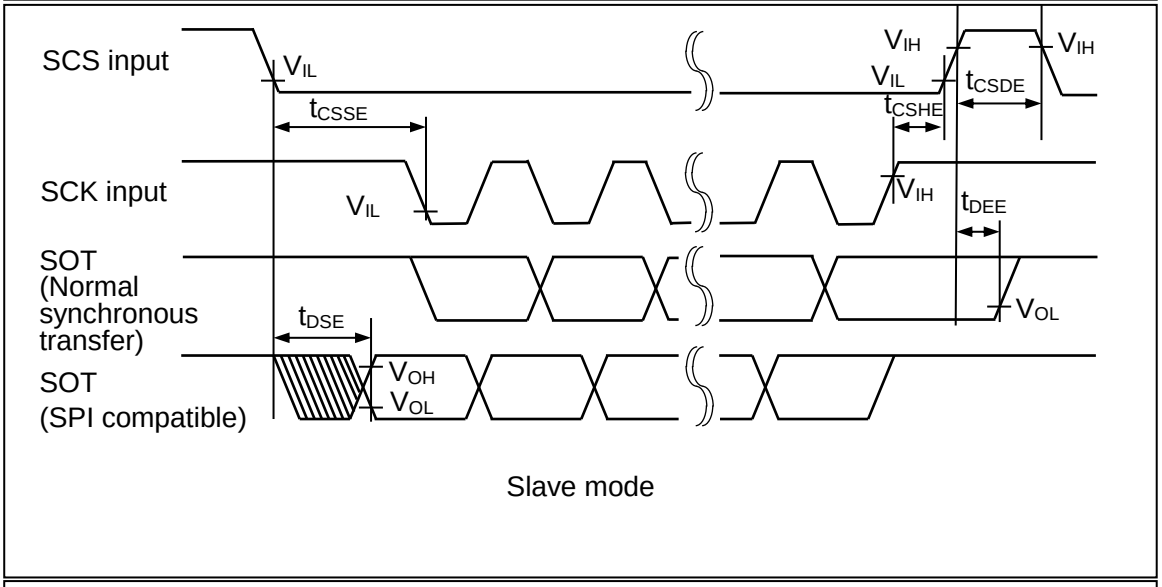
*2: tCSHD=SCSTR:CSHD[7:0] x serial chip select timing operation clock

*3: tCSDS=SCSTR:CSDS[15:0] x serial chip select timing operation clock

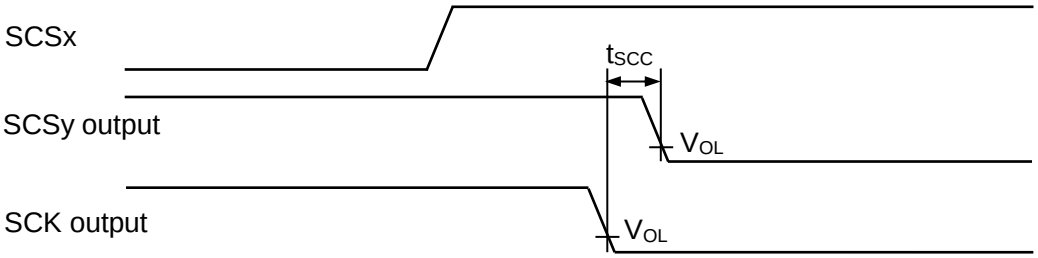
For details on *1, *2, and *3 above, see the hardware manual.



Master mode



Slave mode



Clock switching example by master mode round operation
(x,y=0,1,2,3: x and y are different value.)

(5-1-7) Serial Chip Select Used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H"(SMR, SCSFR:SCINV=0)
- Serial Chip select inactive level "L"(SCSCR, SCSFR:CSLVL=0)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ →SCK ↓ setup time	t_{CSSI}	SCK0 to SCK21 SCS0x to SCS21x	Master mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	t_{CSSU}*1-50	-	ns	
SCK ↑ →SCS ↓ hold time	t_{CSHI}			t_{CSHD}*2+0	-	ns	
SCS deselect time	t_{CSDI}	SCS0x to SCS21x		t_{CSDS}*3-50+5 t_{CLK_LCP0A}	-	ns	
SCS ↑ →SCK ↓ setup time	t_{CSSE}	SCK0 to SCK21 SCS0x to SCS21x	Slave mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	$3t_{CLK\_LCP0A}$ +30	-	ns	
SCK ↑ →SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS0x to SCS21x		$3t_{CLK\_LCP0A}$ +30	-	ns	
SCS ↑ →SOT delay time	t_{DSE}	SCS0x to SCS21x SOT0 to SOT21		-	50	ns	
SCS ↓ →SOT delay time	t_{DEE}			0	-	ns	
SCK ↓ →SCS ↑ clock switch time	t_{SCC}	SCK0 to SCK21 SCS0x to SCS21x	Master mode round operation (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	$3t_{CLK\_LCP0A}$ +0	$3t_{CLK\_LCP0A}$ +50	ns	

*1: tCSSU =SCSTR:CSSU[7:0] x serial chip select timing operation clock

*2: tCSHD=SCSTR:CSHD[7:0] x serial chip select timing operation clock

*3: tCSDS=SCSTR:CSDS[15:0] x serial chip select timing operation clock

For details on *1, *2, and *3 above, see the hardware manual.

Notes:

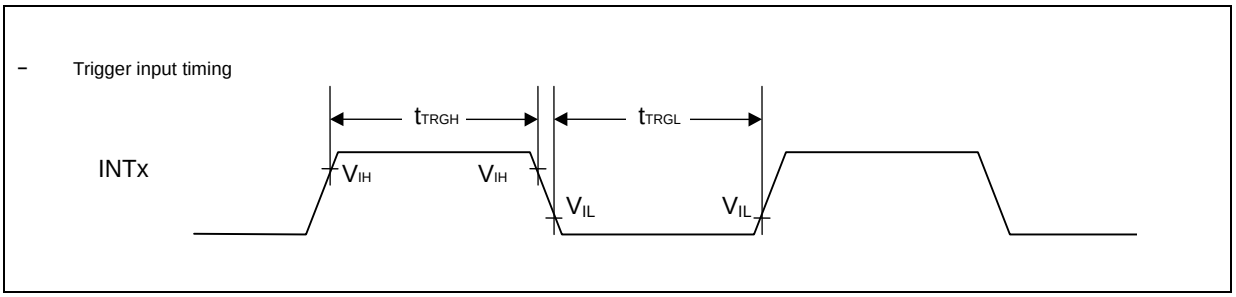
- *This is the AC characteristic in CLK synchronized mode.*
- *CL is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual*

10.6 Trigger Input Timing

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT15	-	100	-	ns	
		INT0 to INT15	-	1	-	µs	Stop mode

- Trigger input timing

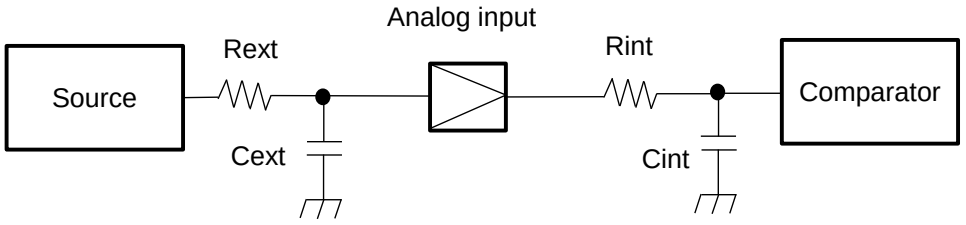


10.11.2 Notes on Using A/D Converter

About the Output Impedance of an External Circuit for Analog Input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 µF) to an analog input pin.

Analog input circuit model



Rint : Analog input impedance
3.9 kiloohms (max) (4.5 V≤AVcc≤5.25 V)
Cint : Capacitance of MCU input pin
11.0pF (max) (4.5 V≤AVcc≤5.25 V)
Rext : External driving impedance
Cext : Capacitance of PCB at A/D converter input

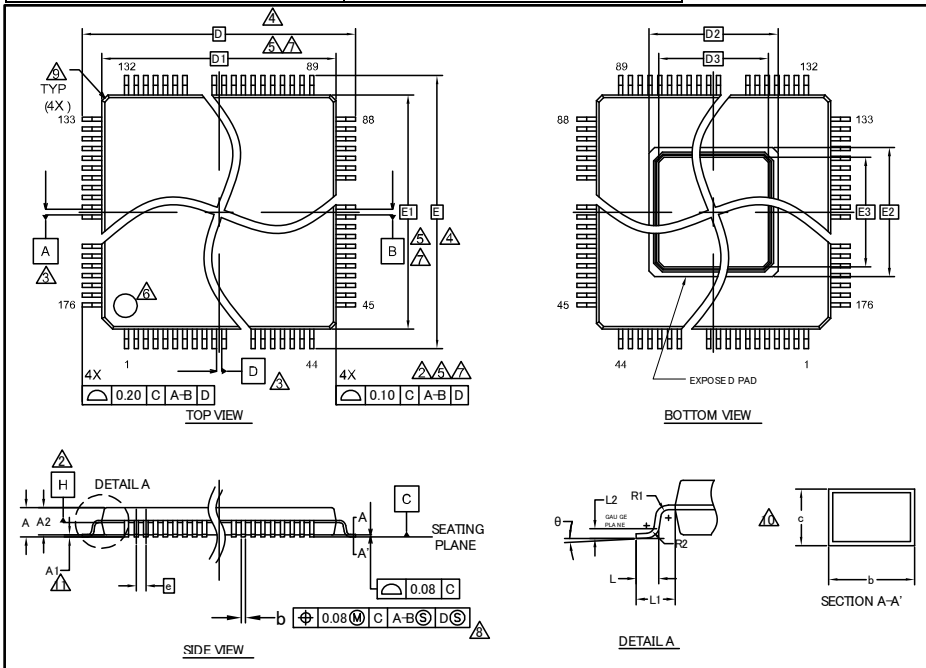
The following approximation formula for the replacement model above can be used:
sampling time (minimum) = 9 x ((Rin + Rext) x Cin + Rext x Cext)

Note: Listed values must be considered as reference values.

13. Package Dimensions

Figure 13-1 LEP176 Package Dimension

Package Type	Package Code
Ex-LQFP 176	LEP176



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
A2	1.35	1.40	1.45
D		26.00 BSC.	
D1		24.00 BSC.	
D2		9.26 REF	
D3		8.06 REF	
E		26.00 BSC.	
E1		24.00 BSC.	
E2		9.26 REF	
E3		8.06 REF	
R1	0.08	——	——
R2	0.08	——	0.20
θ	0°	4°	8°
c	0.12	——	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25	
e		0.50 BSC.	

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

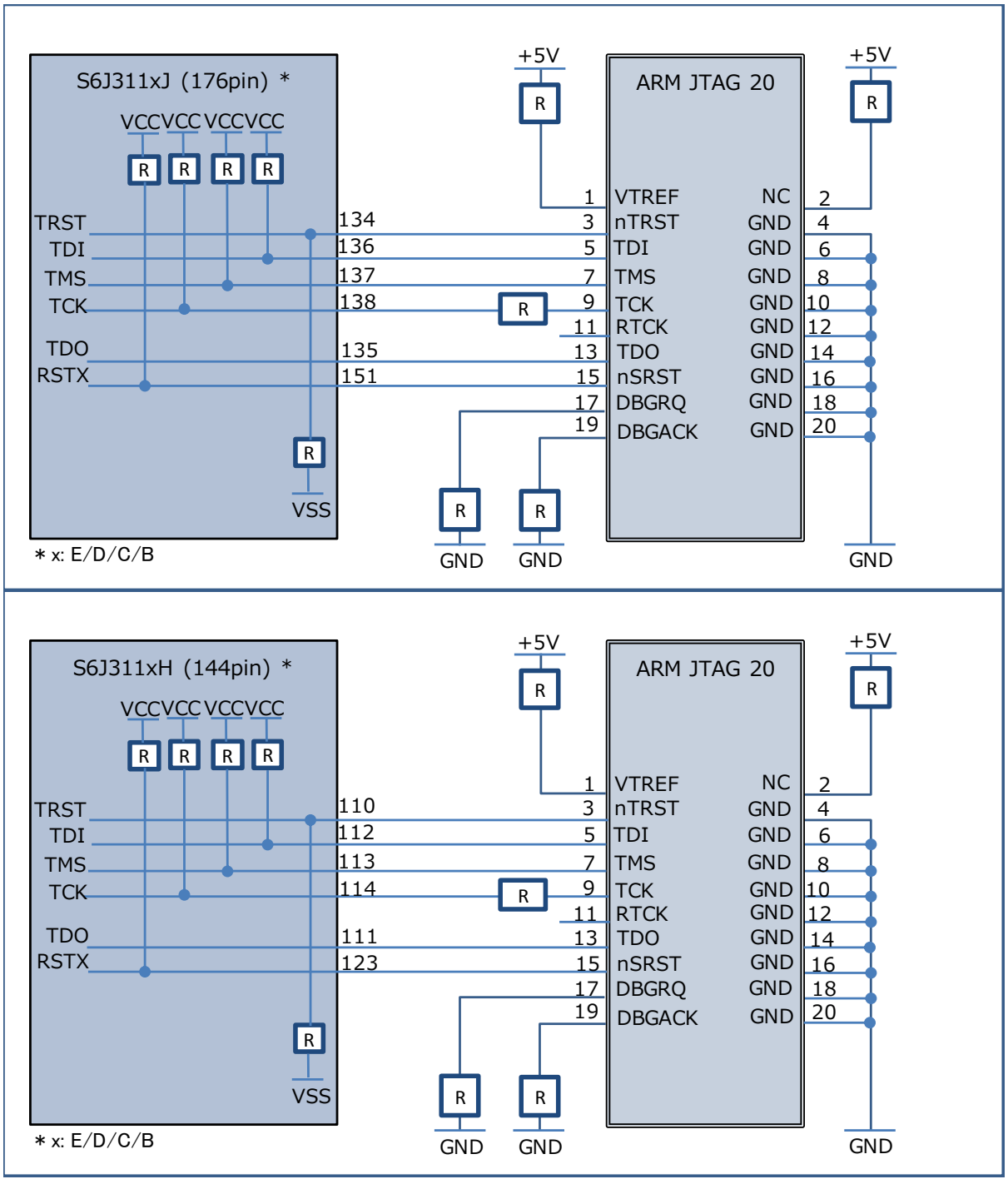
002-13652 **

PACKAGE OUTLINE, 176 LEAD TEQFP
24.0X24.0X1.7 MM LEP176 REV**

14. Appendix

14.1 Application 1: JTAG tool connection

This is an application example of JTAG tool connection. See the relevant application note AN203911 in detail.



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