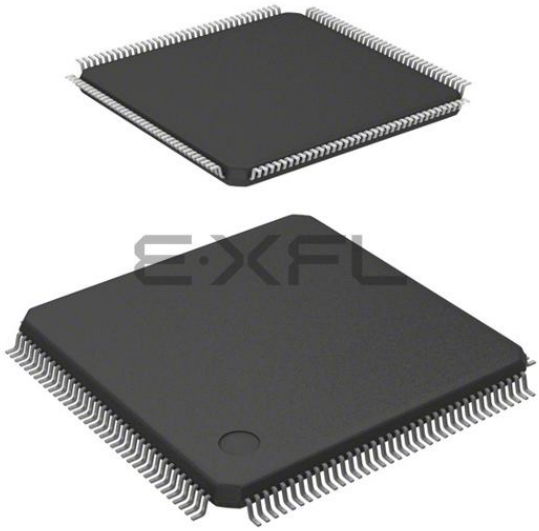

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

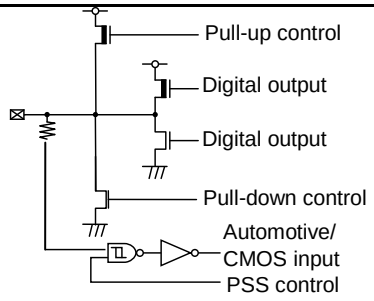
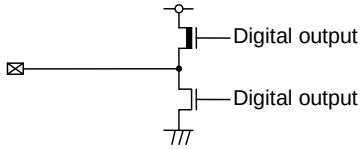
Details	
Product Status	Active
Core Processor	ARM® Cortex®-R5F
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	150
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6j311ejaase2000a

Pin No. S6J311xJzC	Pin Name	Polarity	I/O Circuit Type	Function
30	P028 SIN1_0 TIOB7_0 INT4_0 OUT0_1	- - - - -	P	General-purpose I/O port Multi-function serial ch.1 serial data input pin (0) Base timer ch.7 TIOB input pin (0) INT4 external interrupt input pin (0) Output compare ch.0 output pin (1)
31	P029 SOT1_0 SDA1_0 AN0 OUT1_1	- - - - -	A	General-purpose I/O port Multi-function serial ch.1 serial data output pin (0) I^2C bus ch.1 serial data I/O pin ADC analog 0 input pin Output compare ch.1 output pin (1)
32	P030 SCS43_1 OUT2_1	- - -	P	General-purpose I/O port Multi-function serial chip ch.4 select 3 output pin (1) Output compare ch.2 output pin (1)
33	P031 SCS1_0 AN1 OUT3_1	- - - -	A	General-purpose I/O port Multi-function serial ch.1 chip select I/O pin (0) ADC analog 1 input pin Output compare ch.3 output pin (1)
34	P100 SCK1_0 SCL1_0 AN2 OUT4_1	- - - - -	A	General-purpose I/O port Multi-function serial ch.1 clock I/O pin (0) I^2C bus ch.1 serial clock I/O pin ADC analog 2 input pin Output compare ch.4 output pin (1)
35	P101 AN3 OUT5_1	- - -	A	General-purpose I/O port ADC analog 3 input pin Output compare ch.5 output pin (1)
36	P102 AN4	- -	A	General-purpose I/O port ADC analog 4 input pin
37	P103 SIN17_0 AN5 OUT6_1	- - - -	A	General-purpose I/O port Multi-function serial ch.17 serial data input pin (0) ADC analog 5 input pin Output compare ch.6 output pin (1)
38	P104 SOT17_0 SDA17_0	- - -	P	General-purpose I/O port Multi-function serial ch.17 serial data output pin (0) I^2C bus ch.17 serial data I/O pin
39	P105 SCK17_0 SCL17_0 TIOA9_0 OUT7_1	- - - - -	P	General-purpose I/O port Multi-function serial ch.17 clock I/O pin (0) I^2C bus ch.17 serial clock I/O pin Base timer ch.9 TIOA output pin (0) Output compare ch.7 output pin (1)
40	P106 TX1_2 SCS170_0 OUT8_1	- - - -	P	General-purpose I/O port CAN transmission data 1 output pin (2) Multi-function serial ch.17 chip select 0 I/O pin (0) Output compare ch.8 output pin (1)
41	P107 RX1_2 SIN19_0 TIOA10_0 INT2_1 OUT9_1	- - - - - -	P	General-purpose I/O port CAN reception data 1 input pin (2) Multi-function serial ch.19 serial data input pin (0) Base timer ch.10 TIOA output pin (0) INT2 external interrupt input pin (1) Output compare ch.9 output pin (1)
42	P108 SOT19_0 SDA19_0 AN6 TIOA11_0 INT3_1 OUT10_1	- - - - - - -	A	General-purpose I/O port Multi-function serial ch.19 serial data output pin (0) I^2C bus ch.19 serial data I/O pin ADC analog 6 input pin Base timer ch.11 TIOA output pin (0) INT3 external interrupt input pin (1) Output compare ch.10 output pin (1)

Pin No. S6J311xJzC	Pin Name	Polarity	I/O Circuit Type	Function
43	P109 SIN19_1 SCK19_0 SCL19_0 TIOA12_0 OUT11_1	- - - - - -	P	General-purpose I/O port Multi-function serial ch.19 serial data input pin (1) Multi-function serial ch.19 clock I/O pin (0) I²C bus ch.19 serial clock I/O pin Base timer ch.12 TIOA output pin (0) Output compare ch.11 output pin (1)
47	P110 SCS190_0 AN7	- - -	A	General-purpose I/O port Multi-function serial ch.19 chip select 0 I/O pin (0) ADC analog 7 input pin
48	P111 SIN18_0 AN8	- - -	A	General-purpose I/O port Multi-function serial ch.18 serial data input pin (0) ADC analog 8 input pin
49	P112 SOT18_0 SDA18_0 AN9 TIOA13_0	- - - - -	A	General-purpose I/O port Multi-function serial ch.18 serial data output pin (0) I²C bus ch.18 serial data I/O pin ADC analog 9 input pin Base timer ch.13 TIOA output pin (0)
50	P113 SOT19_1 SCK18_0 SCL18_0 TIOA5_1	- - - - -	P	General-purpose I/O port Multi-function serial ch.19 serial data output pin (1) Multi-function serial ch.18 clock I/O pin (0) I²C bus ch.18 serial clock I/O pin Base timer ch.5 TIOA output pin (1)
51	P114 SCS180_0 AN10 TIOA6_1	- - - -	A	General-purpose I/O port Multi-function serial ch.18 chip select 0 I/O pin (0) ADC analog 10 input pin Base timer ch.6 TIOA output pin (1)
55	P115	-	P	General-purpose I/O port
56	P116 AN11	- -	A	General-purpose I/O port ADC analog 11 input pin
57	P117 AN12 INT4_1	- - -	A	General-purpose I/O port ADC analog 12 input pin INT4 external interrupt input pin (1)
58	P118 AN13 INT5_1	- - -	A	General-purpose I/O port ADC analog 13 input pin INT5 external interrupt input pin (1)
59	P119 SCS60_0 AN14	- - -	A	General-purpose I/O port Multi-function serial ch.6 chip select 0 I/O pin (0) ADC analog 14 input pin
60	P120 SCS61_0 AN15	- - -	A	General-purpose I/O port Multi-function serial ch.6 chip select 1 output pin (0) ADC analog 15 input pin
61	P121 SCS160_0 AN16 TIOA14_0	- - - -	A	General-purpose I/O port Multi-function serial ch.16 chip select 0 I/O pin (0) ADC analog 16 input pin Base timer ch.14 TIOA output pin (0)
62	P122 SCS62_0 AN17 TIOA11_1	- - - -	A	General-purpose I/O port Multi-function serial ch.6 chip select 2 output pin (0) ADC analog 17 input pin Base timer ch.11 TIOA output pin (1)
63	P123 SCS63_0 AN18 TIOA12_1	- - - -	A	General-purpose I/O port Multi-function serial ch.6 chip select 3 output pin (0) ADC analog 18 input pin Base timer ch.12 TIOA output pin (1)
64	P124 SIN16_0 TIOA15_0	- - -	P	General-purpose I/O port Multi-function serial ch.16 serial data input pin (0) Base timer ch.15 TIOA output pin (0)

Pin No. S6J311xJzC	Pin Name	Polarity	I/O Circuit Type	Function
118	P308 IN0_1 SCK13_0 SCL13_0 AN56 TIOA28_1	- - - - - -	A	General-purpose I/O port Input capture ch.0 input pin (1) Multi-function serial ch.13 clock I/O pin (0) I^2C bus ch.13 serial clock I/O pin ADC analog 56 input pin Base timer ch.28 TIOA output pin (1)
119	P309 IN1_1 SCS130_0 AN57 TIOA29_1	- - - - -	A	General-purpose I/O port Input capture ch.1 input pin (1) Multi-function serial ch.13 chip select 0 I/O pin (0) ADC analog 57 input pin Base timer ch.29 TIOA output pin (1)
120	P310 SIN13_0 INT15_0	- - -	P	General-purpose I/O port Multi-function serial ch.13 serial data input pin (0) INT15 external interrupt input pin (0)
121	P311 SOT13_0 SDA13_0	- - -	P	General-purpose I/O port Multi-function serial ch.13 serial data output pin (0) I^2C bus ch.13 serial data I/O pin
122	P312 IN2_1 SCS71_0 AN58	- - - -	A	General-purpose I/O port Input capture ch.2 input pin (1) Multi-function serial ch.7 chip select 1 output pin (0) ADC analog 58 input pin
123	P313 IN3_1 SOT7_0 SDA7_0 AN59 INT10_1	- - - - - -	A	General-purpose I/O port Input capture ch.3 input pin (1) Multi-function serial ch.7 serial data output pin (0) I^2C bus ch.7 serial data I/O pin ADC analog 59 input pin INT10 external interrupt input pin (1)
124	P314 IN4_1 SCK7_0 SCL7_0 AN60 TIOA7_1	- - - - - -	A	General-purpose I/O port Input capture ch.4 input pin (1) Multi-function serial ch.7 clock I/O pin (0) I^2C bus ch.7 serial clock I/O pin ADC analog 60 input pin Base timer ch.7 TIOA output pin (1)
125	P315 IN5_1 SCS70_0 AN61 TIOA8_1	- - - - -	A	General-purpose I/O port Input capture ch.5 input pin (1) Multi-function serial ch.7 chip select 0 I/O pin (0) ADC analog 61 input pin Base timer ch.8 TIOA output pin (1)
126	P316 TIOA21_1	- -	P	General-purpose I/O port Base timer ch.21 TIOA output pin (1)
127	P317 TX1_1 AN62 TIOA9_1 INT11_1	- - - - -	A	General-purpose I/O port CAN transmission data 1 output pin (1) ADC analog 62 input pin Base timer ch.9 TIOA output pin (1) INT11 external interrupt input pin (1)
128	P318 RX1_1 TIOA10_1 INT9_0	- - - -	P	General-purpose I/O port CAN reception data 1 input pin (1) Base timer ch.10 TIOA output pin (1) INT9 external interrupt input pin (0)
129	P319 SIN7_0 AN63 INT12_1	- - - -	A	General-purpose I/O port Multi-function serial ch.7 serial data input pin (0) ADC analog 63 input pin INT12 external interrupt input pin (1)
130	P320 PWUTRG	- -	P	General-purpose I/O port Partial wakeup trigger output pin
131	P321	-	D	General-purpose output port
134	TRST P322	N -	J	JTAG test reset input pin General-purpose output port

Pin No. S6J311xJzC	Pin Name	Polarity	I/O Circuit Type	Function
135	TDO P323	- -	I	JTAG test data output pin General-purpose output port
136	TDI P324	- -	D	JTAG test data input pin General-purpose output port
137	TMS	-	E	JTAG test mode state input pin
138	TCK	-	E	JTAG test clock input pin
139	P325 SIN21_0 INT10_0	- - -	P	General-purpose I/O port Multi-function serial ch.21 serial data input pin (0) INT10 external interrupt input pin (0)
140	P326 SOT21_0 SDA21_0	- - -	P	General-purpose I/O port Multi-function serial ch.21 serial data output pin (0) I^2C bus ch.21 serial data I/O pin
141	P327 SCK6_1 SCK21_0 SCL21_0	- - - -	P	General-purpose I/O port Multi-function serial ch.6 clock I/O pin (1) Multi-function serial ch.21 clock I/O pin (0) I^2C bus ch.21 serial clock I/O pin
142	P328 SOT6_1 SCS210_0	- - -	P	General-purpose I/O port Multi-function serial ch.6 serial data output pin (1) Multi-function serial ch.21 chip select 0 I/O pin (0)
143	P329 SIN6_1	- -	P	General-purpose I/O port Multi-function serial ch.6 serial data input pin (1)
144	P330	-	P	General-purpose I/O port
145	MD	-	C	Mode pin
146	X0	-	G	Main clock oscillation input pin
147	X1	-	G	Main clock oscillation output pin
149	P331 SCS60_1	- -	P	General-purpose I/O port Multi-function serial ch.6 chip select 0 I/O pin (1)
150	P400 SCS61_1	- -	P	General-purpose I/O port Multi-function serial ch.6 chip select 1 output pin (1)
151	RSTX	N	F	External reset input pin
155	P401 IN0_0 TX1_0 SCS62_1	- - - -	Q	General-purpose I/O port Input capture ch.0 input pin (0) CAN transmission data 1 output pin (0) Multi-function serial ch.6 chip select 2 output pin (1)
156	P402 IN1_0 RX1_0 SCS63_1 SCS90_0 INT2_0	- - - - - -	Q	General-purpose I/O port Input capture ch.1 input pin (0) CAN reception data 1 input pin (0) Multi-function serial ch.6 chip select 3 output pin (1) Multi-function serial ch.9 chip select 0 I/O pin (0) INT2 external interrupt input pin (0)
157	P403 IN2_0 TRACEDATA0	- - -	Q	General-purpose I/O port Input capture ch.2 input pin (0) Trace data 0 output pin
158	P404 IN3_0 TRACEDATA1	- - -	Q	General-purpose I/O port Input capture ch.3 input pin (0) Trace data 1 output pin
159	P405 IN4_0 SIN9_0 INT11_0 TRACEDATA2	- - - - -	Q	General-purpose I/O port Input capture ch.4 input pin (0) Multi-function serial ch.9 serial data input pin (0) INT11 external interrupt input pin (0) Trace data 2 output pin

Type	Circuit	Overview
Q		− General-purpose I/O port − Output of 1 mA or 2 mA selectable − 50 kΩ with pull-up resistor control − 50 kΩ with pull-down resistor control − Automotive/CMOS hysteresis input selectable
R		− Output of 2 mA

(1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

- Only the CPU core can access 0000_0000 ~ 01FF_FFFF. Bus masters other than the CPU core cannot access the region.
- Internal area of CR5 complex (0000_0000 ~ 01FF_FFFF) is mapped to AXI_SLAVE_CORE0. All bus masters can access to internal area of CR5 complex via AXI_SLAVE_CORE0.
- In each of the following memory area combinations, the areas are physically the same memory area.
  1. TCM FLASH (0x00A0_0000 -) and AXI FLASH MEMORY (0x01A0_0000 -)
  2. TCM FLASH Small Sector (0x009F_0000 -) and AXI FLASH MEMORY Small Sector (0x019F_0000 -)
  3. WORKFLASH (0x0E00_0000 -), WORKFLASH (0x0E20_0000 -), and WORKFLASH (0x0E30_0000 -)

The ECC movement in TCM port is based on ECC setting inside the CPU.

- The differences between the TCM FLASH and AXI FLASH include the following.

Function	TCM FLASH	AXI FLASH
High-speed Access Using Dedicated Bus	Applicable	Not applicable
Write and Erase	Not applicable (Read-only)	Applicable
Read	Applicable	Applicable

- The differences between WORKFLASH areas include the following.

Area	Function
WORKFLASH Area 1	Used in write operation (with ECC)
WORKFLASH Area 3	Used in write operation (without ECC)
WORKFLASH Area 4	Used in read operation

Table 8-1 S6J311xJzC* Peripheral Map

* x: E/D/C/B, z: A/B

START Address	END Address	Group	Function	PPU No
B000_0000	B010_7FFF		Reserved	-
B010_8000	B010_80FF	SystemSRAM	SystemSRAM registers	-
B010_8100	B02F_FFFF		Reserved	-
B030_0000	B030_7FFF	SYSC1	System Controller #1	-
B030_8000	B03F_FFFF	SYSC1	SWDT	-
B040_0000	B040_7FFF	MEMORY_CONFIG_GROUP	IRC0	21
B040_8000	B040_FFFF	MEMORY_CONFIG_GROUP	TPU0	19
B041_0000	B041_0FFF	MEMORY_CONFIG_GROUP	TCRAM Control Status Register	16
B041_1000	B041_1FFF	MEMORY_CONFIG_GROUP	TCFlash Control Status Register	17
B041_2000	B041_20FF	MEMORY_CONFIG_GROUP	WFlash Control Status Register	18
B041_2100	B04F_FFFF		Reserved	-
B050_0000	B05F_FFFF		Reserved	-
B060_0000	B060_007F	MCU_CONFIG_GROUP	Protection register area	-
B060_0080	B060_00FF	MCU_CONFIG_GROUP	RUN profile register area	-
B060_0100	B060_017F	MCU_CONFIG_GROUP	PSS profile register area	-
B060_0180	B060_01FF	MCU_CONFIG_GROUP	APP profile register area	-
B060_0200	B060_027F	MCU_CONFIG_GROUP	STS profile register area	-
B060_0280	B060_02FF	MCU_CONFIG_GROUP	System register area	-
B060_0300	B060_037F	MCU_CONFIG_GROUP	CSV	-
B060_0380	B060_03FF	MCU_CONFIG_GROUP	RESET	-
B060_0400	B060_047F	MCU_CONFIG_GROUP	SCT(Fast CR)	34
B060_0480	B060_04FF	MCU_CONFIG_GROUP	SCT(Slow CR)	33
B060_0500	B060_05FF	MCU_CONFIG_GROUP	SCT(Main clock)	35
B060_0600	B060_067F	MCU_CONFIG_GROUP	Clock System	-
B060_0680	B060_06FF	MCU_CONFIG_GROUP	Special register area	-
B060_0700	B060_07FF	MCU_CONFIG_GROUP	Debug register area	-
B060_0800	B060_BFFF	MCU_CONFIG_GROUP	Mode	-
B060_C000	B060_FFFF	MCU_CONFIG_GROUP	HWDT	-
B061_0000	B061_7FFF		Reserved	-
B061_8000	B061_FFFF	MCU_CONFIG_GROUP	RTC	32
B062_0000	B063_FFFF	MCU_CONFIG_GROUP	EIC	-
B064_0000	B065_FFFF		Reserved	-
B066_0000	B067_FFFF		Reserved	-
B068_0000	B068_7FFF	MCU_CONFIG_GROUP	BURAMIF	-
B068_8000	B068_83FF	MCU_CONFIG_GROUP	EICU	37
B068_8400	B068_87FF	MCU_CONFIG_GROUP	CR_Calibration	38
B068_8800	B068_8BFF	MCU_CONFIG_GROUP	IRQ_ALL	42
B068_8C00	B068_FFFF	MCU_CONFIG_GROUP	CAN Prescaler	43
B069_0000	B06F_FFFF		Reserved	-
B070_0000	B07F_FFFF		Reserved	-
B080_0000	B0FF_FFFF	Bit RMW alias	Bit RMW alias for MCU config Gr (Covers B060_0000 -- B06F_FFFF)	-
B100_0000	B10F_FFFF	Bit RMW alias	Bit RMW alias for SYSC1 (Covers B030_0000 -- B031_FFFF)	-
B110_0000	B11F_FFFF	Bit RMW alias	Bit RMW alias for MEMC (Covers B040_0000 -- B041_FFFF)	-
B120_0000	B1FF_FFFF		Reserved	-
B200_0000	B20F_FFFF	SHE	SHE configuration registers	63
B210_0000	B46F_FFFF		Reserved	-
B470_0000	B470_3FFF	CommonPERI#2	DMAC #0 registers	64
B470_4000	B470_FFFF		Reserved	-
B471_0000	B471_0FFF	CommonPERI#2	MPU for DMAC#0	66
B471_1000	B471_3FFF		Reserved	-
B471_4000	B471_4FFF	CommonPERI#2	DMA Complex #0 registers (Additional registers, RLTs)	68
B471_5000	B471_7FFF		Reserved	-
B471_8000	B471_83FF	CommonPERI#2	CRC#0	70
B471_8400	B471_87FF	CommonPERI#2	CRC#1	71
B471_8800	B471_8BFF	CommonPERI#2	CRC#2	72
B471_8C00	B471_8FFF	CommonPERI#2	CRC#3	73
B471_9000	B473_7FFF		Reserved	-
B473_8000	B473_FFFF	CommonPERI#2	GPIO	74
B474_0000	B474_7FFF	CommonPERI#2	PPC	75
B474_8000	B474_FFFF	CommonPERI#2	RIC	76
B475_0000	B475_7FFF	CommonPERI#2	PPU	-
B475_8000	B478_FBFF		Reserved	-
B478_FC00	B478_FFFF		Reserved	-
B479_0000	B47F_FFFF		Reserved	-

*1: Input disable is not valid when external interrupts are enabled.

*2: Recovery from standby (power off) becomes a factor.

*3: The pin state from the time that HOLDIO_PD2 was set (SYSC_SSPECFGR.HOLDIO_PD2=1) is retained. If power-off has not occurred and HOLDIO_PD2 has not been set (SYSC_SSPECFGR.HOLDIO_PD2=0), the last state is retained.

*4: To power off power domains 2 and 3, be sure to set HOLDIO_PD2 (SYSC_SSPECFGR.HOLDIO_PD2=1).

*5: When the PWU function is enabled, a change to output occurs.

*6: The pin state when the PORT function is enabled is shown.

*7: When PPC_PCFGRijj:POF[2:0] is set to initial value.

-External Reset Factor 1

Power-on reset (PONR)

RAM retention low-voltage detection reset (RVD)

Internal power supply low-voltage detection reset (LVDL1R)

RSTX pin + MD pin simultaneous assert reset (INITX)

-External Reset Factor 2

RSTX pin input reset (RSTX)

-External Reset Factor 3

Hardware watchdog reset (HWDR)

Software watchdog reset (SWDR)

PLL clock supervisor reset (CSVPRn)

SSCG clock supervisor reset (CSVSRn)

Profile error reset (PRFERR)

Software trigger hard reset (SHRST)

Software reset (SRST)

-Internal Reset Factor

Standby transition reset/ Power domain reset

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P000 to P031, P100 to P131, P200 to P231, P300 to P320, P321 to P324 P325 to P331, P400 to P421	Vcc=4.5 V I_{OH}=-2.0 mA	Vcc-0.5	-	Vcc	V	
"H" level output voltage	V_{OH2}	P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421	Vcc=4.5 V I_{OH}=-1.0 mA	Vcc-0.5	-	Vcc	V	
"L" level output voltage	V_{OL1}	P000 to P031, P100 to P131, P200 to P231, P300 to P320, P321 to P324 P325 to P331, P400 to P421	Vcc=4.5 V I_{OL}=2.0 mA	0	-	0.4	V	
"L" level output voltage	V_{OL2}	P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421	Vcc=4.5 V I_{OL}=1.0 mA	0	-	0.4	V	

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	$Vcc=AV_{CC}=5.25$ V $V_{SS} < VI < V_{CC}$	-5	-	+5	µA	
Pull-up resistor	R_{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R_{UP2}	P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421	Pull-up resistor selected	25	-	100	kΩ	
	R_{UP3}	TDI(P324),TMS, TCK	-	25	-	100	kΩ	
Pull-down resistor	R_{down1}	P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421	Pull-down resistor selected	25	-	100	kΩ	
	R_{down2}	TRST(P322)	-	25	-	100	kΩ	
Input capacitance	C_{IN}	Pins other than VCC, VSS, AVCC0,AVCC1, AVSS0,AVSS1	-	-	5	15	pF	

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

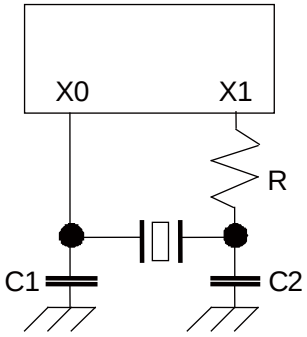
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC5}	VCC	Normal operation	-	140	320	mA	Operating at 144 MHz
			Flash write/erase	-	160	343	mA	Operating at 144 MHz
	I_{CCS5}		CPU Sleep	-	82	265	mA	Operating at 144 MHz
	I_{CCT5}		Timer mode	-	946.0	2967.9	µA	T_A=25°C Slow-CR source Oscillation
	I_{CCH5}		Stop mode	-	945.1	2966.2	µA	T_A=25°C
	I_{CCP}		PWU mode (Shutdown)	-	53.4	130.6	µA	T_A=25°C (PWU operation cycle 16ms)
				-	47.1	116.4	µA	T_A=25°C (PWU operation cycle 32ms)
	I_{CCT52}		Timer mode (Shutdown)	-	40.9	102.3	µA	T_A=25°C Slow-CR source Oscillation
	I_{CCH52}		Stop mode (Shutdown)	-	40.1	101.4	µA	T_A=25°C

Refer to Hardware manual “APPENDIX State transition” for Internal clock frequency setting / Setting of the power domain / Regulator setting.

Relationship between the oscillation clock frequency and internal clock frequency

Oscillation Clock Frequency	Main Clock	PLL Multiplier Setting	PLL Output Division Setting	PLL Clock
4 MHz	4 MHz	144	4	144 MHz
4 MHz	4 MHz	144	6	96 MHz

- Oscillation circuit example



Note:
- When configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.
- The maximum PLL clock frequency must be 144MHz.
  Output division configuration can be set by the following.
  - PLLDIVM bit in SYSC0_RUNPLL0CNTR register
  - PLLDIVM bit in SYSC0_PSSPLL0CNTR register
  - SSCGDIVM bit in SYSC0_RUNSSCG0CNTR0 register
  - SSCGDIVM bit in SYSC0_PSSSSCG0CNTR0 register

  (e.g. If PLLout is 576MHz, these settings must be configured as "multiply by 4" and over multiplication setting)

(5-1-3) SPI Compatible (SCR:SPI=1) and Serial Clock Output Signal Detect Level "H" (SMR:SCINV=0)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK21	Master mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	$4t_{CLK\_LCP0A}$	-	ns	
SCK ↑ →SOT delay time	t_{SHOVI}	SCK0 to SCK21, SOT0 to SOT21		-30	+30	ns	
Valid SIN→SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK21, SIN0 to SIN21		30	-	ns	
SCK ↓ →valid SIN hold time	t_{SLIXI}			0	-	ns	
SOT→SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK21, SOT0 to SOT21		$2t_{CLK\_LCP0A}$ -30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK21	Slave mode (CL=50pF, I_{OL}=-2mA, I_{OH}=2mA), (CL=20pF, I_{OL}=-1mA, I_{OH}=1mA)	t_{CLK_LCP0A} +10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_LCP0A}$ -10	-	ns	
SCK ↑ →SOT delay time	t_{SHOVE}	SCK0 to SCK21, SOT0 to SOT21		-	45	ns	
Valid SIN→SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK21, SIN0 to SIN21		10	-	ns	
SCK ↓ →valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK falling time	t_F	SCK0 to SCK21		-	5	ns	
SCK rising time	t_R	SCK0 to SCK21		-	5	ns	

Notes:

- *This is the AC characteristic in CLK synchronized mode.*
- *CL is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*

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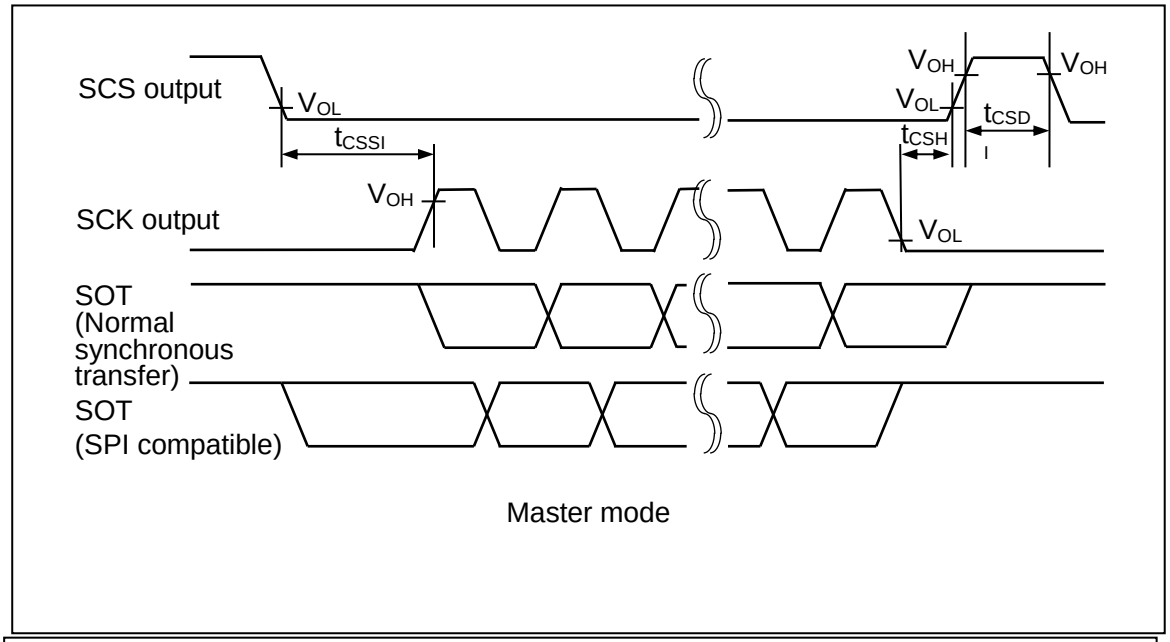
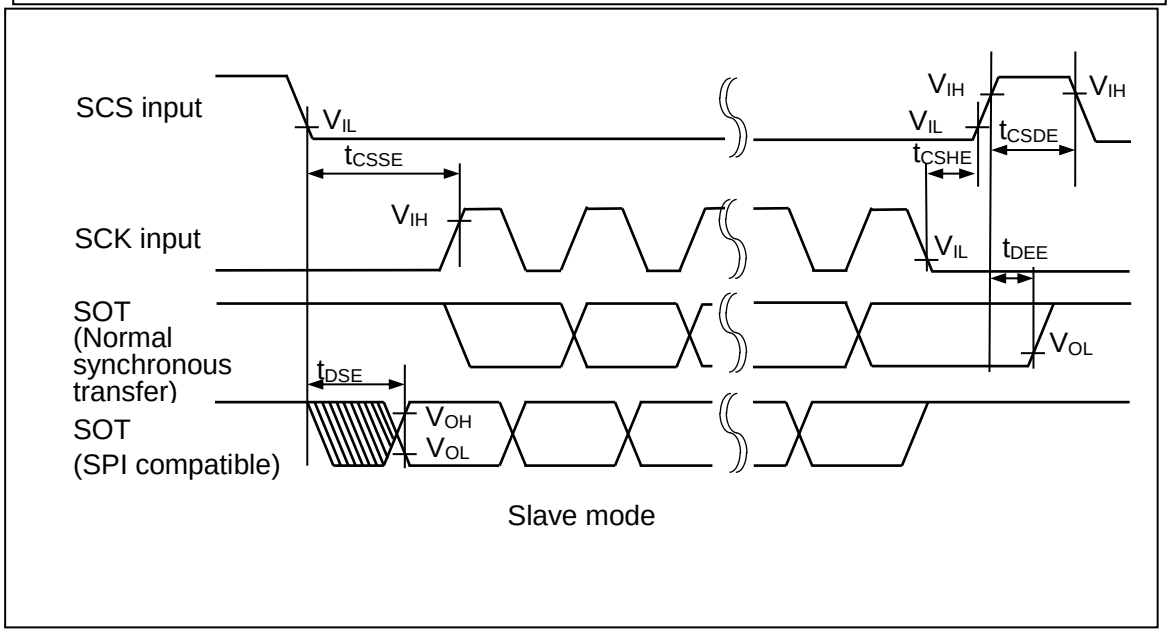
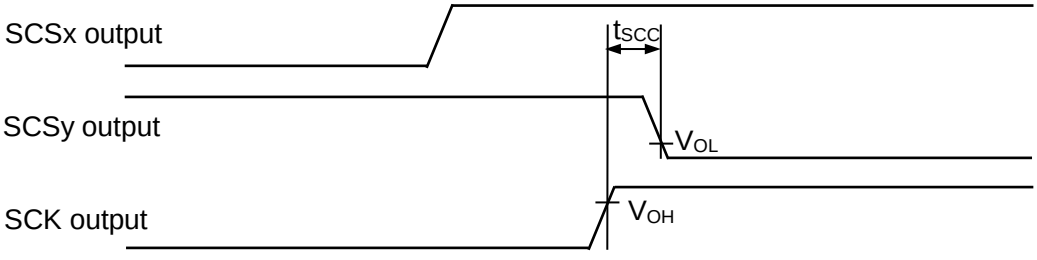






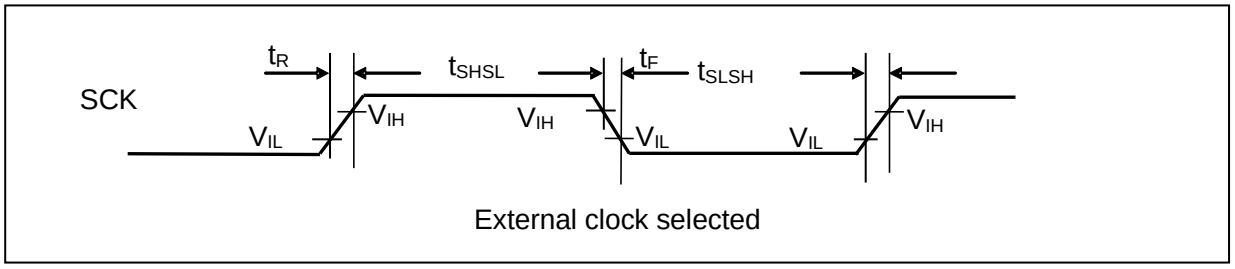
Clock switching example by master mode round operation
(x,y=0,1,2,3: x and y are different value)

10.4.5.2 UART (Async Serial Interface) timing (SMR:MD[2:0]=000B, 001B)

(5-2-1) External Clock Selected (BGR:EXT=1)

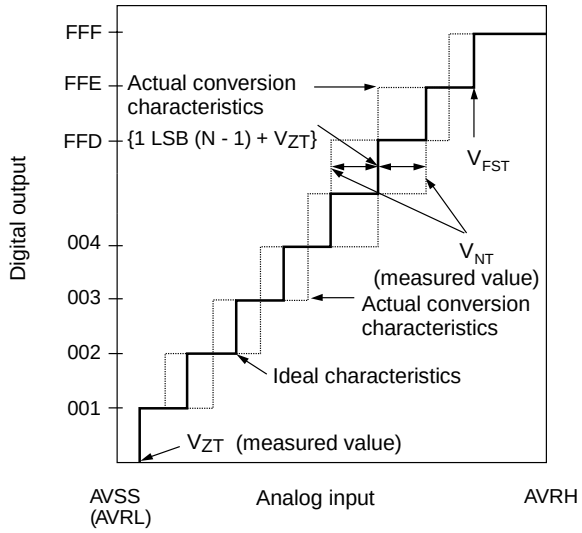
(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, VSS=AVSS=0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Ma		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK21	(CL=50pF, IOL=-2mA, IOH=2mA), (CL=20pF, IOL=-1mA, IOH=1mA)	t_{CLK_LCP0A} +10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CLK_LCP0A} +10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	

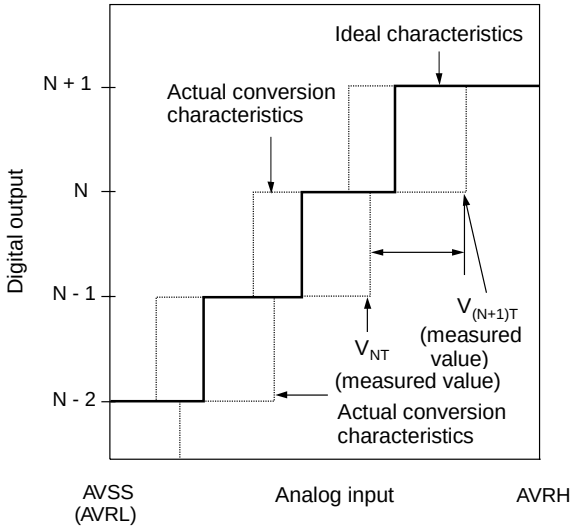


External clock selected

Integral Nonlinearity error



Differential Nonlinearity error



$$\text{Integral Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{ZT}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$\text{Differential Nonlinearity error of digital output N} = \frac{V_{(N+1)}\,T - V_{NT}}{1\text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}\ [\text{V}]$$

V_{ZT}: Voltage for which digital output changes from "0x000" to "0x001"

V_{FST}: Voltage for which digital output changes from "0xFFE" to "0xFFF".

10.12 Flash Memory

Parameter	Rating			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	300	1100	ms	8-KB sector[*1] Internal preprogramming time included
	-	800	3700	ms	64-KB sector[*1] Internal preprogramming time included
8-bit write time	-	15	288	µs	System-level overhead time excluded[*1]
16-bit write time	-	19	384	µs	System-level overhead time excluded[*1]
32-bit write time	-	27	567	µs	System-level overhead time excluded[*1]
64-bit write time	-	45	945	µs	System-level overhead time excluded[*1]
8-bit (with ECC) write time	-	19	384	µs	System-level overhead time excluded[*1]
16-bit (with ECC) write time	-	23	483	µs	System-level overhead time excluded[*1]
32-bit (with ECC) write time	-	31	651	µs	System-level overhead time excluded[*1]
64-bit (with ECC) write time	-	49	1029	µs	System-level overhead time excluded[*1]
Erase count[*2]/ Data retention time	1,000/20 years, 10,000/10 years, 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T_A=+85 degrees Celsius

*1: Guaranteed value for up to 100,000 erases

*2: Number of erases for each sector

Notes:

- *While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.*
- *In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.*
- *To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}), hold Vcc at 2.7V or more within the duration calculated by the following expression:*

  Td^{*1} [µs] + (1 / F_{CRF}^{*2}[MHz]) x 1029 + 25 [µs]

  **1: See "12.8 Low-voltage detection (external low-voltage detection) "*

  **2: See "12.4.1 Source clock timing"*

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>55</td><td>10. Electrical Characteristics
10.1 Absolute Maximum Ratings</td><td>The notes should be corrected as indicated by the shading below.
(Error)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>Power supply voltage*1, *2</td><td>V_{CC}</td><td>V_{SS}-0.3</td><td>V_{SS}+6.0</td><td>V</td><td></td></tr>
<tr><td>Analog supply voltage*1, *2</td><td>AV_{CC}</td><td>V_{SS}-0.3</td><td>V_{SS}+6.0</td><td>V</td><td>Avcc≤Vcc</td></tr>
</table>
(Correct)
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
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</table></td></tr>
<tr><td>55</td><td>10. Electrical Characteristics
10.1 Absolute Maximum Ratings</td><td>Revised the following note

*2: AVCC and VCC must be set to the same voltage. It is required that AVCC does not exceed VCC and that the voltage at the analog inputs does not exceed AVCC when the power is switched on.</td></tr>
<tr><td>57</td><td>10. Electrical Characteristics
10.2 Recommended operating conditions</td><td>Separated the specification of smoothing capacitor from C_{S1}, C_{S2} to C_S
Revised the figure and table</td></tr>
<tr><td>57</td><td>10. Electrical Characteristics
10.2 Recommended operating conditions</td><td>Added the following remarks to “Smoothing capacitor”

Use a ceramic capacitor or a capacitor that has the similar frequency characteristics.
Use a capacitor with a capacitance greater than CS as the smoothing capacitor on the VCC pin.</td></tr>
<tr><td>57</td><td>10. Electrical Characteristics
10.2 Recommended operating conditions</td><td>Revised the notes of “C pin connection diagram” as follow:
1: 154pin(S6J311xJzC) / 126pin(S6J311xHzC*)
2: 46pin(S6J311xJzC) / 38pin(S6J311xHzC*)
* x: E/D/C/B, z: A/B</td></tr>
<tr><td>57</td><td>10. Electrical Characteristics
10.2 Recommended operating conditions</td><td>Revised the connection of C pin in “C pin connection diagram”</td></tr>
<tr><td>58</td><td>10. Electrical Characteristics
10.2 Recommended operating conditions</td><td>Added the following notes

-The following condition should be satisfied in order to facilitate heat dissipation.
1.4 or more layers PCB should be used.
2.The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)
3.1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.
4.35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.
5.The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.</td></tr>
<tr><td>58</td><td>10. Electrical Characteristics
10.2 Recommended operating conditions</td><td>Added the following notes

−Figure 2-1 is a schematic diagram showing PCB in section.
−Figure 2-2, Figure 2-3 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands.
−If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.</td></tr>
</table>