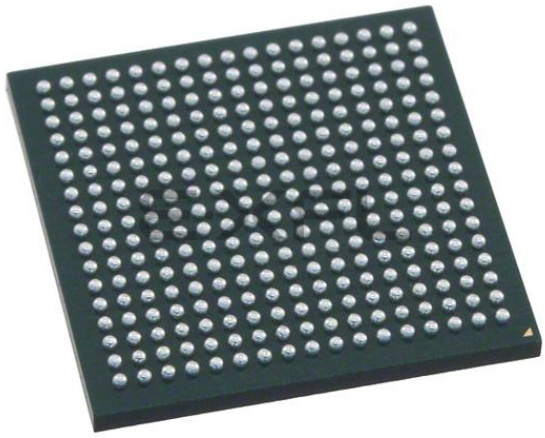


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; C3
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (5)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	Cryptography
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spear310-2

List of tables

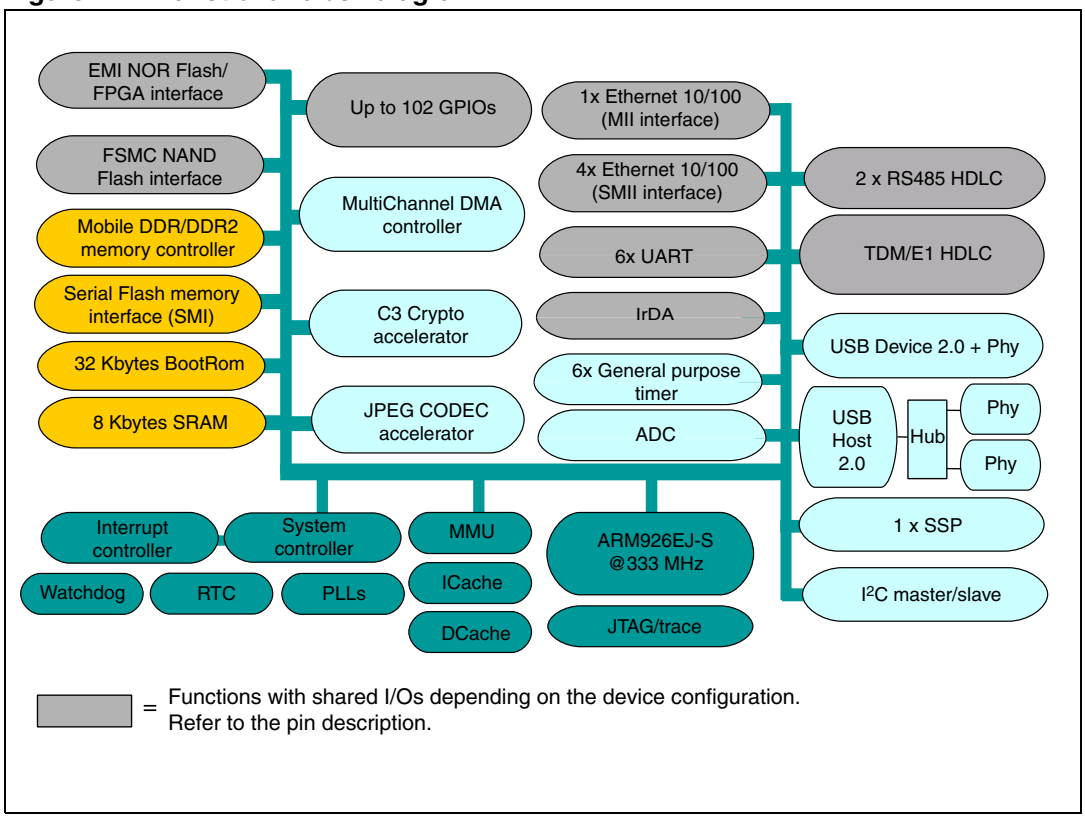
1 Description

The SPEAr310 is a member of the SPEAr family of embedded MPUs, optimized for telecom applications. It is based on the powerful ARM926EJ-S processor (up to 333 MHz), widely used in applications where high computation performance is required.

In addition, SPEAr310 has an MMU that allows virtual memory management -- making the system compliant with advanced operating systems, like Linux. It also offers 16 KB of data cache, 16 KB of instruction cache, JTAG and ETM (embedded trace macro-cell) for debug operations.

A full set of peripherals allows the system to be used in many applications, some typical applications being routers, switches and gateways as well as remote apparatus control and metering concentrators.

Figure 1. Functional block diagram



  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller
  - 3 pairs of 16-bits general purpose timers with programmable prescaler
  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration
- Programmable PLL for CPU and system clocks
- JTAG IEEE 1149.1
- Boundary scan
- ETM functionality multiplexed on primary pins
- Supply voltages
  - 1.2 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs, 1.5 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- LFBGA289 (15 x 15 mm, pitch 0.8 mm)

Main features:

- 8/16-bit wide data path
- FSMC performs only one access at a time and only one external device is accessed.
- Supports little-endian and big-endian memory architectures.
- AHB burst transfer handling to reduce access time to external devices.
- Supplies an independent configuration for each memory bank.
- Programmable timings to support a wide range of devices.
  - Programmable wait states (up to 31).
  - Programmable bus turnaround cycles (up to 15).
  - Programmable output enable and write enable delays (up to 15).
- Independent chip select control for each memory bank.
- Shares the address bus and the data bus with all the external peripherals.
- Only chips selects are unique for each peripheral.
- External asynchronous wait control.

2.9 UARTs

The SPEAr310 has 5 UARTs featuring software flow control and 1 UART featuring hardware and/or software flow control.

2.9.1 UART with hardware flow control

Main features:

- Separate 16 x 8 (16 locations deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 3 Mbps
- Hardware and/or software flow control

2.9.2 UARTs with software flow control

Main features:

- Separate 16 x 8 (16 location deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 5 Mbps.

Each Ethernet port provides the following features:

- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full and half duplex operation
- Statistics counter registers for RMON/MIB
- Interrupt generation to signal receive and transmit completion
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Supports promiscuous mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- External address matching of received frames
- Physical layer management through MDIO interface
- Supports serial network interface operation
- Half duplex flow control by forcing collisions on incoming frames
- Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Wake on LAN support
- Jumbo frames of up to 10240 bytes supported
- Configurable Endianess for the DMA Interface (AHB Master)

2.17 MII Ethernet controller

SPEAr310 provides an Ethernet MAC 10/100 Universal (commonly referred to as GMAC-UNIV), enabling to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard.

Note: GMAC is a hardware block implementing Ethernet MAC layer 2 processing. GMAC is configured for 10/100 Mbps operation on SPEAr3xx family and up to 1 Gbps on SPEAr600.

2.19 USB2 device controller

Main features:

- Supports the 480 Mbps high-speed mode (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the 1.5 Mbps low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints, configurable as different logical endpoints
- Integrated USB transceiver (PHY)
- Local 4 Kbyte FIFO shared among all the endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug (UPD) detects the connection of a cable.

2.20 Cryptographic co-processor (C3)

SPEAr310 has an embedded Channel Control Coprocessor (C3). C3 is a high-performance instruction driven DMA based co-processor. It executes instruction flows generated by the host processor. After it has been set-up by the host it runs in a completely autonomous way (DMA data in, data processing, DMA data out), until the completion of all the requested operations.

C3 has been used to accelerate the processing of cryptographic, security and network security applications. It can be used for other types of data intensive applications as well.

Hardware cryptographic co-processor features are listed below:

- Supported cryptographic algorithms:
  - Advanced encryption standard (AES) cipher in ECB, CBC, CTR modes.
  - Data encryption standard (DES) cipher in ECB and CBC modes.
  - SHA-1, HMAC-SHA-1, MD5, HMAC-MD5 digests.
- Instruction driven DMA based programmable engine.
- AHB master port for data access from/to system memory.
- AHB slave port for co-processor register accesses and initial engine-setup.
- The co-processor is fully autonomous (DMA input reading, cryptographic operation execution, DMA output writing) after being set up by the host processor.
- The co-processor executes programs written by the host in memory, it can execute an unlimited list of programs.
- The co-processor supports hardware chaining of cryptographic blocks for optimized execution of data-flow requiring multiple algorithms processing over the same set of data (for example encryption + hashing on the fly).

Table 4. Debug pin descriptions

Group	Signal name	Ball	Direction	Function	Pin type
DEBUG	TEST_0	K16	Input	Test_[4:0] configuration ports. For functional mode, they have to be set to 00110.	TTL input buffer, 3.3 V tolerant, PD
	TEST_1	K15			
	TEST_2	K14			
	TEST_3	K13			
	TEST_4	J15			
	BOOT_SEL	J14		Reserved, to be fixed at high level	
	nTRST	L16	Input	Test reset input	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
	TDO	L15	Output	Test data output	TTL output buffer, 3.3 V capable 4 mA
	TCK	L17	Input	Test clock	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
	TDI	L14	Input	Test data input	
	TMS	L13	Input	Test mode select	

Table 5. Serial memory interface (SMI) pin description

Group	Signal name	Ball	Direction	Function	Pin type
SMI	SMI_DATAIN	M13	Input	Serial Flash input data	TTL Input Buffer 3.3 V tolerant, PU
	SMI_DATAOUT	M14	Output	Serial Flash output data	TTL output buffer 3.3 V capable 4 mA
	SMI_CLK	N17	I/O	Serial Flash clock	
	SMI_CS_0	M15	Output	Serial Flash chip select	
	SMI_CS_1	M16			

Table 6. USB pin descriptions

Group	Signal name	Ball	Direction	Function	Pin type
USB DEV	USB_DEVICE_DP	M1	I/O	USB Device D+	Bidirectional analog buffer 5 V tolerant
	USB_DEVICE_DM	M2		USB Device D-	
	USB_DEVICE_VBUS	G3	Input	USB Device VBUS	TTL input buffer 3.3 V tolerant, PD

Table 6. USB pin descriptions (continued)

Group	Signal name	Ball	Direction	Function	Pin type
USB HOST	USB_HOST1_DP	H1	I/O	USB HOST1 D+	Bidirectional analog buffer 5 V tolerant
	USB_HOST1_DM	H2		USB HOST1 D-	
	USB_HOST1_VBUS	H3	Output	USBHOST1 VBUS	TTL output buffer 3.3 V capable, 4 mA
	USB_HOST1_OVERCUR	J4	Input	USB Host1 Over-Current	TTL input buffer 3.3 V tolerant, PD
	USB_HOST0_DP	K1	I/O	USB HOST0 D+	Bidirectional analog buffer 5 V tolerant
	USB_HOST0_DM	K2		USB HOST0 D-	
	USB_HOST0_VBUS	J3	Output	USB HOST0 VBUS	TTL output buffer 3.3 V capable, 4 mA
	USB_HOST0_OVERCUR	H4	Input	USB Host0 Over-current	TTL Input Buffer 3.3 V tolerant, PD
USB	USB_TXRTUNE	K5	Output	Reference resistor	Analog
	USB_ANALOG_TEST	L4	Output	Analog Test Output	Analog

Table 7. ADC pin description

Group	Signal name	Ball	Direction	Function	Pin type
ADC	AIN_0	N16	Input	ADC analog input channel	Analog buffer 2.5 V tolerant
	AIN_1	N15			
	AIN_2	P17			
	AIN_3	P16			
	AIN_4	P15			
	AIN_5	R17			
	AIN_6	R16			
	AIN_7	R15			
	ADC_VREFN	N14		ADC negative voltage reference	
	ADC_VREFP	P14		ADC positive voltage reference	

3.3 Shared I/O pins (PL_GPIOs)

SPEAr3xx devices feature, in the Reconfigurable Array Subsystem (RAS), specific sets of IPs as well as groups of software controllable GPIOs (that can be used alternatively). In the SPEAr310 the following IPs are implemented in the RAS:

- External Memory Interface for external NOR Flash or other devices such as FPGAs
- FSMC NAND Flash interface
- TDM/E1 HDLC interface
- 2 RS485 ports
- 4 SMII interfaces for customized Ethernet MACs

The 98 PL_GPIO and 4 PL_CLK pins have the following characteristics:

- Output buffer: TTL 3.3 V capable up to 10 mA
- Input buffer: TTL, 3.3 V tolerant, selectable internal pull up/pull down (PU/PD)

3.3.1 PL_GPIO pin description

Table 9. PL_GPIO pin description

Group	Signal name	Ball	Direction	Function	Pin type
PL_GPIOs	PL_GPIO_97... PL_GPIO_0	(see the section *Table 10*)	I/O	General purpose I/O or multiplexed pins (see the section *Table 10*)	(see the introduction of the *Section 3.3* here above)
	PL_CLK1... PL_CLK4			programmable logic external clocks	

3.3.2 Configuration modes

RAS normal or RAS GPIO mode is selected by programming the RAS control registers. Details of each PL_GPIO pin are given in *Table 10: PL_GPIO multiplexing scheme on page 34*

RAS normal mode is the default mode for SPEAr310. It mainly provides:

- External Memory Interface (16 data bits, 24 address bits and 4 chip selects)
- FSMC NAND Flash interface (8-16 bits and 3 control lines shared with EMI)
- TDM/E1 HDLC interface
- 2 RS485 ports
- 4 SMII interfaces for customized Ethernet MACs,
- 6 UARTs, 1 with hardware flow control (up to 3 Mbps), 5 with software flow control (baud rate up to 5 Mbps)
- SSP port
- 1 independent I2C interface
- GPIOs with interrupt capabilities

Figure 5. Hierarchical multiplexing scheme

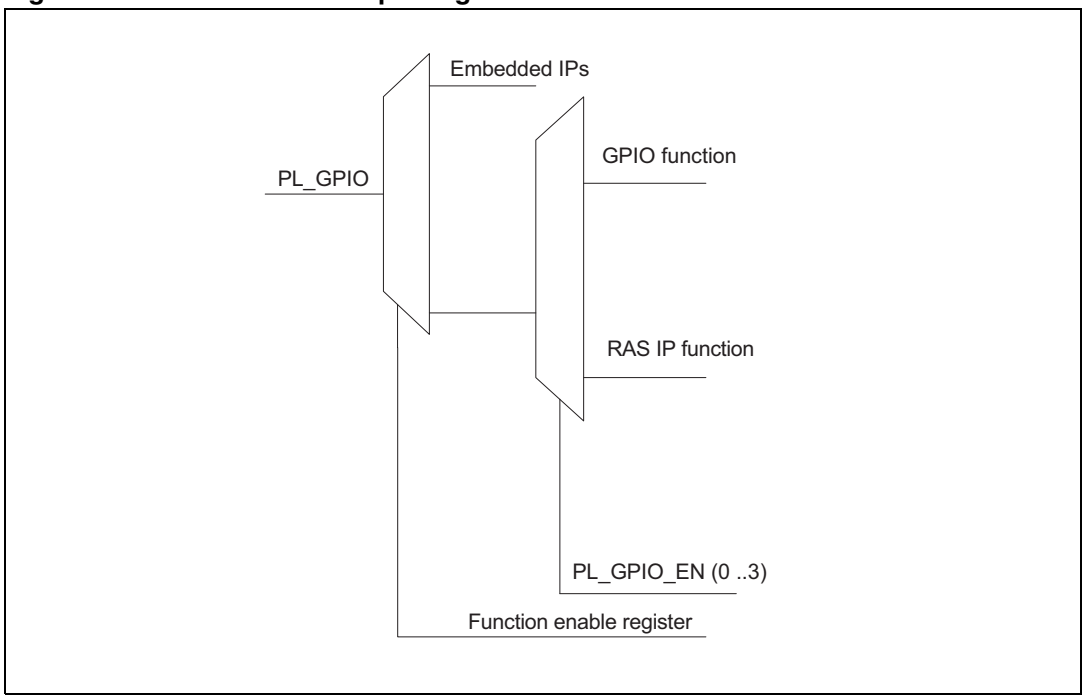


Table 10. PL_GPIO multiplexing scheme

PL / pin number	Function in RAS normal mode	Alternate function (enabled by Function Enable register)	Boot pins	Function in RAS GPIO mode
PL_GPIO_97/H16	ETH0_TX			GPIO12_7
PL_GPIO_96/H15	ETH0_RX			GPIO12_6
PL_GPIO_95/H14	ETH1_TX			GPIO12_5
PL_GPIO_94/H13	ETH1_RX			GPIO12_4
PL_GPIO_93/G17	ETH2_TX			GPIO12_3
PL_GPIO_92/G16	ETH2_RX			GPIO12_2
PL_GPIO_91/G15	ETH3_TX			GPIO12_1
PL_GPIO_90/G14	ETH3_RX			GPIO12_0
PL_GPIO_89/F17	ETH_SYNC			GPIO11_7
PL_GPIO_88/F16	SMII_MDIO			GPIO11_6
PL_GPIO_87/G13	SMII_MDC			GPIO11_5
PL_GPIO_86/E17	EMI_ADDB_0/FSMC_D0		B0	GPIO11_4
PL_GPIO_85/F15	EMI_ADDB_1/FSMC_D1		B1	GPIO11_3
PL_GPIO_84/D17	EMI_ADDB_2/FSMC_D2		B2	GPIO11_2
PL_GPIO_83/E16	EMI_ADDB_3/FSMC_D3		B3	GPIO11_1
PL_GPIO_82/E15	EMI_ADDB_4/FSMC_D4		B4	GPIO11_0
PL_GPIO_81/C17	EMI_ADDB_5/FSMC_D5		B5	GPIO10_7
PL_GPIO_80/D16	EMI_ADDB_6/FSMC_D6		B6	GPIO10_6

Table 10. PL_GPIO multiplexing scheme (continued)

PL / pin number	Function in RAS normal mode	Alternate function (enabled by Function Enable register)	Boot pins	Function in RAS GPIO mode
PL_GPIO_79/F14	EMI_ADDB_7/FSMC_D7			GPIO10_5
PL_GPIO_78/D15	EMI_ADDB_8/FSMC_D8			GPIO10_4
PL_GPIO_77/B17	EMI_ADDB_9/FSMC_D9			GPIO10_3
PL_GPIO_76/F13	EMI_ADDB_10/FSMC_D10			GPIO10_2
PL_GPIO_75/E14	EMI_ADDB_11/FSMC_D11			GPIO10_1
PL_GPIO_74/C16	EMI_ACK			GPIO10_0
PL_GPIO_73/A17	EMI_ADDB_13/FSMC_D13			GPIO9_7
PL_GPIO_72/B16	EMI_ADDB_14/FSMC_D14			GPIO9_6
PL_GPIO_71/D14	EMI_ADDB_15/FSMC_D15			GPIO9_5
PL_GPIO_70/C15	EMI_ADDB_16			GPIO9_4
PL_GPIO_69/A16	EMI_ADDB_17			GPIO9_3
PL_GPIO_68/B15	EMI_ADDB_18			GPIO9_2
PL_GPIO_67/C14	EMI_ADDB_19			GPIO9_1
PL_GPIO_66/E13	EMI_ADDB_20			GPIO9_0
PL_GPIO_65/B14	EMI_ADDB_21			GPIO8_7
PL_GPIO_64/D13	EMI_ADDLE/FSMC_AL			GPIO8_6
PL_GPIO_63/C13	EMI_ADDB_23			GPIO8_5
PL_GPIO_62/A15	EMI_ADDB_24			GPIO8_4
PL_GPIO_61/E12	EMI_ADDB_25			GPIO8_3
PL_GPIO_60/A14	EMI_ADDB_26			GPIO8_2
PL_GPIO_59/B13	EMI_ADDB_27			GPIO8_1
PL_GPIO_58/D12	EMI_ADDB_28			GPIO8_0
PL_GPIO_57/E11	EMI_ADDB_29			GPIO7_7
PL_GPIO_56/C12	EMI_ADDB_30			GPIO7_6
PL_GPIO_55/A13	EMI_ADDB_31			GPIO7_5
PL_GPIO_54/E10	EMI_ADDB_12/FSMC_D12			GPIO7_4
PL_GPIO_53/D11	EMI_ADDB_22			GPIO7_3
PL_GPIO_52/B12	EMI_OE/FSMC_/R			GPIO7_2
PL_GPIO_51/D10	EMI_WE/FSMC_/W			GPIO7_1
PL_GPIO_50/A12	EMI_CS[0]	TMR_CPTR4		GPIO7_0
PL_GPIO_49/C11	EMI_CS[1]	TMR_CPTR3		GPIO6_7
PL_GPIO_48/B11	EMI_CS[2]	TMR_CPTR2		GPIO6_6
PL_GPIO_47/C10	EMI_CS[3]	TMR_CPTR1		GPIO6_5
PL_GPIO_46/A11	EMI_CS[4]	TMR_CLK4		GPIO6_4
PL_GPIO_45/B10	EMI_CS[5]	TMR_CLK3		GPIO6_3
PL_GPIO_44/A10	UART2_TX	TMR_CLK2		GPIO6_2
PL_GPIO_43/E9	UART2_RX	TMR_CLK1		GPIO6_1

1. Case 1 - All the PL_GPIO get values from Boundary scan registers during Ex-test instruction of JTAG . Typically this configuration is used to verify correctness of the soldering process during the production flow .
2. Case 2 - All the PL_GPIO maintain their original meaning but the JTAG Interface is connected to the processor. This configuration is useful during the development phase but offers only "static" debug.
3. Case 3 - Some PL_GPIO, as shown in *Table 12: Ball sharing during debug*, are used to connect the ETM9 lines to an external box. This configuration is typically used only during the development phase. It offers a very powerful debug capability. When the processor reaches a breakpoint it is possible, by analyzing the trace buffer, to understand the reason why the processor has reached the break.

Table 12. Ball sharing during debug

Signal	Case 1 - Board Debug	Case 2 - Static Debug	Case 3 - Full Debug
Test[0]	0	1	0
Test[1]	0	0	1
Test[2]	0	0/1	0/1
Test[3]	0	0/1	0/1
Test[4]	1	0	0
nTRST	nTRST_bscan	nTRST_ARM	nTRST_ARM
TCK	TCK_bscan	TCK_ARM	TCK_ARM
TMS	TSM_bscan	TMS_ARM	TSM_ARM
TDI	TDI_bscan	TDI_ARM	TDI_ARM
TDO	TDO_bscan	TDO_ARM	TDO_ARM
PL_GPIO[97]	BSR Value	Functional I/O	ARM_TRACE_CLK
PL_GPIO[96]	BSR Value	Functional I/O	ARM_TRACE_PKTA[0]
PL_GPIO[95]	BSR Value	Functional I/O	ARM_TRACE_PKTA[1]
PL_GPIO[94]	BSR Value	Functional I/O	ARM_TRACE_PKTA[2]
PL_GPIO[93]	BSR Value	Functional I/O	ARM_TRACE_PKTA[3]
PL_GPIO[92]	BSR Value	Functional I/O	ARM_TRACE_PKTB[0]
PL_GPIO[91]	BSR Value	Functional I/O	ARM_TRACE_PKTB[1]
PL_GPIO[90]	BSR Value	Functional I/O	ARM_TRACE_PKTB[2]
PL_GPIO[89]	BSR Value	Functional I/O	ARM_TRACE_PKTB[3]
PL_GPIO[88]	BSR Value	Functional I/O	ARM_TRACE_SYNCA
PL_GPIO[87]	BSR Value	Functional I/O	ARM_TRACE_SYNCB
PL_GPIO[86]	BSR Value	Functional I/O	ARM_PIPESTATA[0]
PL_GPIO[85]	BSR Value	Functional I/O	ARM_PIPESTATA[1]
PL_GPIO[84]	BSR Value	Functional I/O	ARM_PIPESTATA[2]
PL_GPIO[83]	BSR Value	Functional I/O	ARM_PIPESTATB[0]
PL_GPIO[82]	BSR Value	Functional I/O	ARM_PIPESTATB[1]

4 Memory map

Table 13. SPEAr310 memory mapping

Start address	End address	Peripheral	Description
0x0000_0000	0x3FFF_FFFF	LP DDR/DDR2 external memory	
0x4000_0000	0x43FF_FFFF	FSMC	External NAND Flash memory
0x4400_0000	0x44FF_FFFF		FSMC configuration registers
0x4500_0000	0x4EFF_FFFF	Reserved	
0x4F00_0000	0x4FFF_FFFF	EMI	EMI configuration registers
0x5000_0000	0x5FFF_FFFF		256 MB Ext. memory EMI CS[0]/NOR_CS[0]
0x6000_0000	0x6FFF_FFFF		256 MB Ext. memory EMI CS[1]
0x7000_0000	0x7FFF_FFFF		256 MB Ext. memory EMI CS[2]
0x8000_0000	0x8FFF_FFFF		256 MB Ext. memory EMI CS[3]
0x9000_0000	0x9FFF_FFFF		256 MB Ext. memory EMI CS[4]
0xA000_0000	0xAFFF_FFFF		256 MB Ext. memory EMI CS[5]
0xB000_0000	0xB07F_FFFF	MACB 0 (SMII)	MACB configuration registers
0xB080_0000	0xB0FF_FFFF	MACB 1 (SMII)	MACB configuration registers
0xB100_0000	0xB17F_FFFF	MACB 2 (SMII)	MACB configuration registers
0xB180_0000	0xB1FF_FFFF	MACB 3 (SMII)	MACB configuration registers
0xB200_0000	0xB207_FFFF	UART 1	UART configuration registers
0xB208_0000	0xB20F_FFFF	UART 2	UART configuration registers
0xB210_0000	0xB217_FFFF	UART 3	UART configuration registers
0xB218_0000	0xB21F_FFFF	UART 4	UART configuration registers
0xB220_0000	0xB227_FFFF	UART 5	UART configuration registers
0xB228_0000	0xB27F_FFFF	Reserved	
0xB280_0000	0xB2FF_FFFF	TDM/E1 HDLC	TDM/E1 HDLC configuration registers
0xB300_0000	0xB37F_FFFF	RS485 HDLC 1	RS485 HDLC 1 configuration registers
0xB380_0000	0xB3FF_FFFF	RS485 HDLC 2	RS485 HDLC 2 configuration registers
0xB400_0000	0xB47F_FFFF	RAS	RAS configuration registers
0xB480_0000	0xCFFF_FFFF	Reserved	
0xD000_0000	0xD007_FFFF	UART 0	UART configuration registers
0xD008_0000	0xD00F_FFFF	ADC	ADC configuration registers
0xD010_0000	0xD017_FFFF	SSP	SSP configuration registers

Table 13. SPEAr310 memory mapping (continued)

Start address	End address	Peripheral	Description
0xFC98_0000	0xFC9F_FFFF	General Purpose I/O	GPIO configuration registers
0xFCA0_0000	0xFCA7_FFFF	System Controller	SYS Ctrl configuration registers
0xFCA8_0000	0xFCAF_FFFF	MISC (Miscellaneous)	MISC configuration registers
0xFCB0_0000	0xFCB7_FFFF	Timer 3	GPT configuration registers
0xFCB8_0000	0xFEFF_FFFF	Reserved	
0xFF00_0000	0xFFFF_FFFF	Internal ROM	Boot ROM

6.1.3 DDR2 command timings

Figure 12. DDR2 Command waveforms

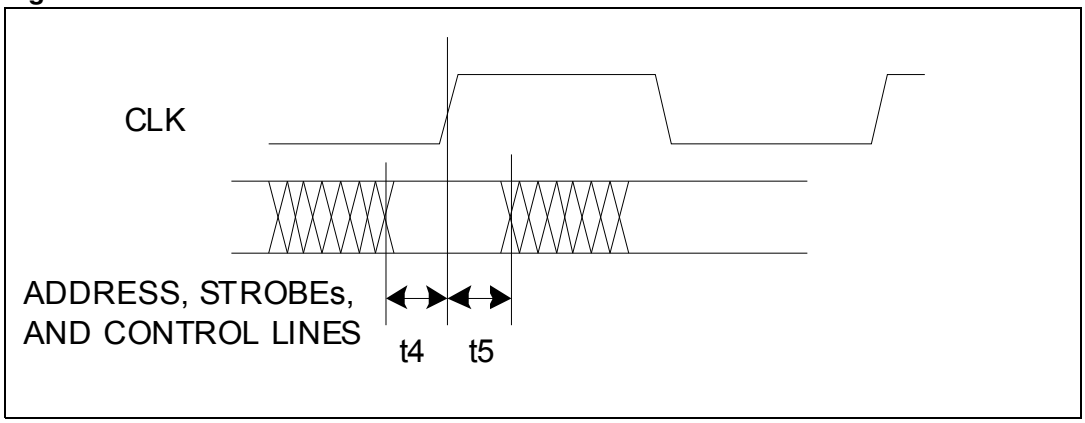


Figure 13. DDR2 Command path

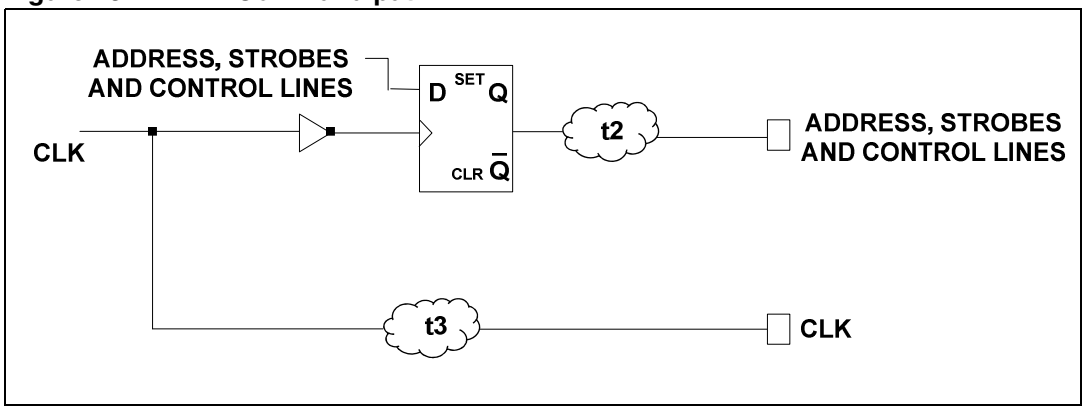


Table 27. DDR2 Command timings

Frequency	t4 max	t5 max	Unit
333 MHz	1.39	1.40	ns
266 MHz	1.77	1.78	ns
200 MHz	2.39	2.40	ns
166 MHz	2.90	2.91	ns
133 MHz	3.65	3.66	ns

6.2 I²C timing characteristics

The characterization timing is done considering an output load of 10 pF on SCL and SDA. The operating conditions are V = 0.90 V, T_A=125° C in worst case and V =1.10 V, T_A= 40° C in best case.

Figure 14. I²C output pins

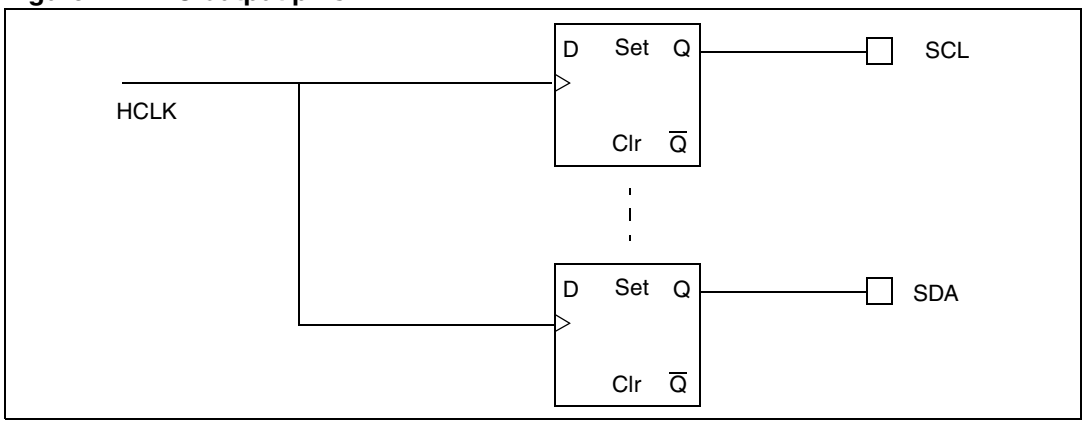
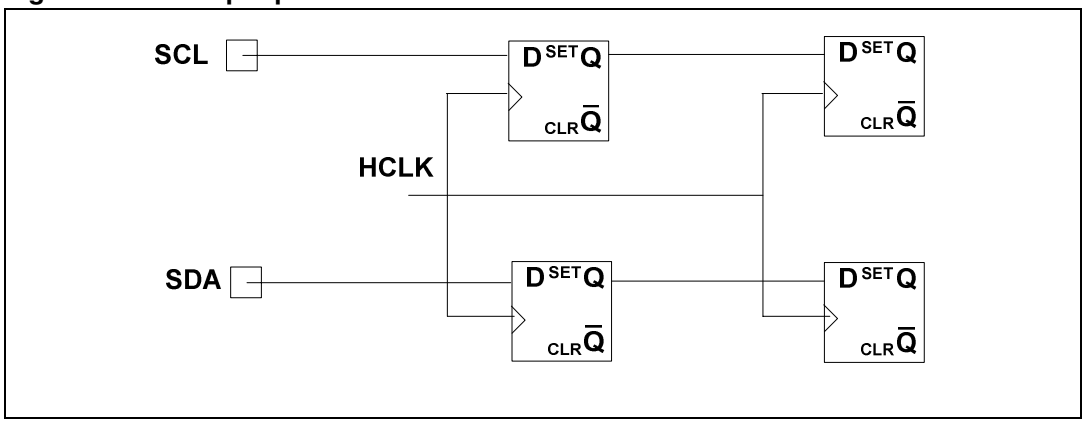


Figure 15. I²C input pins



The flip-flops used to capture the incoming signals are re-synchronized with the AHB clock (HCLK): so, no input delay calculation is required.

Table 28. Output delays for I²C signals

Parameter	Min	Max	Unit
$t_{HCLK->SCLH}$	8.1067	11.8184	ns
$t_{HCLK->SCLL}$	7.9874	12.6269	ns
$t_{HCLK->SDAH}$	7.5274	11.2453	ns
$t_{HCLK->SDAL}$	7.4081	12.0530	ns

Those values are referred to the common internal source clock which has a period of:

t_{HCLK} = 6 ns.

6.3.1 8-bit NAND Flash configuration

Figure 18. Output pads for 8-bit NAND Flash configuration

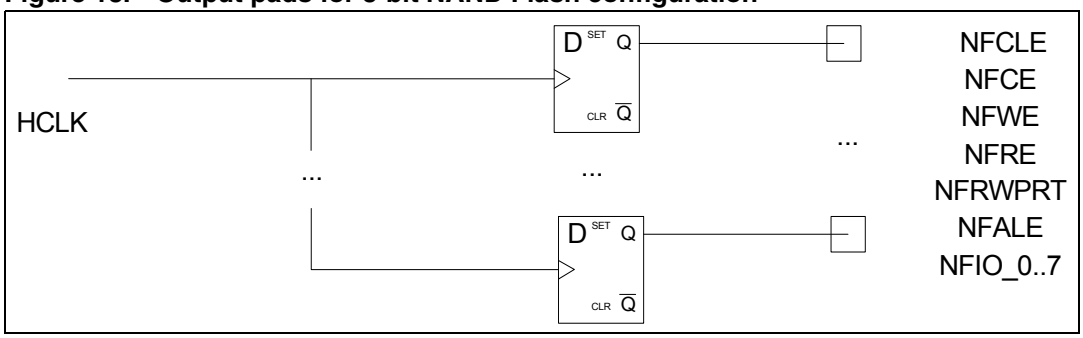


Figure 19. Input pads for 8-bit NAND Flash configuration

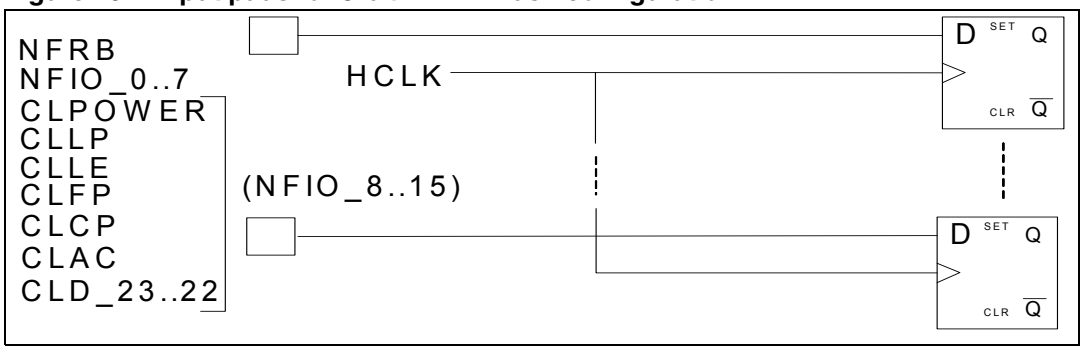
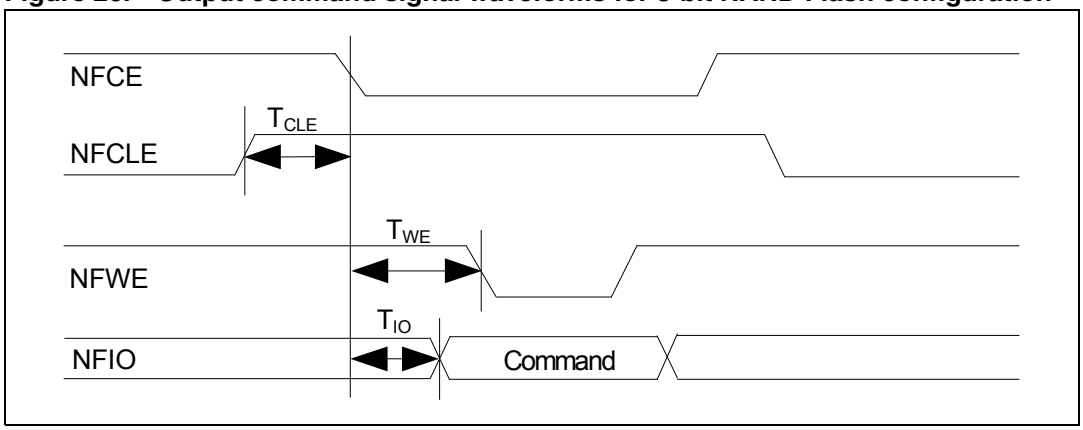


Figure 20. Output command signal waveforms for 8-bit NAND Flash configuration



6.5 SMI - Serial memory interface timing characteristics

Figure 34. SMI_DATAIN data path

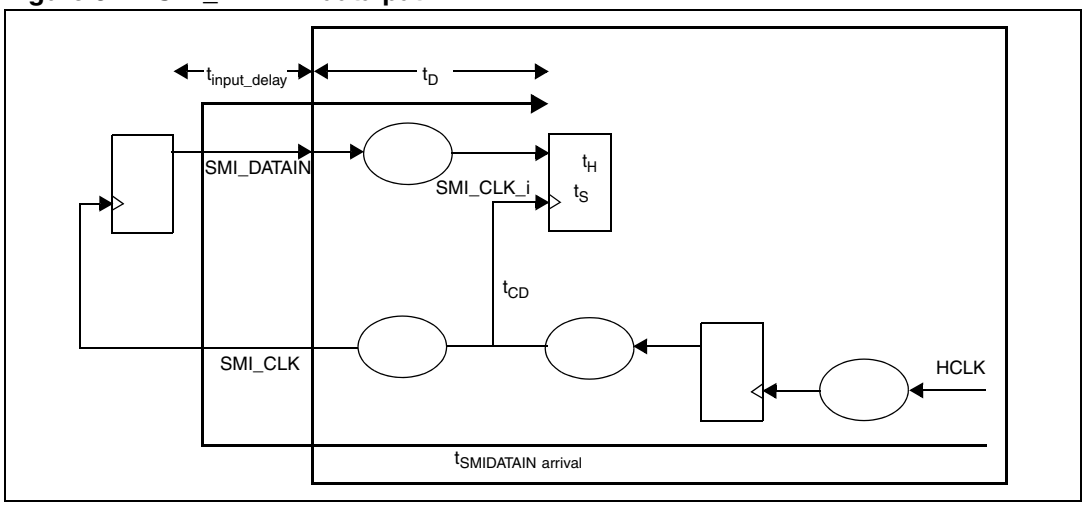


Table 36. SMI_DATAIN timings

Signal	Parameter	Value
SMI_DATAIN	t_{d_max}	$t_{SMIDATAIN\_arrival\_max} - t_{input\_delay}$
	t_{d_min}	$t_{SMIDATAIN\_arrival\_min} - t_{input\_delay}$
	t_{cd_min}	$t_{SMI\_CLK\_i\_arrival\_min}$
	t_{cd_max}	$t_{SMI\_CLK\_i\_arrival\_max}$
	t_{SETUP_max}	$t_s + t_{d\_max} - t_{cd\_min}$
	t_{HOLD_min}	$t_h - t_{d\_min} + t_{cd\_max}$

Figure 35. SMI_DATAOUT/SMI_CSn data paths

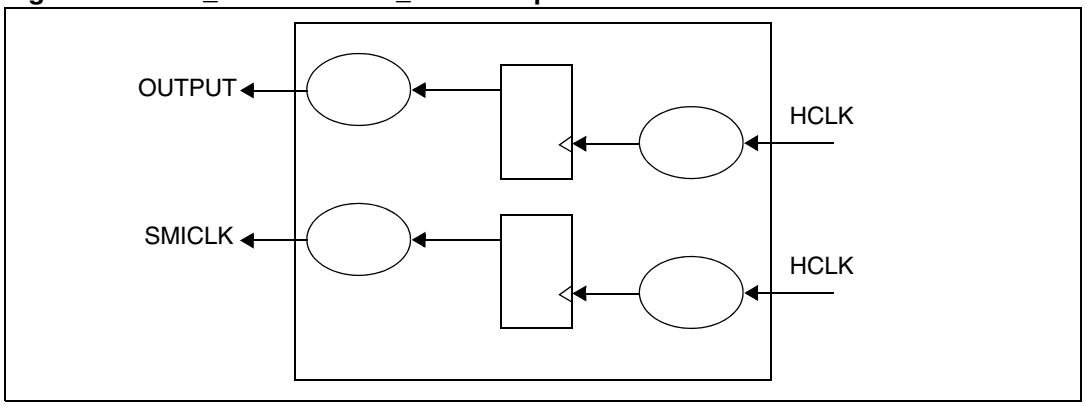
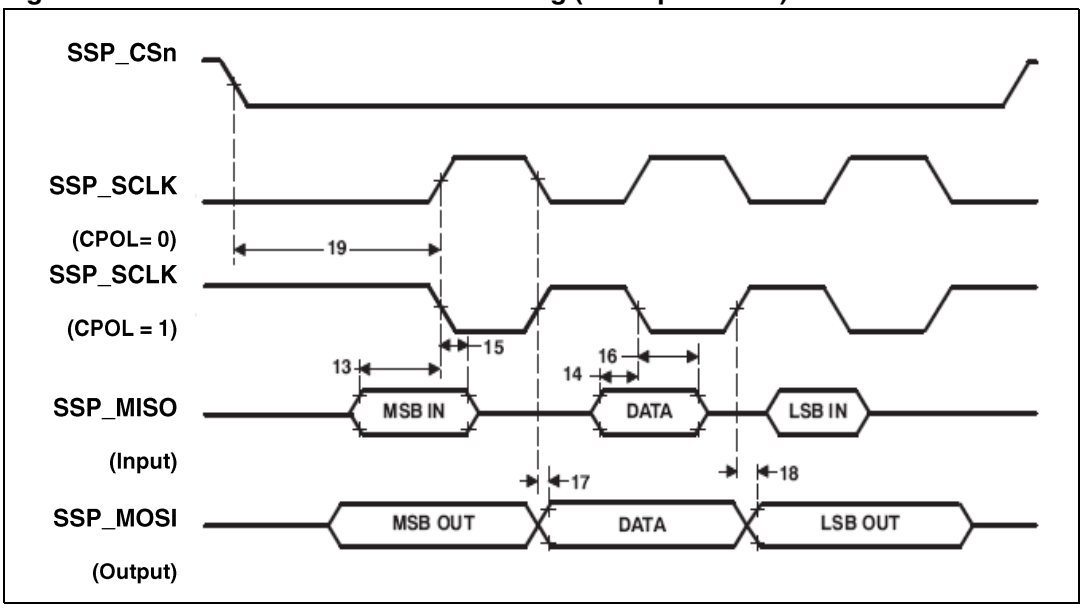


Figure 40. SPI master mode external timing (clock phase = 0)



6.6.2 SPI master mode timings (clock phase = 1)

Table 44. Timing requirements for SPI master mode (clock phase = 1)

No.	Parameters			Min	Max	Unit
4	$t_{su(DIV-CLKL)}$	Setup time, MISO (input) valid before SSP_CLK (output) falling edge	Clock polarity = 0	-0.411	-0.342	ns
5	$t_{su(DIV-CLKH)}$	Setup time, MISO (input) valid before SSP_CLK (output) rising edge	Clock polarity = 1	-0.411	-0.342	ns
6	$t_{h(CLKL-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) falling edge	Clock polarity = 0	0.912	1.720	ns
7	$t_{h(CLKH-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) rising edge	Clock polarity = 1	0.912	1.720	ns

Table 45. Switching characteristics over recommended operating conditions for SPI master mode (clock phase = 1)

No.	Parameters			Min	Max	Unit
8	$t_{d(CLKH-DOV)}$	Delay time, SSP_CLK (output) rising edge to MOSI (output) transition	Clock Polarity = 0	-3.138	2.175	ns
9	$t_{d(CLKL-DOV)}$	Delay time, SSP_CLK (output) falling edge to MOSI (output) transition	Clock Polarity = 1	-3.138	2.175	ns

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 48. LFBGA289 (15 x 15 x 1.7 mm) mechanical data

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.700			0.0669
A1	0.270			0.0106		
A2		0.985			0.0387	
A3		0.200			0.0078	
A4			0.800			0.0315
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	14.850	15.000	15.150	0.5846	0.5906	0.5965
D1		12.800			0.5039	
E	14.850	15.000	15.150	0.5846	0.5906	0.5965
E1		12.800			0.5039	
e		0.800			0.0315	
F		1.100			0.0433	
ddd			0.200			0.0078
eee			0.150			0.0059
fff			0.080			0.0031