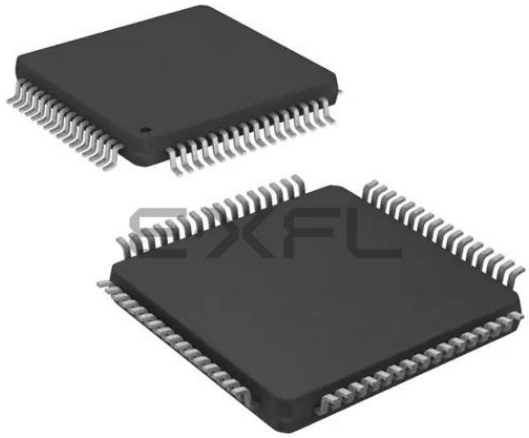

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.5K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 47x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f67k40-e-pt

4.3 Clock Source Types

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (ECH, ECM, ECL mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes).

A 4x PLL is provided that can be used in conjunction with the external clock. See **Section 4.3.1.4 "4x PLL"** for more details.

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators that are used to generate internal system clock sources. The High-Frequency Internal Oscillator (HFINTOSC) can produce 1, 2, 4, 8, 12, 16, 32, 48 and 64 MHz clock. The frequency can be controlled through the OSCFRQ register (Register 4-5). The Low-Frequency Internal Oscillator (LFINTOSC) generates a fixed 31 kHz frequency.

The system clock can be selected between external or internal clock sources via the NOSC bits in the OSCCON1 register. See **Section 4.4 "Clock Switching"** for additional information. The system clock can be made available on the OSC2/CLKOUT pin for any of the modes that do not use the OSC2 pin. The clock out functionality is governed by the $\overline{\text{CLKOUTEN}}$ bit in the CONFIG1H register (Register 3-2). If enabled, the clock out signal is always at a frequency of FOSC/4.

4.3.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC<2:0> and FEXTOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> and NDIV<3:0> bits in the OSCCON1 register to switch the system clock source.

See **Section 4.4 "Clock Switching"** for more information.

4.3.1.1 EC Mode

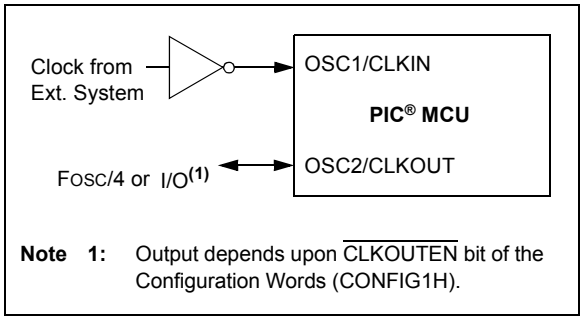
The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 4-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- ECH – High power, above 8 MHz
- ECM – Medium power, 100 kHz-8 MHz
- ECL – Low power, below 100 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 4-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Output depends upon $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words (CONFIG1H).

4.3.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

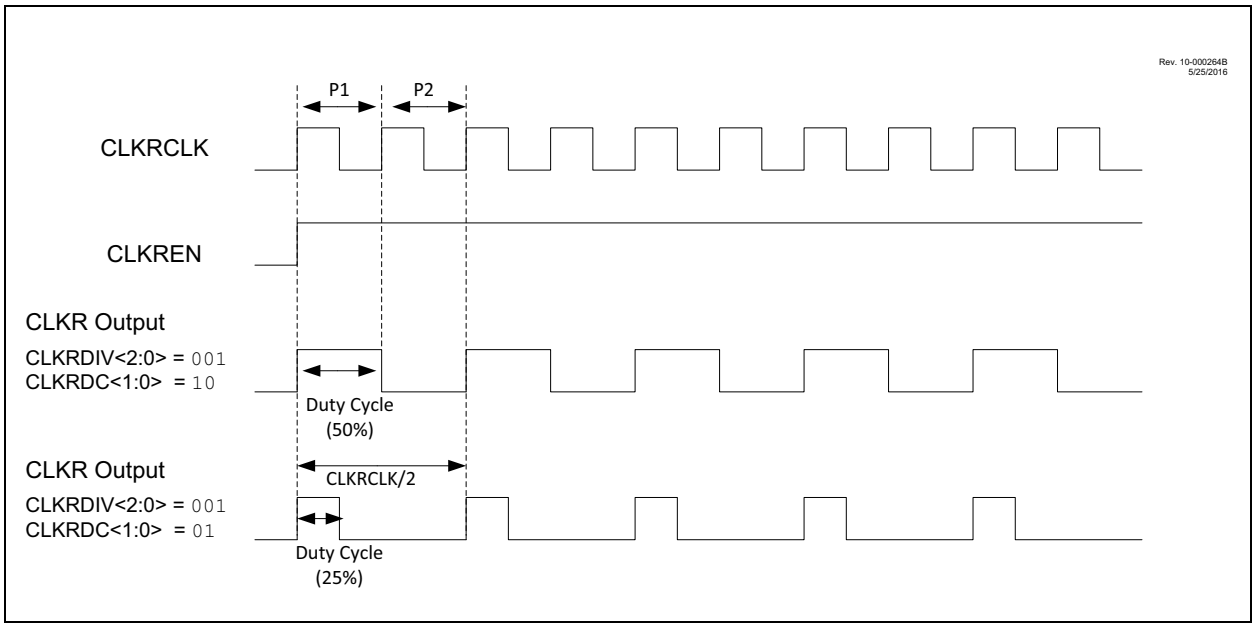
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification (above 100 kHz - 8 MHz).

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting (above 8 MHz).

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 5-2: CLOCK REFERENCE TIMING



9.7 Operation During Sleep

When the device enters Sleep, the WWDT is cleared. If the WWDT is enabled during Sleep, the WWDT resumes counting. When the device exits Sleep, the WWDT is cleared again.

The WWDT remains clear until the Oscillator Start-up Timer (OST) completes, if enabled. See **Section 4.3.1.3 "Oscillator Start-up Timer (OST)"** for more information on the OST.

When a WWDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register are changed to indicate the event. The $\overline{RWDT}$ bit in the PCON0 register can also be used. See **Section 10.0 "Memory Organization"** for more information.

TABLE 9-2: WWDT CLEARING CONDITIONS

Conditions	WWDT
WDTE<1:0> = 00	Cleared
WDTE<1:0> = 01 and SEN = 0	
WDTE<1:0> = 10 and enter Sleep	
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = SOSC, EXTRC, INTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST
Change INTOSC divider (IRCF bits)	Unaffected

FIGURE 9-2: WINDOW PERIOD AND DELAY

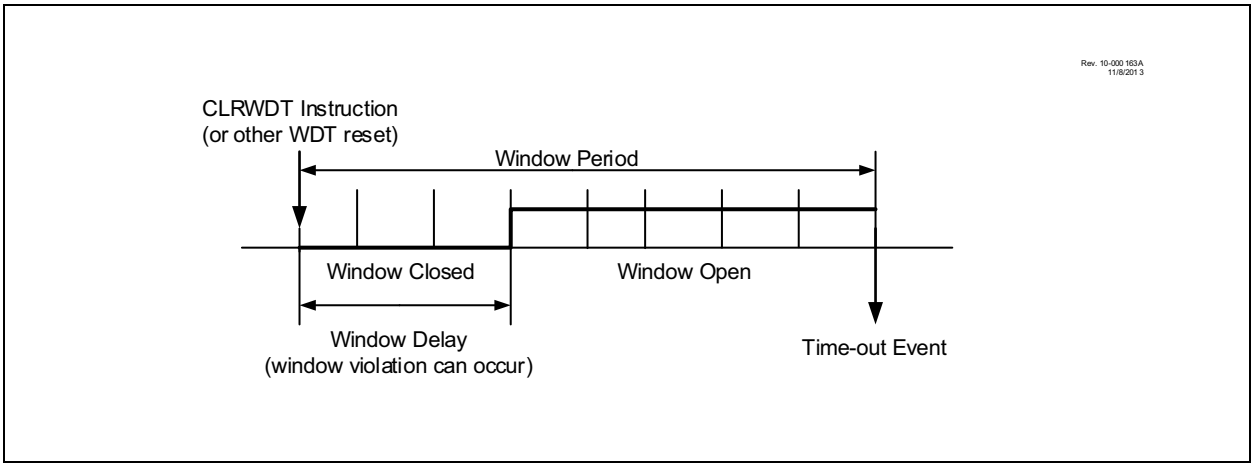


TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH WINDOWED WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PCON0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	74
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	121
WDTCON0	—	—	WDTPS<4:0>					SEN	83
WDTCON1	—	WDTCS<2:0>			—	WINDOW<2:0>			84
WDTPSL	PSCNT<7:0>								85
WDTPSH	PSCNT<15:8>								85
WDTTMR	WDTTMR<4:0>					STATE	PSCNT<17:16>		86

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by Windowed Watchdog Timer.

TABLE 9-4: SUMMARY OF CONFIGURATION WORD WITH WINDOWED WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Windowed Watchdog Timer.

10.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 enhanced microcontroller devices:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate buses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Program Flash Memory and Data EEPROM Memory is provided in **Section 11.0 "Nonvolatile Memory (NVM) Control"**.

10.1 Program Memory Organization

PIC18 microcontrollers implement a 21-bit program counter, which is capable of addressing a 2 Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2 Mbyte address will return all '0's (a NOP instruction).

These devices contains the following:

- PIC18(L)F67K40: 128 Kbytes of Flash memory, up to 65,536 single-word instructions

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

Note:	For memory information on this family of devices, see Table 10-1 and Table 10-2.

EXAMPLE 11-3: ERASING A PROGRAM FLASH MEMORY BLOCK

```
; This sample row erase routine assumes the following:
; 1. A valid address within the erase row is loaded in variables TBLPTR register
; 2. ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)

            MOVLW       CODE_ADDR_UPPER    ; load TBLPTR with the base
            MOVWF       TBLPTRU            ; address of the memory block
            MOVLW       CODE_ADDR_HIGH
            MOVWF       TBLPTRH
            MOVLW       CODE_ADDR_LOW
            MOVWF       TBLPTRL
ERASE_BLOCK
            BCF         NVMCON1, NVMREG0   ; point to Program Flash Memory
            BSF         NVMCON1, NVMREG1   ; access Program Flash Memory
            BSF         NVMCON1, WREN      ; enable write to memory
            BSF         NVMCON1, FREE      ; enable block Erase operation
            BCF         INTCON, GIE        ; disable interrupts
Required    MOVLW       55h
Sequence    MOVWF       NVMCON2            ; write 55h
            MOVLW       AAh
            MOVWF       NVMCON2            ; write AAh
            BSF         NVMCON1, WR        ; start erase (CPU stalls)
            BSF         INTCON, GIE        ; re-enable interrupts
```

13.2 Register Definitions: CRC and Scanner Control

Long bit name prefixes for the CRC and Scanner peripherals are shown in Table 13-1. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

TABLE 13-1:

Peripheral	Bit Name Prefix
CRC	CRC

REGISTER 13-1: CRCCON0: CRC CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R-0	R/W-0/0	U-0	U-0	R/W-0/0	R-0
EN	GO	BUSY	ACCM	—	—	SHIFTM	FULL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** CRC Enable bit
1 = CRC module is released from Reset
0 = CRC is disabled and consumes no operating current

bit 6 **GO:** CRC Start bit
1 = Start CRC serial shifter
0 = CRC serial shifter turned off

bit 5 **BUSY:** CRC Busy bit
1 = Shifting in progress or pending
0 = All valid bits in shifter have been shifted into accumulator and EMPTY = 1

bit 4 **ACCM:** Accumulator Mode bit
1 = Data is augmented with zeros
0 = Data is not augmented with zeros

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **SHIFTM:** Shift Mode bit
1 = Shift right (LSb)
0 = Shift left (MSb)

bit 0 **FULL:** Data Path Full Indicator bit
1 = CRCDATH/L registers are full
0 = CRCDATH/L registers have shifted their data into the shifter

REGISTER 13-2: CRCCON1: CRC CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
DLEN<3:0>				PLEN<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **DLEN<3:0>:** Data Length bits
Denotes the length of the data word -1 (See Example 13-1)

bit 3-0 **PLEN<3:0>:** Polynomial Length bits
Denotes the length of the polynomial -1 (See Example 13-1)

13.9 Program Memory Scan Configuration

If desired, the program memory scan module may be used in conjunction with the CRC module to perform a CRC calculation over a range of program memory addresses. In order to set up the scanner to work with the CRC you need to perform the following steps:

1. Set the Enable bit in both the CRCCON0 and SCANCON0 registers. If they get disabled, all internal states of the scanner and the CRC are reset (registers are unaffected).
2. Choose which memory access mode is to be used (see **Section 13.11 "Scanning Modes"**) and set the MODE bits of the SCANCON0 register appropriately.
3. Based on the memory access mode, set the INTM bits of the SCANCON0 register to the appropriate interrupt mode (see **Section 13.11.5 "Interrupt Interaction"**)
4. Set the SCANLADRL/H/U and SCANHADRL/H/U registers with the beginning and ending locations in memory that are to be scanned.
5. The CRCGO bit must be set before setting the SCANGO bit. Setting the SCANGO bit starts the scan. Both CRCEN and CRCGO bits must be enabled to use the scanner. When either of these bits are disabled, the scan aborts and the INVALID bit SCANCON0 is set. The scanner will wait for the signal from the CRC that it is ready for the first Flash memory location, then begin loading data into the CRC. It will continue to do so until it either hits the configured end address or an address that is unimplemented on the device, at which point the SCANGO bit will clear, Scanner functions will cease, and the SCANIF interrupt will be triggered. Alternately, the SCANGO bit can be cleared in software if desired.

13.10 Scanner Interrupt

The scanner will trigger an interrupt when the SCANGO bit transitions from '1' to '0'. The SCANIF interrupt flag of PIR7 is set when the last memory location is reached and the data is entered into the CRCDATA registers. The SCANIF bit can only be cleared in software. The SCAN interrupt enable is the SCANIE bit of the PIE7 register.

13.11 Scanning Modes

The memory scanner can scan in four modes: Burst, Peek, Concurrent, and Triggered. These modes are controlled by the MODE bits of the SCANCON0 register. The four modes are summarized in Table 13-2.

13.11.1 BURST MODE

When MODE = 01, the scanner is in Burst mode. In Burst mode, CPU operation is stalled beginning with the operation after the one that sets the SCANGO bit, and the scan begins, using the instruction clock to execute. The CPU is held in its current state until the scan stops. Note that because the CPU is not executing instructions, the SCANGO bit cannot be cleared in software, so the CPU will remain stalled until one of the hardware end-conditions occurs. Burst mode has the highest throughput for the scanner, but has the cost of stalling other execution while it occurs.

13.11.2 CONCURRENT MODE

When MODE = 00, the scanner is in Concurrent mode. Concurrent mode, like Burst mode, stalls the CPU while performing accesses of memory. However, while Burst mode stalls until all accesses are complete, Concurrent mode allows the CPU to execute in between access cycles.

13.11.3 TRIGGERED MODE

When MODE = 11, the scanner is in Triggered mode. Triggered mode behaves identically to Concurrent mode, except instead of beginning the scan immediately upon the SCANGO bit being set, it waits for a rising edge from a separate trigger clock, the source of which is determined by the SCANTRIG register.

13.11.4 PEEK MODE

When MODE = 10, the scanner is in Peek mode. Peek mode waits for an instruction cycle in which the CPU does not need to access the NVM (such as a branch instruction) and uses that cycle to do its own NVM access. This results in the lowest throughput for the NVM access (and can take a much longer time to complete a scan than the other modes), but does so without any impact on execution times, unlike the other modes.

15.3 Register Definitions: Port Control

REGISTER 15-1: PORTx: PORTx REGISTER(1)

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1	Rx0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets		

bit 7-0 **Rx<7:0>:** Rx7:Rx0 Port I/O Value bits
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTx are actually written to the corresponding LATx register. Reads from PORTx register return actual I/O pin values.

TABLE 15-1: PORT REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
PORTB	RB7(1)	RB6(1)	RB5	RB4	RB3	RB2	RB1	RB0
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
PORTE	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0
PORTG	RG7	RG6	RG5(2)	RG4	RG3	RG2	RG1	RG0
PORTH	—	—	—	—	RH3	RH2	RH1	RH0

Note 1: Bits RB6 and RB7 read '1' while in Debug mode.
2: Bit PORTG5 is read-only, and will read '1' when MCLRE = 1 (Master Clear enabled).

TABLE 17-1: PPS INPUT REGISTER DETAILS

Peripheral	PPS Input Register	Default Pin Selection at POR	Register Reset Value at POR	Input Available from Selected PORTx							
Interrupt 0	INT0PPS	RB0	0x08	A	B	—	—	—	—	—	—
Interrupt 1	INT1PPS	RB1	0x09	—	B	C	—	—	—	—	—
Interrupt 2	INT2PPS	RB2	0x0A	—	B	—	D	—	—	—	—
Interrupt 3	INT3PPS	RB3	0x0B	—	B	—	—	E	—	—	—
Timer0 Clock	T0CKIPPS	RA4	0x04	A	B	—	—	—	—	—	—
Timer1 Clock	T1CKIPPS	RC0	0x10	—	—	C	D	—	—	—	—
Timer1 Gate	T1GPPS	RB5	0x0D	—	B	C	—	—	—	—	—
Timer3 Clock	T3CKIPPS	RB5	0x0D	—	B	C	—	—	—	—	—
Timer3 Gate	T3GPPS	RA5	0x05	A	—	C	—	—	—	—	—
Timer5 Clock	T5CKIPPS	RD1	0x19	—	—	—	D	E	—	—	—
Timer5 Gate	T5GPPS	RG4	0x34	—	—	—	—	E	—	G	—
Timer7 Clock	T7CKIPPS	RG4	0x34	—	—	—	—	E	—	G	—
Timer7 Gate	T7GPPS	RD1	0x19	—	—	—	D	E	—	—	—
Timer2 Clock	T2INPPS	RA1	0x01	A	—	C	—	—	—	—	—
Timer4 Clock	T4INPPS	RE4	0x24	—	B	—	—	E	—	—	—
Timer6 Clock	T6INPPS	RC1	0x11	—	B	C	—	—	—	—	—
Timer8 Clock	T8INPPS	RA0	0x00	A	—	—	—	E	—	—	—
ADC Conversion Trigger	ADACTPPS	RH1	0x39	—	B	C	—	—	—	—	—
CCP1	CCP1PPS	RE5	0x25	—	—	—	—	E	—	G	—
CCP2	CCP2PPS	RE4	0x24	—	—	—	—	E	—	G	—
CCP3	CCP3PPS	RE6	0x26	—	—	C	—	E	—	—	—
CCP4	CCP4PPS	RG3	0x33	—	—	C	—	E	—	—	—
CCP5	CCP5PPS	RG4	0x34	—	—	C	—	E	—	—	—
SMT1 Window	SMT1WINPPS	RE6	0x26	—	—	C	—	E	—	—	—
SMT1 Signal	SMT1SIGPPS	RE7	0x27	—	—	C	—	E	—	—	—
SMT2 Window	SMT2WINPPS	RG6	0x36	—	—	C	—	—	—	G	—
SMT2 Signal	SMT2SIGPPS	RG7	0x37	—	—	C	—	—	—	G	—
CWG	CWG1PPS	RC2	0x12	A	—	C	—	—	—	—	—
DSM Carrier Low	MDCARLPPS	RD3	0x1B	—	—	—	D	—	—	—	H
DSM Carrier High	MDCARHPPS	RD4	0x1C	—	—	—	D	—	—	—	H
DSM Source	MDSRCPPS	RD5	0x1D	—	—	—	D	—	—	—	H
EUSART1 Receive	RX1PPS	RC7	0x17	—	—	C	D	—	—	—	—
EUSART1 Transmit	TX1PPS	RC6	0x16	—	—	C	D	—	—	—	—
EUSART2 Receive	RX2PPS	RG2	0x32	—	—	—	D	—	—	G	—
EUSART2 Transmit	TX2PPS	RG1	0x31	—	—	—	D	—	—	G	—
EUSART3 Receive	RX3PPS	RE1	0x21	—	B	—	—	E	—	—	—

22.1.5 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 22-4.

EQUATION 22-4: PWM RESOLUTION

$$Resolution = \frac{log[4(PR2 + 1)]}{log(2)} \ bits$$

Note:	If the pulse-width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 22-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	0.31 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	64	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 22-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	0.31 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	64	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

22.1.6 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

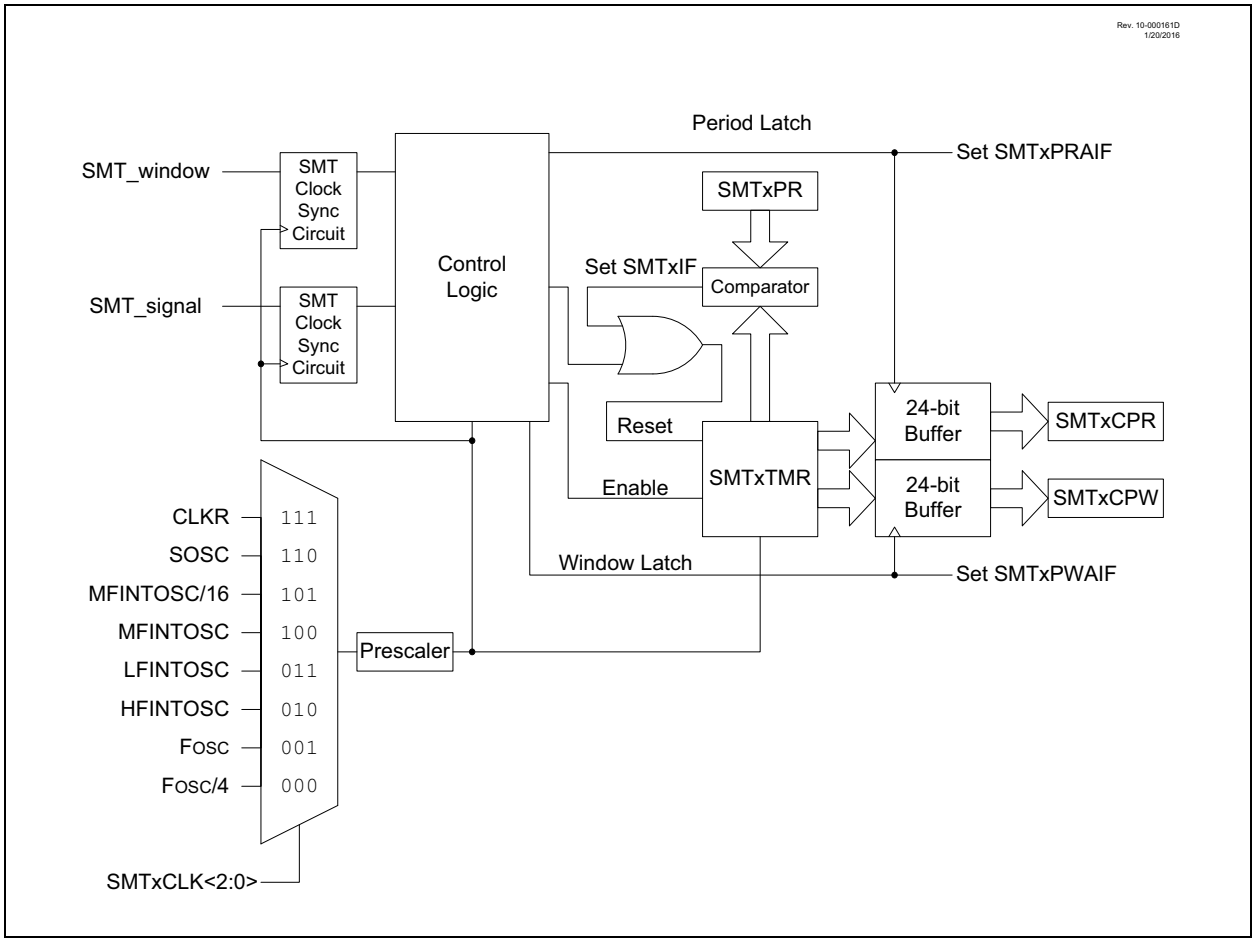
22.1.7 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (FOSC). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 4.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for additional details.

22.1.8 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the PWM registers to their Reset states.

FIGURE 25-1: SMTx BLOCK DIAGRAM



Note:	These devices implement two SMT modules. All references to SMTx apply to SMT1 and SMT2.

FIGURE 25-2: SMTx SIGNAL AND WINDOW BLOCK DIAGRAM

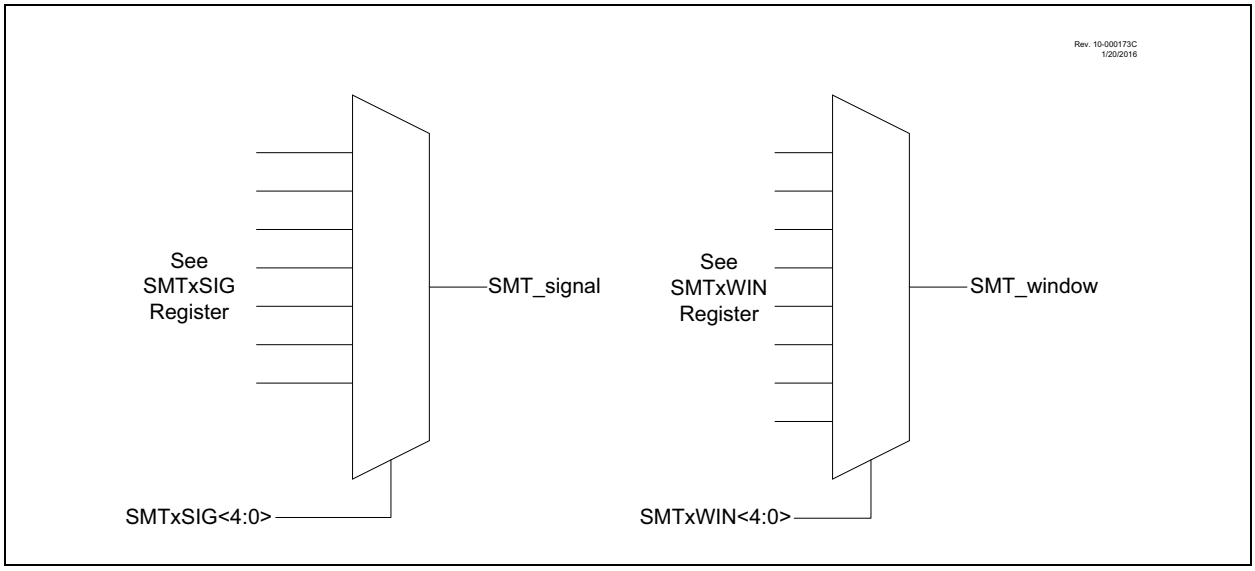


FIGURE 25-10: WINDOWED MEASURE MODE REPEAT ACQUISITION TIMING DIAGRAM

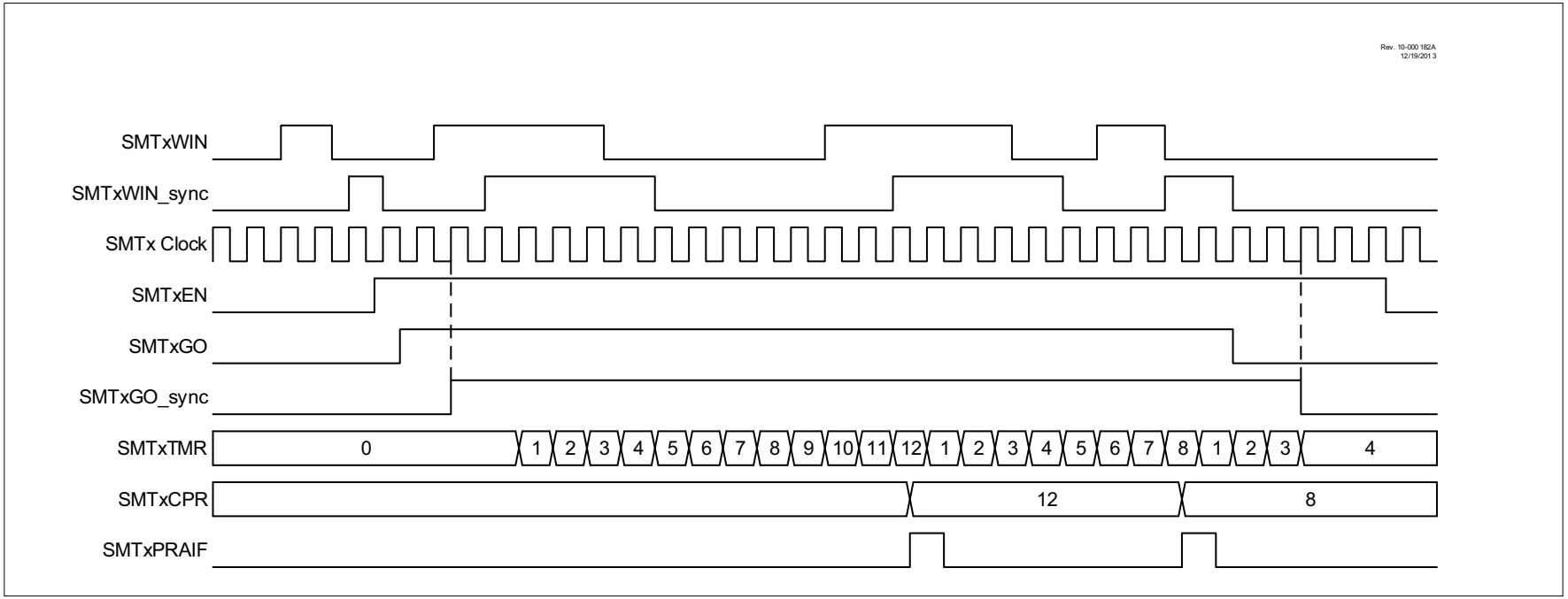


FIGURE 26-2: On Off Keying (OOK) Synchronization

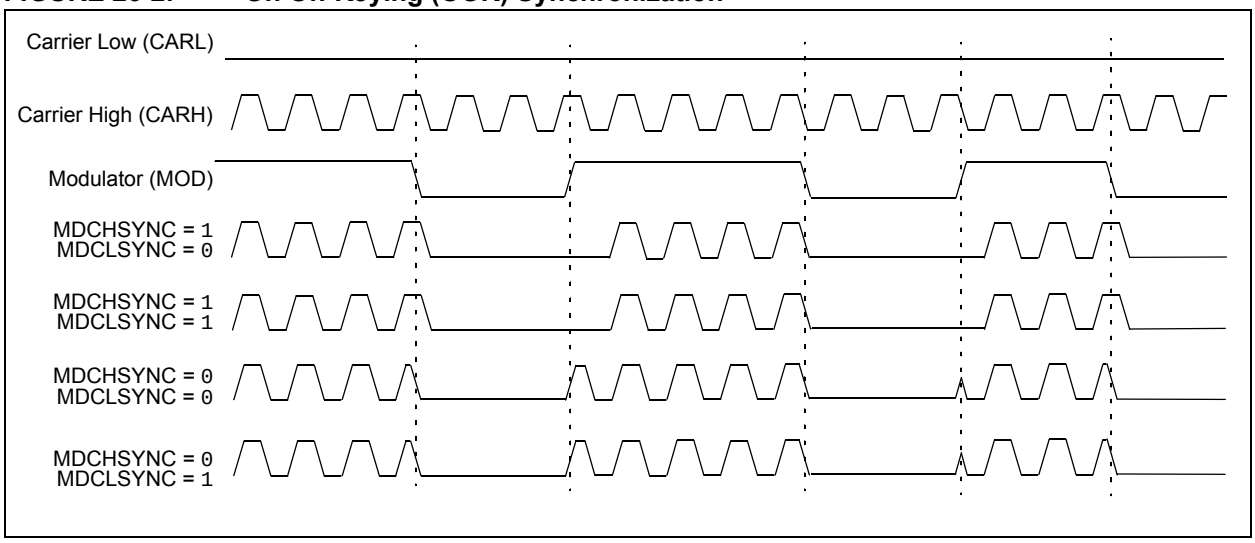


FIGURE 26-3: No Synchronization (MDSHSYNC = 0, MDCLSYNC = 0)

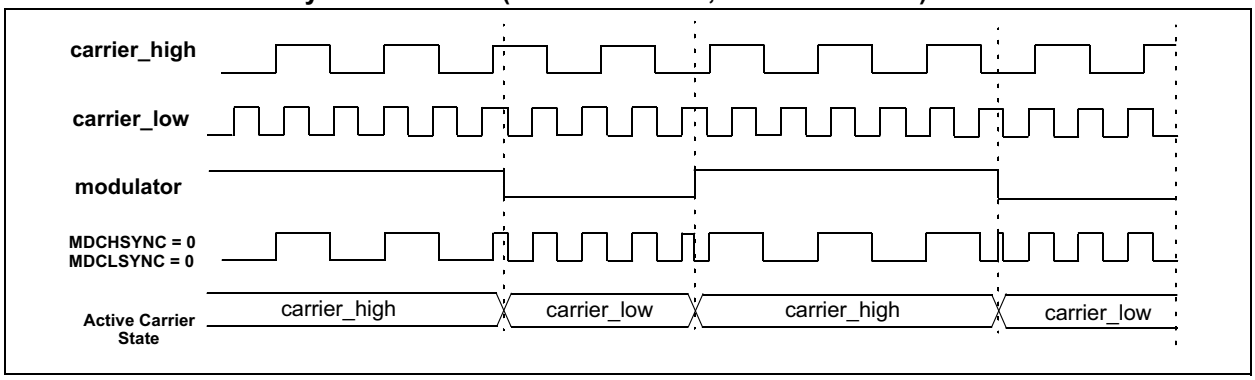


FIGURE 26-4: Carrier High Synchronization (MDSHSYNC = 1, MDCLSYNC = 0)

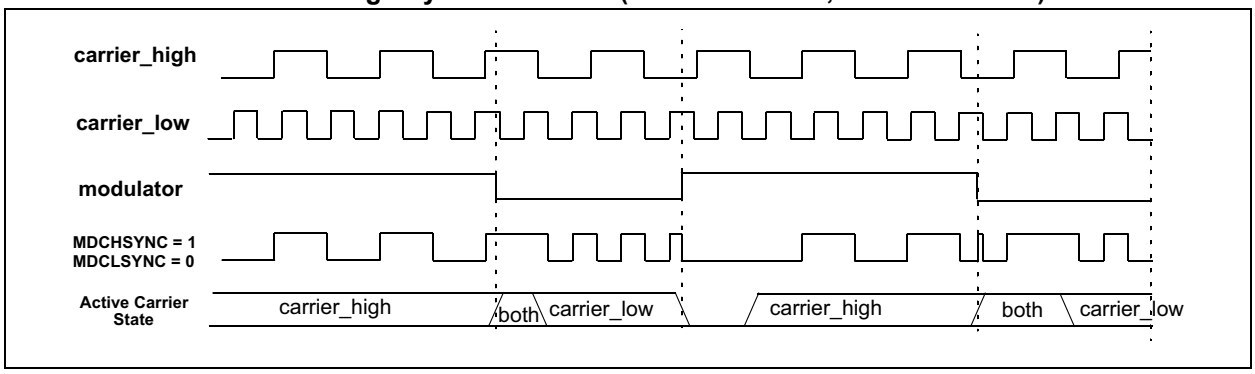


FIGURE 26-5: Carrier Low Synchronization (MDSHSYNC = 0, MDCLSYNC = 1)

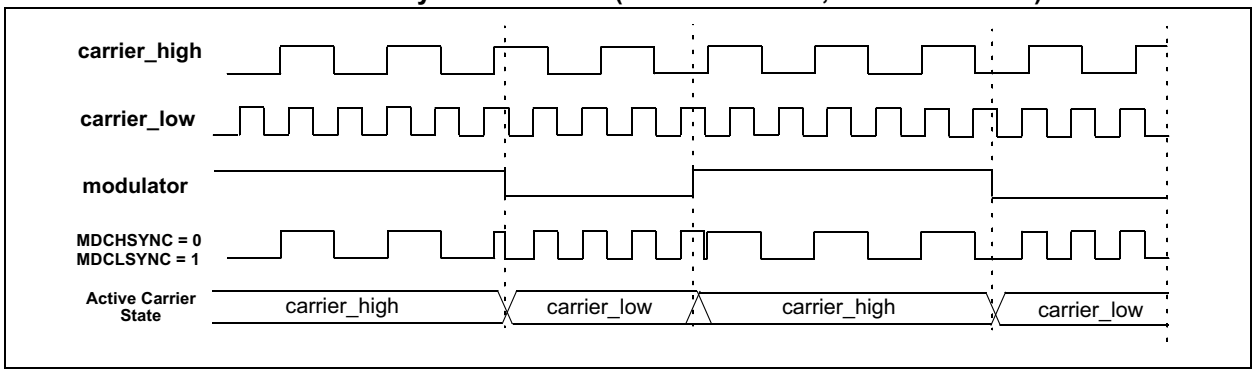
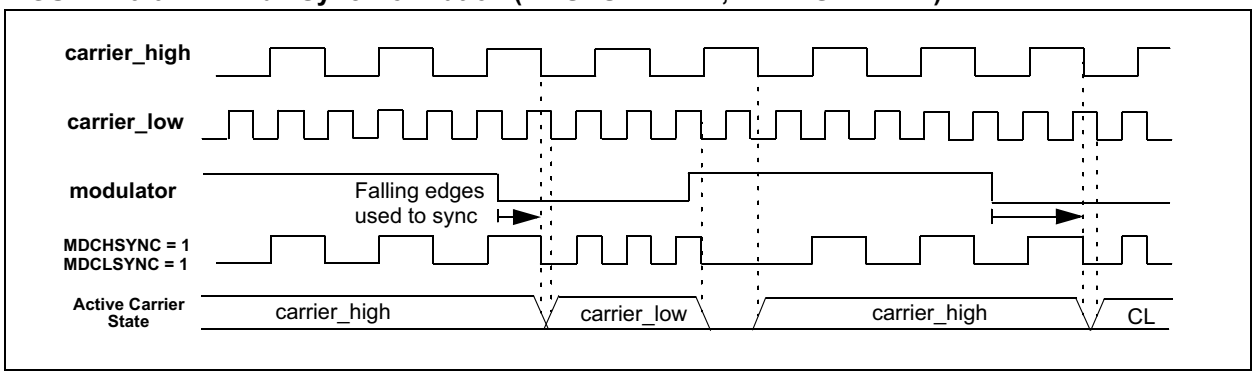


FIGURE 26-6: Full Synchronization (MDSHSYNC = 1, MDCLSYNC = 1)



32.2 ADC Operation

32.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. A conversion may be started by any of the following:

- Software setting the ADGO bit of ADCON0 to '1'
- An external trigger (selected by Register 32-3)
- A continuous-mode retrigger (see section **Section 32.5.8 "Continuous Sampling mode"**)

.

Note:	The ADGO bit should not be set in the same instruction that turns on the ADC. Refer to **Section 32.2.6 "ADC Conversion Procedure (Basic Mode)"**.

32.2.2 COMPLETION OF A CONVERSION

When any individual conversion is complete, the value already in ADRES is written into ADPREV (if ADPSIS = 1) and the new conversion results appear in ADRES. When the conversion completes, the ADC module will:

- Clear the ADGO bit (unless the ADCONT bit of ADCON0 is set)
- Set the ADIF Interrupt Flag bit
- Set the ADMATH bit
- Update ADACC

When ADDSEN = 0 then after every conversion, or when ADDSEN = 1 then after every other conversion, the following events occur:

- ADERR is calculated
- ADTIF is set if ADERR calculation meets threshold comparison

Importantly, filter and threshold computations occur after the conversion itself is complete. As such, interrupt handlers responding to ADIF should check ADTIF before reading filter and threshold results.

32.2.3 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC oscillator source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

32.2.4 EXTERNAL TRIGGER DURING SLEEP

If the external trigger is received during sleep while ADC clock source is set to the FRC, ADC module will perform the conversion and set the ADIF bit upon completion.

If an external trigger is received when the ADC clock source is something other than FRC, the trigger will be recorded, but the conversion will not begin until the device exits Sleep.

32.2.5 AUTO-CONVERSION TRIGGER

The Auto-conversion Trigger allows periodic ADC measurements without software intervention. When a rising edge of the selected source occurs, the ADGO bit is set by hardware.

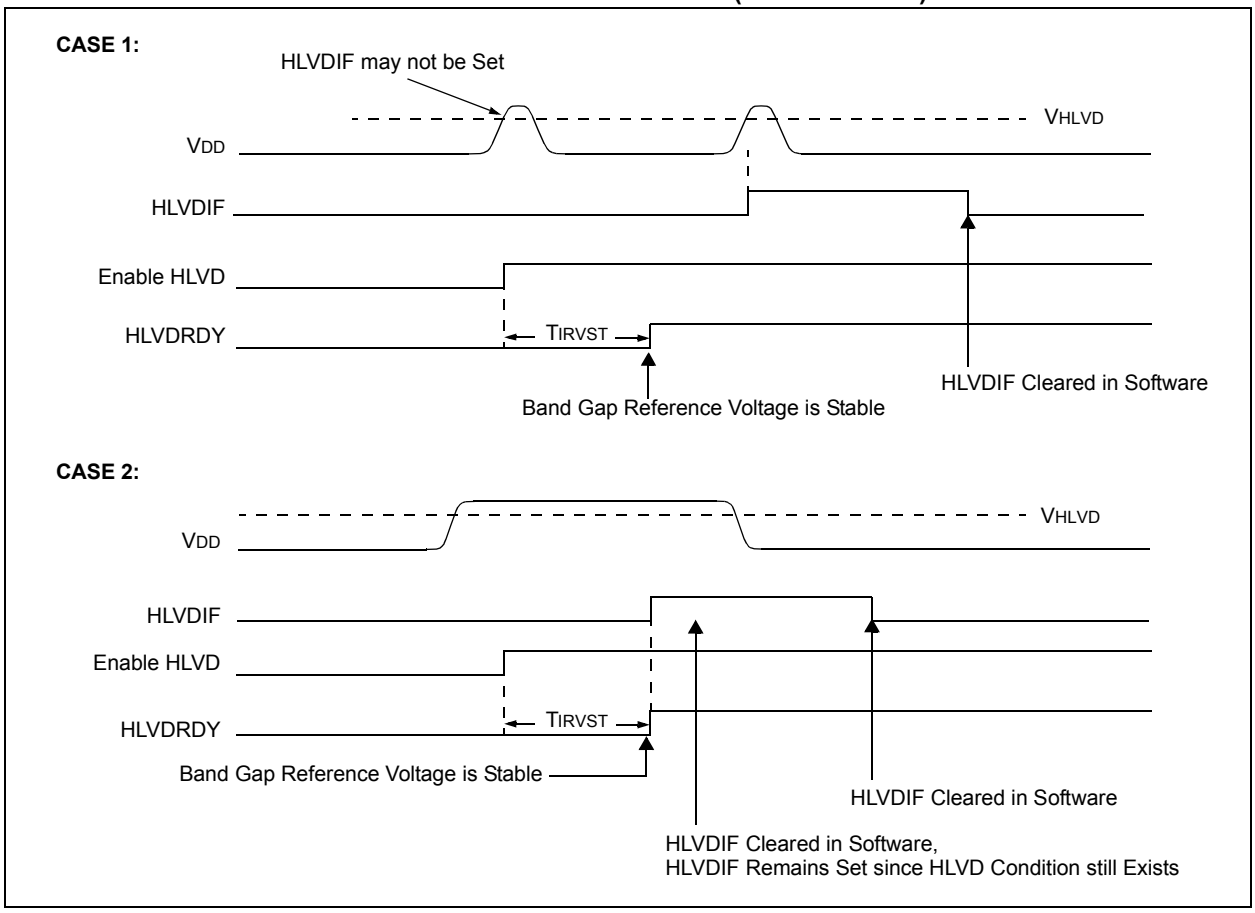
The Auto-conversion Trigger source is selected with the ADACT<4:0> bits of the ADACT register.

Using the Auto-conversion Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met. See Table 32-2 for auto-conversion sources.

TABLE 32-2: ADC AUTO-CONVERSION TABLE

Source Peripheral	Description
ADCACTPPS	Pin selected by ADCACTPPS
TMR0	Timer0 overflow condition
TMR1/3/5/7	Timer1/3/5/7 overflow condition
TMR2/4/6/8	Match between Timer2/4/6/8 postscaled value and PR2/4/6/8
CCP1/2/3/4/5	CCP1/2/3/4/5 output
PWM/6/7	PWM/6/7 output
C1/2/3	Comparator C1/2/3 output
IOC	Interrupt-on-change interrupt trigger
ADERR	Read of ADERRH register
ADRESH	Read of ADRESH register
ADPCH	Write of ADPCH register
SMT1/2	Signal Measurement Timer 1/2 Out

FIGURE 34-3: HIGH-VOLTAGE DETECT OPERATION (HLVDINTH = 1)



34.5 Applications

In many applications, it is desirable to detect a drop below, or rise above, a particular voltage threshold. For example, the HLVD module could be periodically enabled to detect Universal Serial Bus (USB) attach or detach. This assumes the device is powered by a lower voltage source than the USB when detached. An attach would indicate a High-Voltage Detect from, for example, 3.3V to 5V (the voltage on USB) and vice versa for a detach. This feature could save a design a few extra components and an attach signal (input pin).

For general battery applications, Figure 34-4 shows a possible voltage curve. Over time, the device voltage decreases. When the device voltage reaches voltage, VA, the HLVD logic generates an interrupt at time, TA. The interrupt could cause the execution of an Interrupt Service Routine (ISR), which would allow the application to perform “housekeeping tasks” and a controlled shutdown before the device voltage exits the valid operating range at TB. This would give the application a time window, represented by the difference between TA and TB, to safely exit.

FIGURE 34-4: TYPICAL LOW-VOLTAGE DETECT APPLICATION

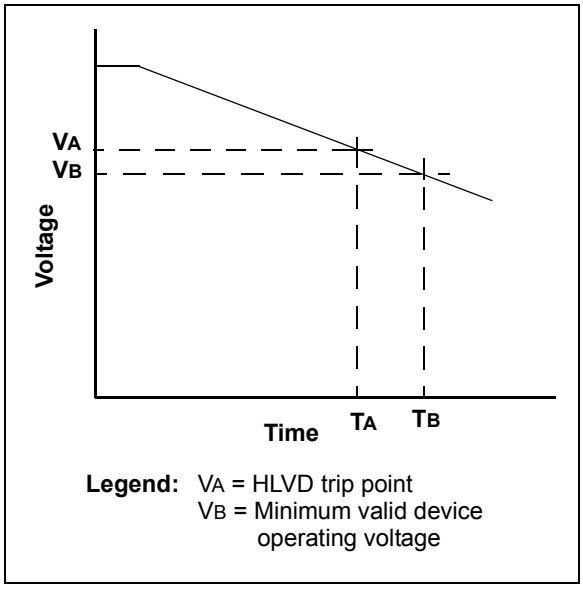
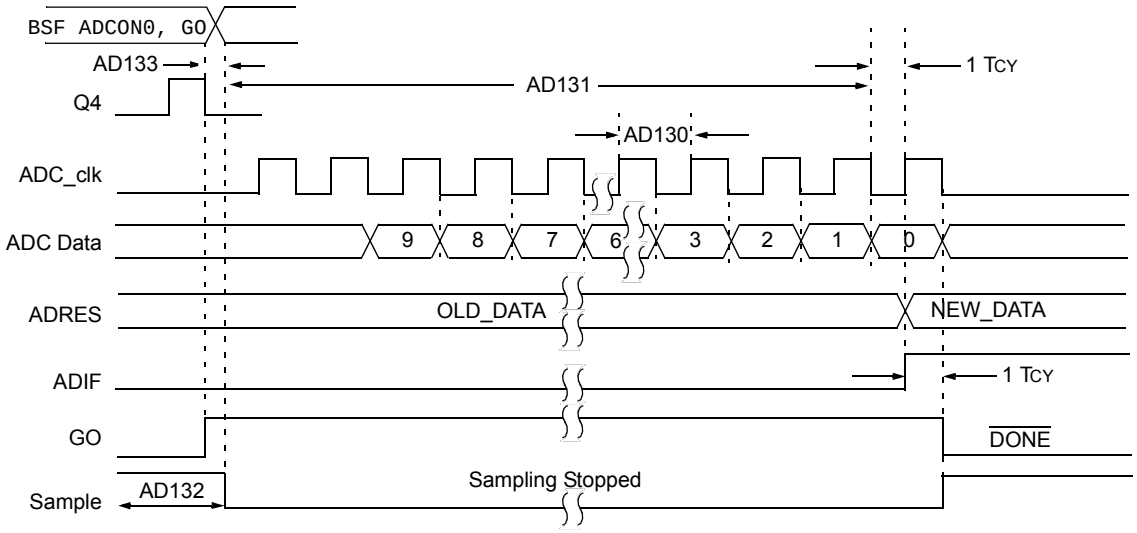
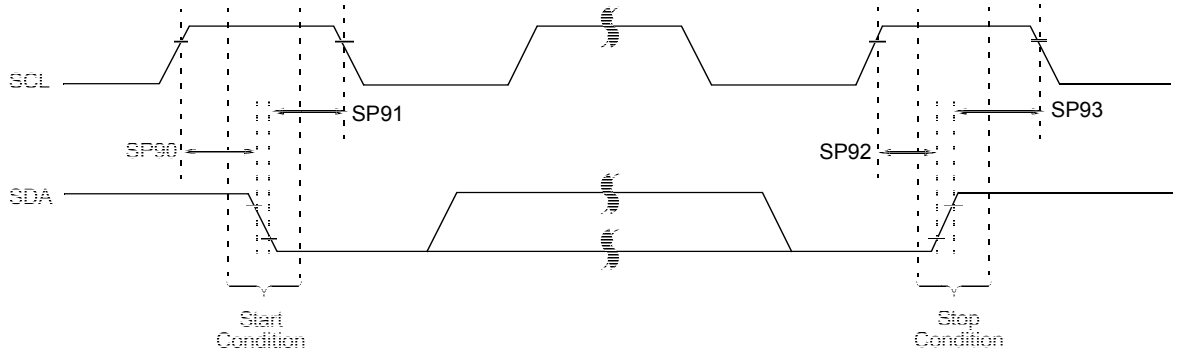


FIGURE 38-11: ADC CONVERSION TIMING (ADC CLOCK FROM ADCRC)



Note 1: If the ADC clock source is selected as ADCRC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.

FIGURE 38-20: I²C BUS START/STOP BITS TIMING



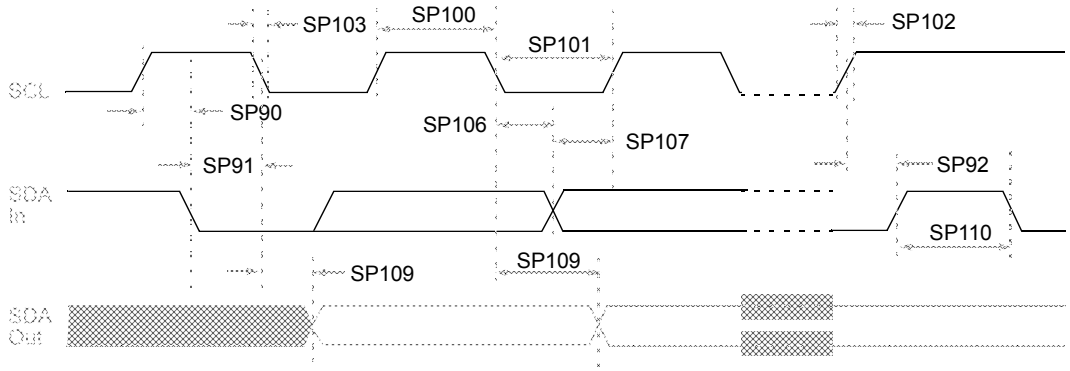
Note: Refer to Figure 38-4 for load conditions.

TABLE 38-24: I²C BUS START/STOP BITS REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
SP90*	TSU:STA	Start condition	100 kHz mode	4700	—	—	ns	Only relevant for Repeated Start condition
		Setup time	400 kHz mode	600	—	—		
SP91*	THD:STA	Start condition	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
SP92*	TSU:STO	Stop condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
SP93	THD:STO	Stop condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

FIGURE 38-21: I²C BUS DATA TIMING



Note: Refer to Figure 38-4 for load conditions.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features[1]	PIC18(L)F65K40	PIC18(L)F66K40	PIC18(L)F67K40
Program Memory (Bytes)	32768	65536	131072
SRAM (Bytes)	2048	3562	3562

Note 1: PIC18F6xK40: operating voltage, 2.3V-5.5V. PIC18LF6xK40: operating voltage, 1.8V-3.6V.