Renesas Electronics America Inc - IDT79RC32T351-100DH Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t351-100dh

- *Supports burst transfers*

◆ **USB**
- *Revision 1.1 compliant*
- *USB slave device controller*
- *Supports a 6th USB endpoint*
- *Full speed operation at 12 Mb/s*
- *Supports control, interrupt, bulk and isochronous endpoints*
- *Supports USB remote wakeup*
- *Integrated USB transceiver*

◆ **EJTAG**
- *Run-time Mode provides a standard JTAG interface*
- *Real-Time Mode provides additional pins for real-time trace information*

◆ **Ethernet**
- *Full duplex support for 10 and 100 Mb/s Ethernet*
- *IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface*
- *IEEE 802.3u auto-negotiation for automatic speed selection*
- *Flexible address filtering modes*
- *64-entry hash table based multicast address filtering*

◆ **ATM SAR**
- *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
- *Supports 25Mb/s and faster ATM*
- *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
- *Supports standard 53-byte ATM cells*
- *Performs HEC generation and checking*
- *Cell processing discards short cells and clips long cells*
- *16 cells worth of buffering*
- *UTOPIA modes: 8 cell input buffer and 8 cell output buffer*
- *Hardware support for CRC-32 generation and checking for AAL5*
- *Hardware support for CRC-10 generation and checking*
- *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
- *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention*

◆ **System Features**
- *JTAG interface (IEEE Std. 1149.1 compatible)*
- *208 pin PQFP package*
- *2.5V core supply and 3.3V I/O supply*
- *Up to 133 MHz pipeline frequency and up to 66 MHz bus frequency*

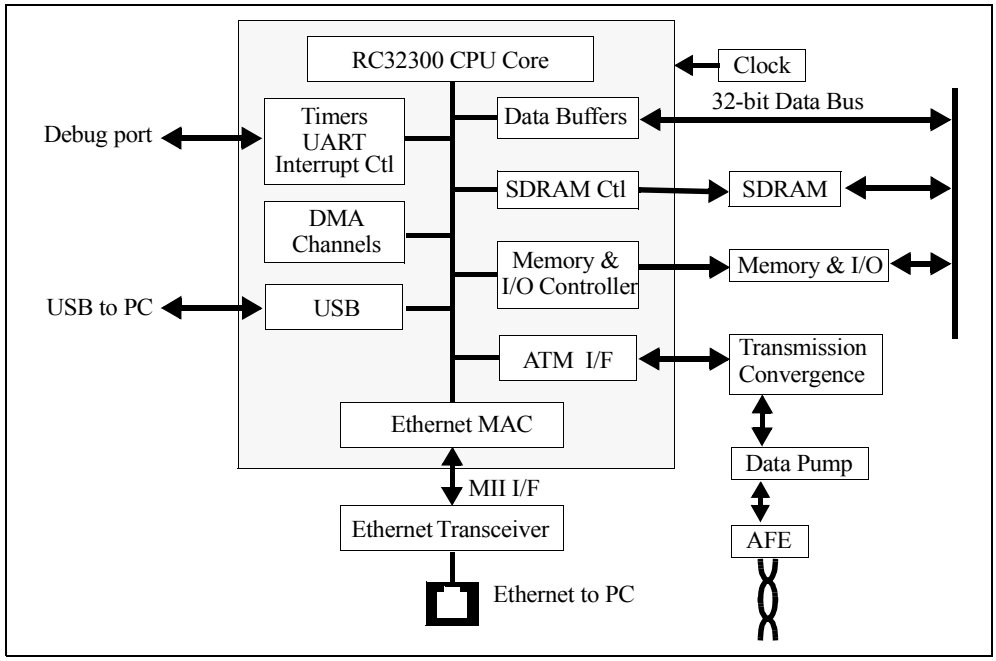


Figure 2 Example of xDSL Residential Gateway Using RC32351

Device Overview

The RC32351 is a “System on a Chip” which contains a high performance 32-bit microprocessor. The microprocessor core is used extensively at the heart of the device to implement the most needed functionalities in software with minimal hardware support. The high performance microprocessor handles diverse general computing tasks and specific application tasks that would have required dedicated hardware. Specific application tasks implemented in software can include routing functions, fire wall functions, modem emulation, ATM SAR emulation, and others.

The RC32351 meets the requirements of various embedded communications and digital consumer applications. It is a single chip solution that incorporates most of the generic system functionalities and application specific interfaces that enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate.

CPU Execution Core

The RC32351 is built around the RC32300 32-bit high performance microprocessor core. The RC32300 implements the enhanced MIPS-II ISA and helps meet the real-time goals and maximize throughput of communications and consumer systems by providing capabilities such as a prefetch instruction, multiple DSP instructions, and cache locking. The DSP instructions enable the RC32300 to implement 33.6 and 56kbps modem functionality in software, removing the need for external dedicated hardware. Cache locking guarantees real-time performance by holding critical DSP code and parameters in the cache for immediate availability. The microprocessor also implements an on-chip MMU with a TLB, making the it fully compliant with the requirements of real time operating systems.

Memory and IO Controller

The RC32351 incorporates a flexible memory and peripheral device controller providing support for SDRAM, Flash ROM, SRAM, dual-port memory, and other I/O devices. It can interface directly to 8-bit boot ROM for a very low cost system implementation. It enables access to high bandwidth external memory (200 MB/sec peak) at very low system costs. It also offers various trade-offs in cost / performance for the main memory architecture. The timers implemented on the RC32351 satisfy the requirements of most RTOS.

DMA Controller

The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The DMA controller supports scatter / gather DMA with no alignment restrictions, appropriate for communications and graphics systems.

Ethernet Interface

The RC32351 contains an on-chip Ethernet MAC capable of 10 and 100 Mbps line interface with an MII interface. It supports up to 4 MAC addresses. In a SOHO router, the high performance RC32300 CPU core routes the data between the Ethernet and the ATM interface. In other applications, such as high speed modems, the Ethernet interface can be used to connect to the PC.

USB Device Interface

The RC32351 includes the industry standard USB device interface to enable consumer appliances to directly connect to the PC.

ATM SAR

The RC32351 includes a configurable ATM SAR that supports a UTOPIA level 1 or a UTOPIA level 2 interface. The ATM SAR is implemented as a hybrid between software and hardware. A hardware block provides the necessary low level blocks (like CRC generation and checking and cell buffering) while the software is used for higher level SARing functions. In xDSL modem applications, the UTOPIA port interfaces directly to an xDSL chip set. In SOHO routers or in a line card for a Layer 3 switch, it provides access to an ATM network.

Enhanced JTAG Interface for ICE

For low-cost In-Circuit Emulation (ICE), the RC32300 CPU core includes an Enhanced JTAG (EJTAG) interface. This interface consists of two operation modes: Run-Time Mode and Real-Time Mode.

The Run-Time Mode provides a standard JTAG interface for on-chip debugging, and the Real-Time Mode provides additional status pins—PCST[2:0]—which are used in conjunction with the JTAG pins for real-time trace information at the processor internal clock or any division of the pipeline clock.

Thermal Considerations

The RC32351 consumes less than 1.5 W peak power and is guaranteed in an ambient temperature range of 0° to +70° C (commercial).

Revision History

January 7, 2002: Initial publication.

May 20, 2002: Added values (in place of TBD) to Table 18, Power Consumption.

September 19, 2002: Added COLDRSTN Trise1 parameter to Table 5, Reset and System AC Timing Characteristics.

December 6, 2002: In Features section, changed UART speed from 115 Kb/s to 1.5 Mb/s.

December 17, 2002: Added V_{OH} parameter to Table 16, DC Electrical Characteristics.

May 25, 2004: In Table 7, signals MIIRXCLK and MIITXCLK, the Min and Max values for 10 Mbps Thigh1/Tlow1 were changed to 140 and 260 respectively and the Min and Max values for 100 Mbps Thigh1/Tlow1 were changed to 14.0 and 26.0 respectively.

Pin Description Table

The following table lists the functions of the pins provided on the RC32351. Some of the functions listed may be multiplexed onto the same pin.

To define the active polarity of a signal, a suffix will be used. Signals ending with an "N" should be interpreted as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses and select lines) will be interpreted as being active, or asserted when at a logic one (high) level.

Note: The input pads of the RC32351 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as BRN) which, if left floating, could adversely affect the RC32351's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Name	Type	I/O Type	Description
System			
CLKP	I	Input	**System Clock input.** This is the system master clock input. The RISCore 32300 pipeline frequency is a multiple (x2, x3, or x4) of this clock frequency. All other logic runs at this frequency or less.
COLDRSTN	I	STI[1]	**Cold Reset.** The assertion of this signal low initiates a cold reset. This causes the RC32351 state to be initialized, boot configuration to be loaded, and the internal processor PLL to lock onto the system clock (CLKP).
RSTN	I/O	Low Drive with STI	**Reset.** This bidirectional signal is either driven low or tri-stated, an external pull-up is required to supply the high state. The RC32351 drives RSTN low during a reset (to inform the external system that a reset is taking place) and then tri-states it. The external system can drive RSTN low to initiate a warm reset, and then should tri-state it.
SYSCLKP	O	High Drive	**System clock output.** This is a buffered and delayed version of the system clock input (CLKP). All SDRAM transactions are synchronous to this clock. This pin should be externally connected to the SDRAMs and to the RC32351 SDCLKINP pin (SDRAM clock input).
Memory and Peripheral Bus			
MADDR[25:0]	O	[21:0] High Drive [25:22] Low Drive with STI	**Memory Address Bus.** 26-bit address bus for memory and peripheral accesses. MADDR[20:17] are used for the SODIMM data mask enables if SODIMM mode is selected. MADDR[22] Primary function: General Purpose I/O, GPIOP[27]. MADDR[23] Primary function: General Purpose I/O, GPIOP[28]. MADDR[24] Primary function: General Purpose I/O, GPIOP[29]. MADDR[25] Primary function: General Purpose I/O, GPIOP[30].
MDATA[31:0]	I/O	High Drive	**Memory Data Bus.** 32-bit data bus for memory and peripheral accesses.
BDIRN	O	High Drive	**External Buffer Direction.** External transceiver direction control for the memory and peripheral data bus, MDATA[31:0]. It is asserted low during any read transaction, and remains high during write transactions.
BOEN[1:0]	O	High Drive	**External Buffer Output Enable.** These signals provide two output enable controls for external data bus transceivers on the memory and peripheral data bus, MDATA. BOEN[0] is asserted low during external device read transactions. BOEN[1] is asserted low during SDRAM read transactions.
BRN	I	STI	**External Bus Request.** This signal is asserted low by an external master device to request ownership of the memory and peripheral bus.
BGN	O	Low Drive	**External Bus Grant.** This signal is asserted low by RC32351 to indicate that RC32351 has relinquished ownership of the local memory and peripheral bus to an external master.
WAITACKN	I	STI	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted low during a memory and peripheral device bus transaction to extend the bus cycle. When configured as transfer acknowledge, this signal is asserted low during a memory and peripheral device bus transaction to signal the completion of the transaction.
CSN[5:0]	O	[3:0] High Drive [5:4] Low Drive	**Device Chip Select.** These signals are used to select an external device on the memory and peripheral bus during device transactions. Each bit is asserted low during an access to the selected external device. CSN[4] Primary function: General purpose I/O, GPIOP[16]. CSN[5] Primary function: General purpose I/O, GPIOP[17].

Table 1 Pin Descriptions (Part 1 of 7)

Name	Type	I/O Type	Description
MIIMDIOP	I/O	Low Drive with STI	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
MIIRXCLKP	I	STI	**MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data.
MIIRXDP[3:0]	I	STI	**MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY.
MIIRXDVP	I	STI	**MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MIIRXERP	I	STI	**MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MIITXCLKP	I	STI	**MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MIITXDP[3:0]	O	Low Drive	**MII Transmit Data.** This nibble wide data bus contains the data to be transmitted.
MIITXENP	O	Low Drive	**MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission.
MIITXERP	O	Low Drive	**MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
EJTAG			
JTAG_TCK	I	STI	**JTAG Clock.** This is an input test clock, used to shift data into or out of the boundary scan logic. This signal requires an external resistor, listed in Table 14.
JTAG_TDI	I	STI	**JTAG Data Input.** This is the serial data shifted into the boundary scan logic. This signal requires an external resistor, listed in Table 14. This is also used to input EJTAG_DINTN during EJTAG/ICE mode. EJTAG_DINTN is an interrupt to switch the PC trace mode off.
JTAG_TDO	O	Low Drive	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic. When no data is being shifted out, this signal is tri-stated. This signal requires an external resistor, listed in Table 14. This is also used to output the EJTAG_TPC during EJTAG/ICE mode. EJTAG_TPC is the non-sequential program counter output.
JTAG_TMS	I	STI	**JTAG Mode Select**. This input signal is decoded by the tap controller to control test operation. This signal requires an external resistor, listed in Table 14.
EJTAG_PCST[0]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[10]. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN.
EJTAG_PCST[1]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11]. 1st Alternate function: UART channel 1 data set ready, U1DSRN.
EJTAG_PCST[2]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[12]. 1st Alternate function: UART channel 1 request to send, U1RTSN.
EJTAG_DCLK	O	Low Drive	**PC trace clock.** This is used to capture address and data during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[13]. 1st Alternate function: UART channel 1 clear to send, U1CTSN.

Table 1 Pin Descriptions (Part 5 of 7)

Name	Type	I/O Type	Description
EJTAG_TRST_N	I	STI	**EJTAG Test Reset.** EJTAG_TRST_N is an active-low signal for asynchronous reset of only the EJTAG/ICE controller. EJTAG_TRST_N requires an external pull-up on the board. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary: General Purpose I/O, GPIOP[31] 1st Alternate function: DMA finished output, DMAFIN.
JTAG_TRST_N	I	STI	**JTAG Test Reset.** JTAG_TRST_N is an active-low signal for asynchronous reset of only the JTAG boundary scan controller. JTAG_TRST_N requires an external pull-down on the board that will hold the JTAG boundary scan controller in reset when not in use if selected. JTAG reset enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[2]. 1st Alternate function: UART channel 0 ring indicator, U0RIN.
Debug			
INSTP	O	Low Drive	**Instruction or Data Indicator**. This signal is driven high during CPU instruction fetches and low during CPU data transactions on the memory and peripheral bus.
CPUP	O	Low Drive	**CPU or DMA Transaction Indicator**. This signal is driven high during CPU transactions and low during DMA transactions on the memory and peripheral bus if CPU/DMA Transaction Indicator Enable is enabled. CPU/DMA Status mode enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[4]. 1st Alternate function: UART channel 0 data terminal ready U0DTRN.
DMAP[0]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[23]. 1st Alternate function: TXADDR[1].
DMAP[1]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[25]. 1st Alternate function: RXADDR[1].
DMAP[2]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[9]. 1st Alternate function: U1SINP.
DMAP[3]	O	Low Drive	**Active DMA channel code**. DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[8]. 1st Alternate function: U1SOUTP.
UART			
U0SOUTP	I	STI	**UART channel 0 serial transmit.** Primary function: General Purpose I/O, GPIOP[0]. At reset, this pin defaults to primary function GPIOP[0].
U0SINP	I	STI	**UART channel 0 serial receive.** Primary function: General Purpose I/O, GPIOP[1]. At reset, this pin defaults to primary function GPIOP[1].
U0RIN	I	STI	**UART channel 0 ring indicator.** Primary function: General Purpose I/O, GPIOP[2]. At reset, this pin defaults to primary function GPIOP[2] if JTAG reset enable is not selected during reset using the boot configuration. 2nd Alternate function: JTAG boundary scan reset, JTAG_TRST_N.
U0DCRN	I	STI	**UART channel 0 data carrier detect.** Primary function: General Purpose I/O, GPIOP[3]. At reset, this pin defaults to primary function GPIOP[3].

Table 1 Pin Descriptions (Part 6 of 7)

Name	Type	I/O Type	Description
U0DTRN	O	Low Drive	**UART channel 0 data terminal ready.** Primary function: General Purpose I/O, GPIOP[4]. At reset, this pin defaults to primary function GPIOP[4] if CPU/DMA Status Mode enable is not selected during reset using the boot configuration. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.
U0DSRN	I	STI	**UART channel 0 data set ready.** Primary function: General Purpose I/O, GPIOP[5]. At reset, this pin defaults to primary function GPIOP[5].
U0RTSN	O	Low Drive	**UART channel 0 request to send.** Primary function: General Purpose I/O, GPIOP[6]. At reset, this pin defaults to primary function GPIOP[6].
U0CTSN	I	STI	**UART channel 0 clear to send.** Primary function: General Purpose I/O, GPIOP[7]. At reset, this pin defaults to primary function GPIOP[7].
U0SOUTP	O	Low Drive	**UART channel 1 serial transmit.** Primary function: General Purpose I/O, GPIOP[8]. At reset, this pin defaults to primary function GPIOP[8] if DMA Debug enable is not selected during reset using the boot configuration. 2nd Alternate function: DMA channel, DMAP[3].
U1SINP	I	STI	**UART channel 1 serial receive.** Primary function: General Purpose I/O, GPIOP[9]. At reset, this pin defaults to primary function GPIOP[9] if DMA Debug enable is not selected during reset using the boot configuration. 2nd Alternate function: DMA channel, DMAP[2].
U1DTRN	O	Low Drive	**UART channel 1 data terminal ready.** Primary function: General Purpose I/O, GPIOP[10]. At reset, this pin defaults to primary function GPIOP[10] if ICE Interface enable is not selected during reset using the boot configuration. Alternate function: PC trace status bit 0, EJTAG_PCST[0].
U1DSRN	I	STI	**UART channel 1 data set ready.** Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace status bit 1, EJTAG_PCST[1].
U1RTSN	O	Low Drive	**UART channel 1 request to send.** Primary function: General Purpose I/O, GPIOP[12]. At reset, this pin defaults to primary function GPIOP[12] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace status bit 2, EJTAG_PCST[2].
U1CTSN	I	STI	**UART channel 1 clear to send.** Primary function: General Purpose I/O, GPIOP[13]. At reset, this pin defaults to primary function GPIOP[13] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace clock, EJTAG_DCLK.

Table 1 Pin Descriptions (Part 7 of 7)

1. Schmitt Trigger Input.

Boot Configuration Vector

The boot configuration vector is read into the RC32351 during cold reset. The vector defines parameters in the RC32351 that are essential to operation when cold reset is complete.

The encoding of boot configuration vector is described in Table 2, and the vector input is illustrated in Figure 6.

Logic Diagram

The following Logic Diagram shows the primary pin functions of the RC32351.

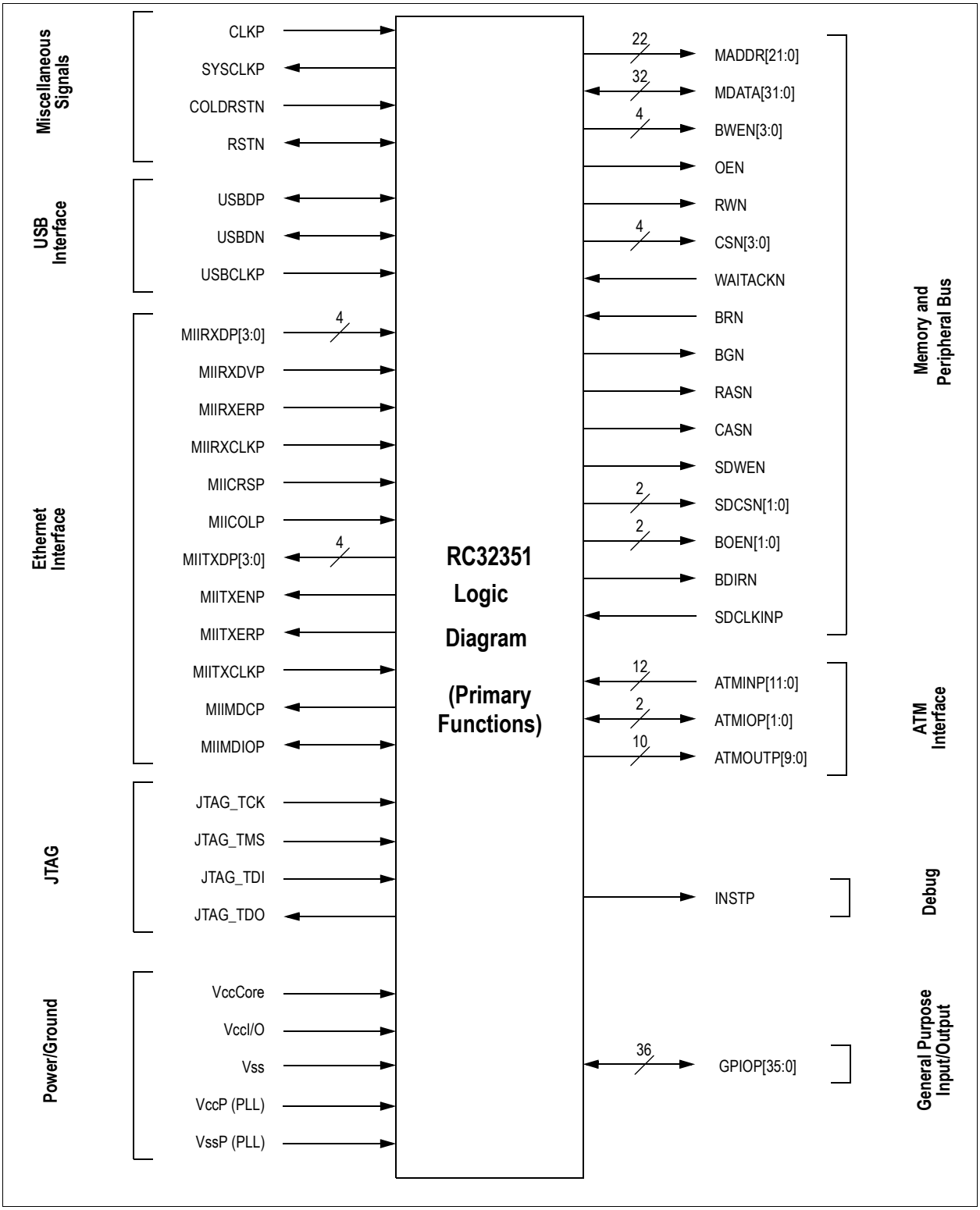


Figure 3 Logic Diagram

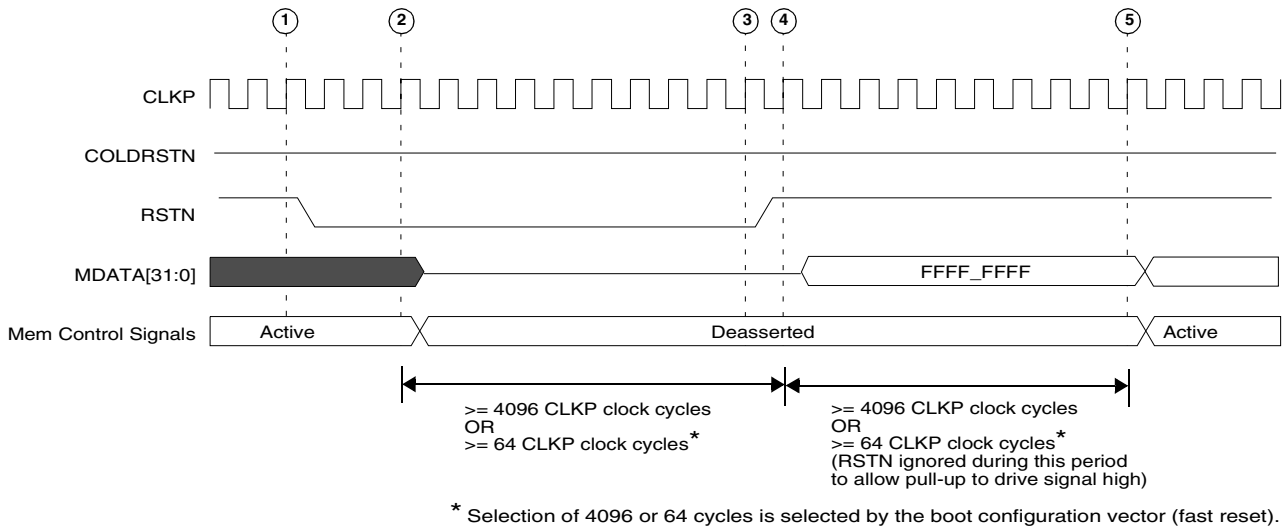
AC Timing Characteristics

(Ta = 0°C to +70°C Commercial, Vcc I/O = +3.3V±5%,V_{cc} Core = +2.5V±5%, V_{cc}P = +2.5V±5%)

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
Reset and System									
COLDRSTN	Tpw1	none	110	—	110	—	ms		Figure 6 Figure 7
	Trise1	none	—	5.0	—	5.0	ns		
RSTN[1]	Tdo2	CLKP rising	4.0	10.7	4.0	10.7	ns		
MDATA[15:0] Boot Configuration Vector	Thld3	COLDRSTN rising	3	—	3	—	ns		
INSTP	Tdo	CLKP rising	5	8	5.0	8.0	ns		
CPUP	Tdo	CLKP rising	3.5	7	3.5	7.0	ns		
DMAP	Tdo	CLKP rising	3.5	6.6	3.5	6.6	ns		
DMAREQN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	ns		
DMADONEN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	ns		
DMAFIN	Tdo	CLKP rising	3.5	5.9	3.5	5.9	ns		
BRN	Tsu	CLKP rising	1.6	—	1.6	—	ns		
	Thld		0	—	0	—	ns		
BGN	Tdo	CLKP rising	3.3	5.8	3.3	5.8	ns		

[1] RSTN is a bidirectional signal. It is treated as an asynchronous input.
[2] DMAREQN and DMADONEN minimum pulse width equals the CLKP period plus 7ns.

Table 5 Reset and System AC Timing Characteristics



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32351 asserts RSTN output low in response.
2. The RC32351 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32351 deasserts RSTN.
4. The RC32351 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 7 Warm Reset AC Timing Waveform

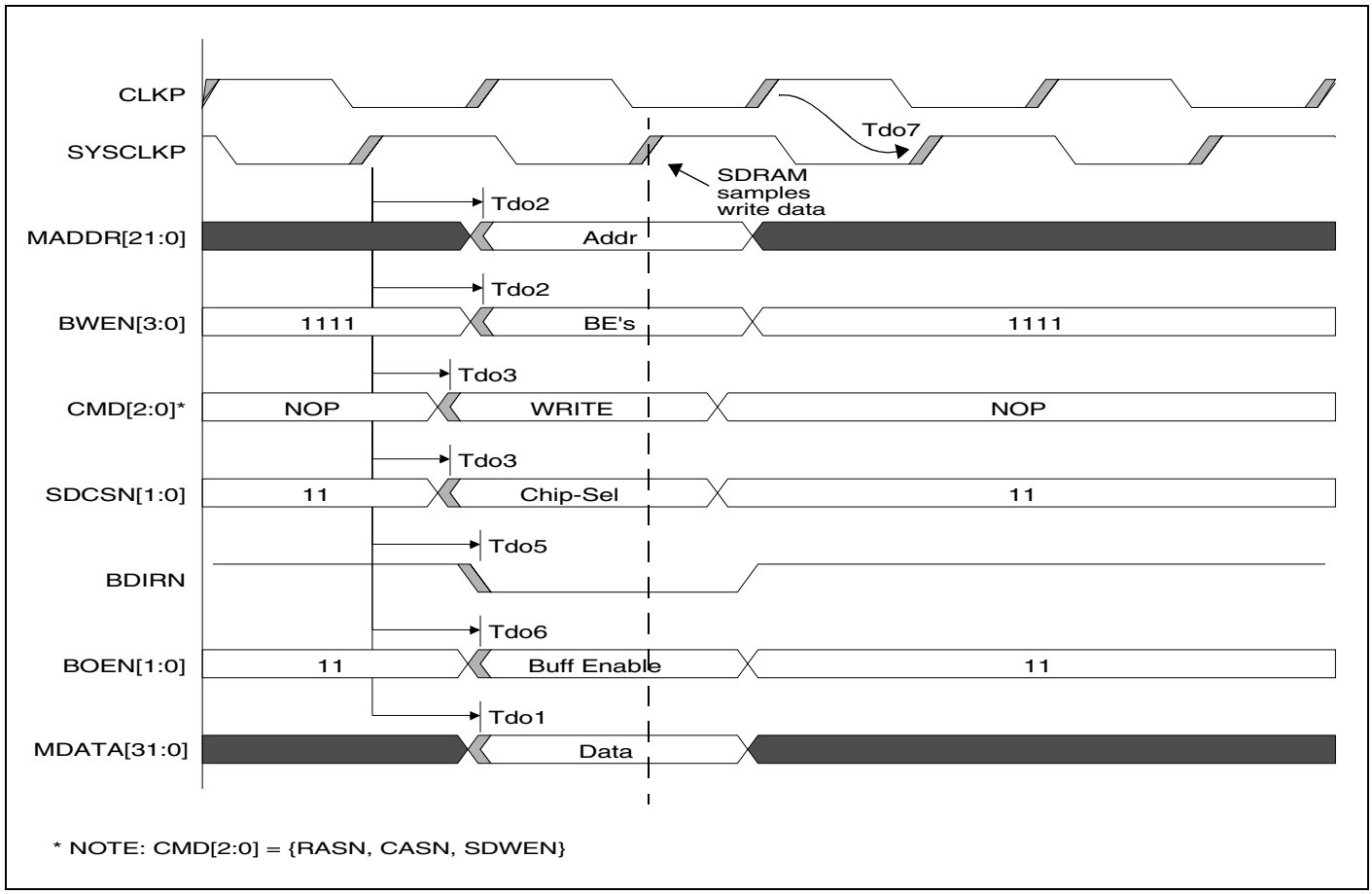


Figure 10 Memory and Peripheral Bus AC Timing Waveform - SDRAM Write Access

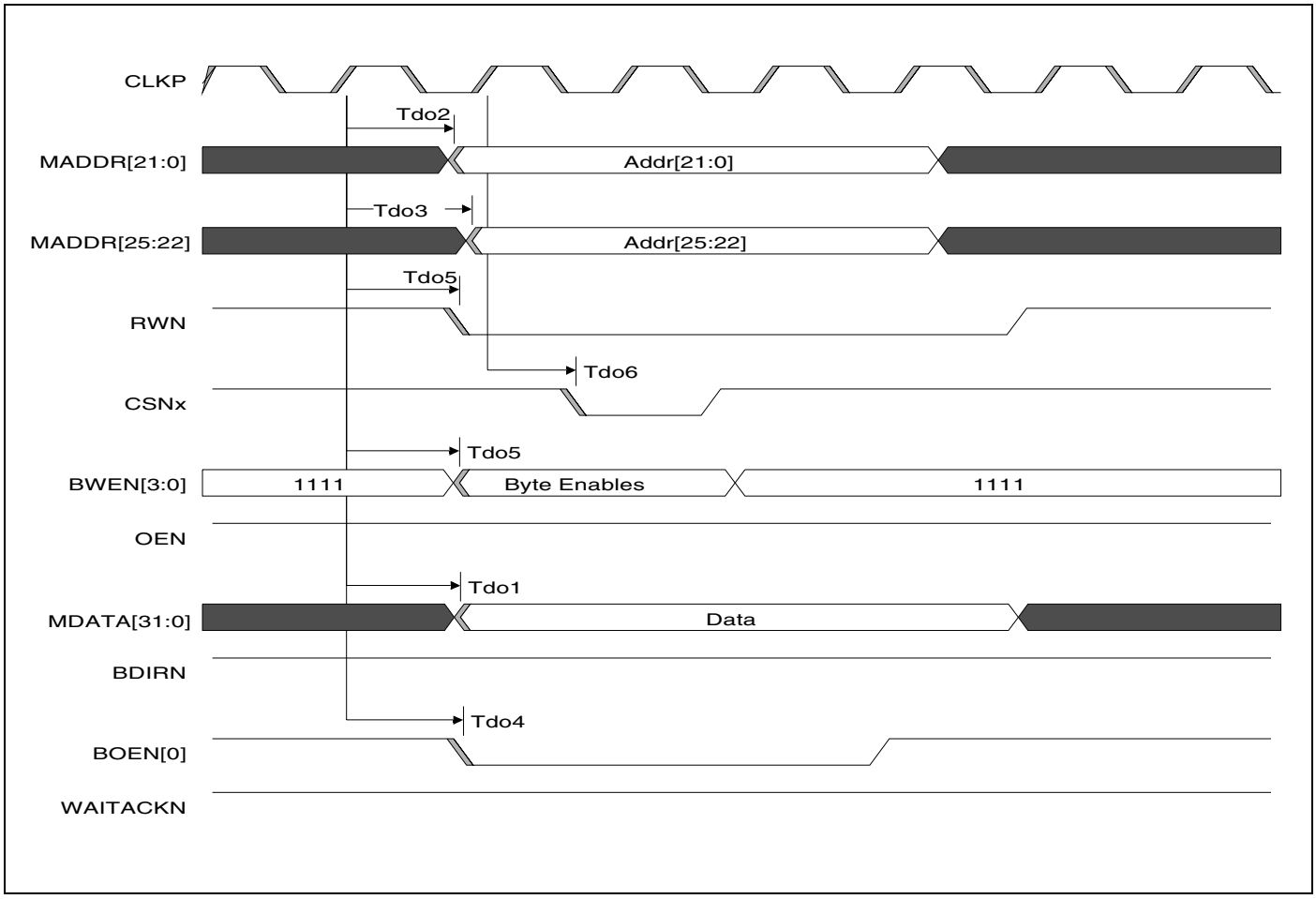


Figure 12 Memory AC and Peripheral Bus Timing Waveform - Device Write Access

ATM Pin Name	Utopia Level 1	Utopia Level 2
ATMINP[0]	RXDATA[0]	RXDATA[0]
ATMINP[1]	RXDATA[1]	RXDATA[1]
ATMINP[2]	RXDATA[2]	RXDATA[2]
ATMINP[3]	RXDATA[3]	RXDATA[3]
ATMINP[4]	RXDATA[4]	RXDATA[4]
ATMINP[5]	RXDATA[5]	RXDATA[5]
ATMINP[6]	RXDATA[6]	RXDATA[6]
ATMINP[7]	RXDATA[7]	RXDATA[7]
ATMINP[8]	RXCLKP	RXCLKP
ATMINP[9]	RXEMPTYN	RXEMPTYN
ATMINP[10]	RXSOC	RXSOC
ATMINP[11]	TXFULLN	TXFULLN
ATMIOP[0]	RXENBN	RXENBN
ATMIOP[1]	TXCLKP	TXCLKP
ATMOUTP[0]	TXDATA[0]	TXDATA[0]
ATMOUTP[1]	TXDATA[1]	TXDATA[1]
ATMOUTP[2]	TXDATA[2]	TXDATA[2]
ATMOUTP[3]	TXDATA[3]	TXDATA[3]
ATMOUTP[4]	TXDATA[4]	TXDATA[4]
ATMOUTP[5]	TXDATA[5]	TXDATA[5]
ATMOUTP[6]	TXDATA[6]	TXDATA[6]
ATMOUTP[7]	TXDATA[7]	TXDATA[7]
ATMOUTP[8]	TXSOC	TXSOC
ATMOUTP[9]	TXENBN	TXENBN
GPIOP[22]		TXADDR[0]
GPIOP[23]		TXADDR[1]
GPIOP[24]		RXADDR[0]
GPIOP[25]		RXADDR[1]

Table 9 ATM I/O Pin Description

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
USB									
USBCLKP[1]	Tperiod1	none	19.79	21.87	19.79	21.87	ns		Figure 15
	Thigh1,Tlow1		8.3	—	8.3	—	ns		
	Trise1,Tfall1		—	3	—	3	ns		
	Tjitter1		—	0.8	—	0.8	ns	1/4th of the minimum Source data jitter	
USBDN, USBDP	Trise2		4	20	4	20	ns	Universal Serial Bus Specification (USBS) Revision 1.1: Figures 7.6 and 7.7.	
	Tfall2		4	20	4	20	ns	USBS Revision 1.1: Figures 7.6 and 7.7.	
USBDN and USBDP Rise and Fall Time Matching			90	111.11	90	111.11	%	USBS Revision 1.1: Note 10, Section 7.1.2.	
Data valid period	Tstate		60	—	60	—	ns		
Skew between USBDN and USBDP			—	0.4	—	0.4	ns	USBS Revision 1.1: Section 7.1.3	
Source data jitter			—	3.5	—	3.5	ns	USBS Revision 1.1: Table 7-6	
Receive data jitter			—	12	—	12	ns		
Source EOP length	Tseop		160	175	160	175	ns		
Receive EOP length	Treop		82	—	82	—	ns		
EOP jitter			-2	5	-2	5	ns		
Full-speed Data Rate	Tfdrate		11.97	12.03	11.97	12.03	MHz	Average bit rate, USBS Section 7.1.11.	
Frame Interval			0.9995	1.0005	0.9995	1.0005	ms	USBS Section 7.1.12.	
Consecutive Frame Interval Jitter			—	42	—	42	ns	Without frame adjustment.	
			—	126	—	126	ns	With frame adjustment.	

[1] USB clock (USBCLKP) frequency must be less than CLKP frequency.

Table 10 USB AC Timing Characteristics

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
EJTAG and JTAG									
JTAG_TCK	Tperiod1	none	100	—	100	—	ns		Figure 17
	Thigh1,Tlow1		40	—	40	—	ns		
	Trise1,Tfall1		—	5	—	5	ns		
EJTAG_DCLK[1]	Tperiod2	none	10.0	10.0	7.5	10.0	ns		
	Thigh2,Tlow2		2.5	—	2.5	—	ns		
	Trise2,Tfall2		—	3.5	—	3.5	ns		
JTAG_TMS, JTAG_TDI, JTAG_TRST_N	Tsu3	JTAG_TCK rising	3.0	—	3.0	—	ns		
	Thld3		1.0	—	1.0	—	ns		
JTAG_TDO	Tdo4	JTAG_TCK falling	2.0	12.0	2.0	12.0	ns		
	Tdo5	EJTAG_DCLK rising	-0.7[2]	1.0	-0.7[2]	1.0	ns		
JTAG_TRST_N	Tpw6	none	100	—	100	—	ns		
	Tsu6	JTAG_TCK rising	2	—	2	—	ns		
EJTAG_PCST[2:0]	Tdo7	EJTAG_DCLK rising	-0.3[2]	3.3	-0.3[2]	3.3	ns		

1. EJTAG_DCLK is equal to the internal CPU pipeline clock.

2. A negative delay denotes the amount of time before the reference clock edge.

Table 13 JTAG AC Timing Characteristics

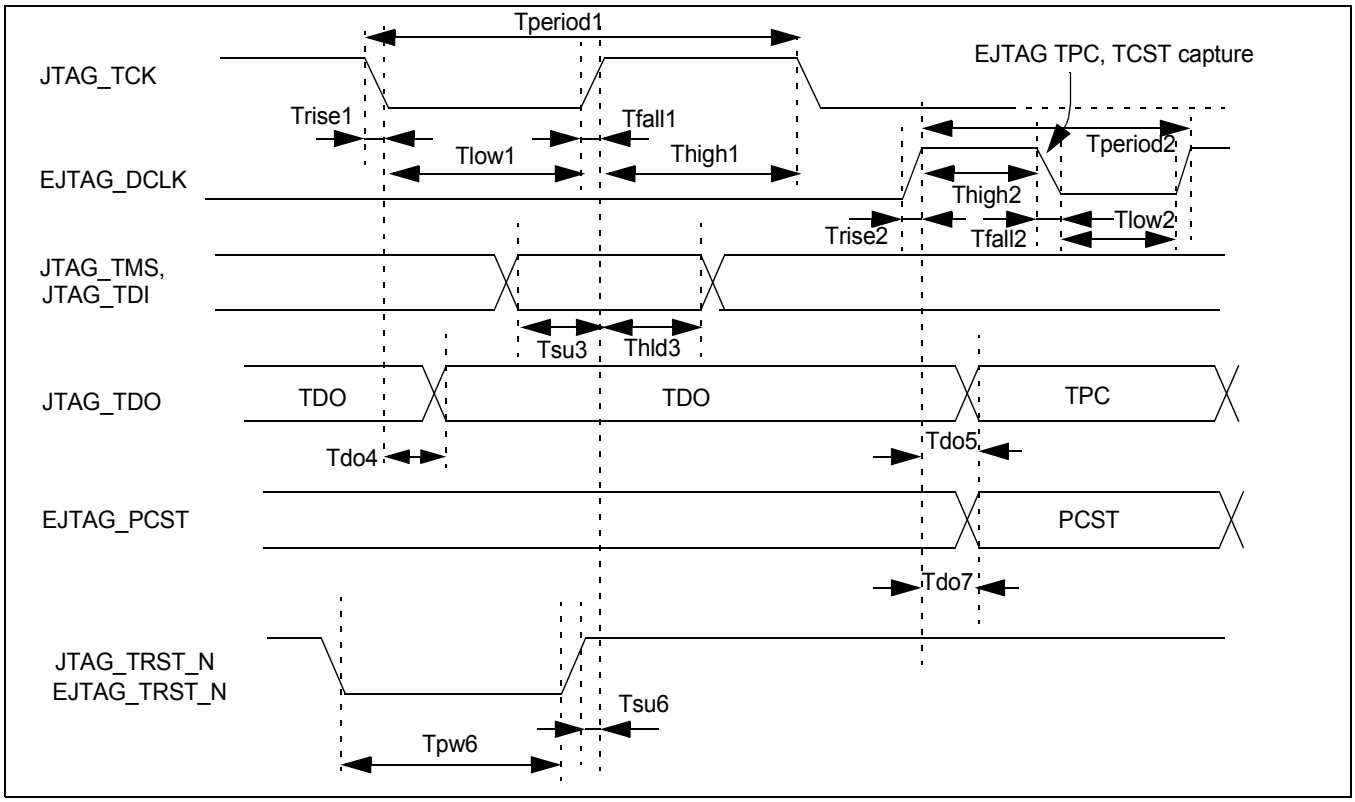


Figure 17 JTAG AC Timing Waveform

Power-on RampUp

The 2.5V core supply (and 2.5V V_{cc}PLL supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

DC Electrical Characteristics

($T_{ambient}$ = 0°C to +70°C Commercial, Vcc I/O = +3.3V±5%, V_{cc} Core and V_{cc} P = +2.5V±5%)

	Parameter	Min	Max	Unit	Pin Numbers	Conditions
LOW Drive Output with Schmitt Trigger Input (STI)	I_{OL}	7.3	—	mA	1-4,6-8,10-16,18,20-25,27-29,32,33,35-37, 39-42,44,46-48,50,52,53,56,58-60,62-69, 71-77,82-85,87-94,96-99,101-105,167, 205-208	V_{OL} = 0.4V
	I_{OH}	-8.0	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
	V_{IL}	—	0.8	V		—
	V_{IH}	2.0	(V_{cc}I/O + 0.5)	V		—
	V_{OH}	V_{cc} - 0.4	—	V		—
HIGH Drive Output with Standard Input	I_{OL}	9.4	—	mA	49,51,54,55,106-108,110,112-117,119, 121,123-128,130,132-137,139,141,143, 150,152,154-159,161,163-166,168-170, 172,174-179,181,185-190,192,194-200, 202,204	V_{OL} = 0.4V
	I_{OH}	-15	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
	V_{IL}	—	0.8	V		—
	V_{IH}	2.0	(V_{cc}I/O + 0.5)	V		—
	V_{OH}	V_{cc} - 0.4	—	V		—
Clock Drive Output	I_{OL}	39	—	mA	183	V_{OL} = 0.4V
	I_{OH}	-24	—	mA		V_{OH} = (V_{cc} I/O - 0.4)
Capacitance	C_{IN}	—	10	pF	All pins	—
Leakage	I/O_{LEAK}	—	20	µA	All pins	—

Table 16 DC Electrical Characteristics

Power Curve

The following graph contains a power curve that shows power consumption at various bus frequencies.

Note: The system clock (CLKP) can be multiplied by 2, 3, or 4 to obtain the CPU pipeline clock (PClock) speed.

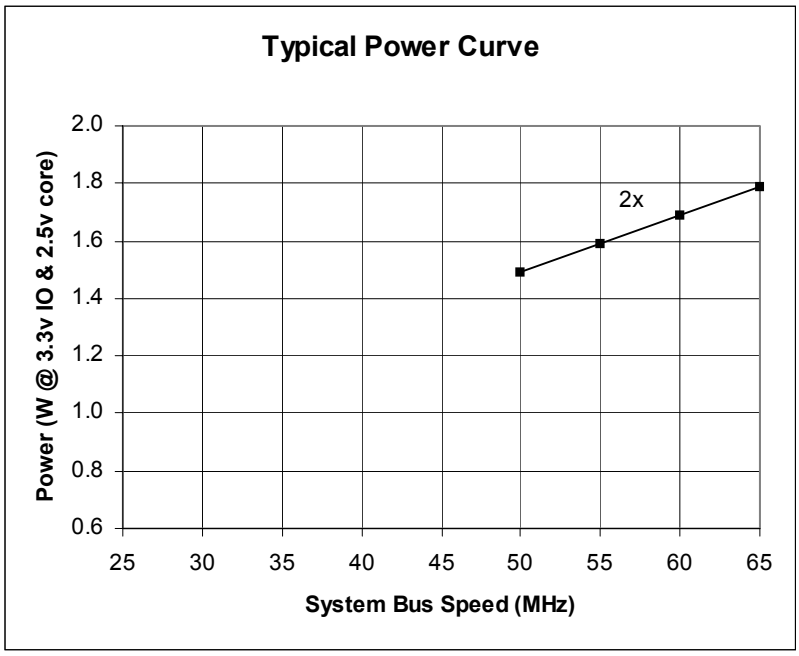


Figure 20 Typical Power Usage

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O Supply Voltage	-0.3	4.0	V
V_{CC}Core	Core Supply Voltage	-0.3	3.0	V
V_{CC}P	PLL Supply Voltage	-0.3	3.0	V
Vimin	Input Voltage - undershoot	-0.6	—	V
Vi	I/O Input Voltage	Gnd	V_{CC}I/O+0.5	V
Ta, Commercial	Ambient Operating Temperature	0	70	degrees C
Tstg	Storage Temperature	-40	125	degrees C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

Package Pin-out — 208-Pin PQFP

The following table lists the pin numbers and signal names for the RC32351.

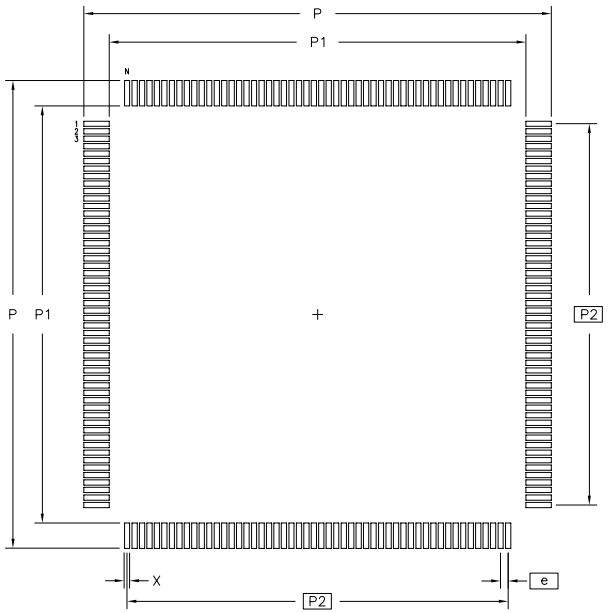
Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	ATMOUTP[0]		53	JTAG_TDO		105	BGN		157	MDATA[28]	
2	ATMOUTP[1]		54	GPIOP[16]	1	106	CSN[0]		158	MDATA[13]	
3	ATMINP[02]		55	GPIOP[17]	1	107	CSN[1]		159	MDATA[29]	
4	ATMOUTP[2]		56	GPIOP[18]	1	108	CSN[2]		160	Vcc I/O	
5	Vss		57	Vss		109	Vcc I/O		161	MDATA[14]	
6	ATMOUTP[3]		58	JTAG_TCK		110	CSN[3]		162	Vss	
7	ATMINP[03]		59	GPIOP[19]	1	111	Vss		163	MDATA[30]	
8	ATMOUTP[4]		60	GPIOP[20]	1	112	OEN		164	MDATA[15]	
9	Vcc I/O		61	Vcc I/O		113	RWN		165	MDATA[31]	
10	ATMOUTP[5]		62	GPIOP[21]	1	114	BDIRN		166	CLKP	
11	ATMINP[04]		63	JTAG_TDI		115	BOEN[0]		167	WAITACKN	
12	ATMOUTP[6]		64	GPIOP[22]	1	116	BOEN[1]		168	MADDR[00]	
13	ATMOUTP[7]		65	GPIOP[23]	2	117	BWEN[0]		169	MADDR[11]	
14	ATMINP[05]		66	GPIOP[24]	1	118	Vcc I/O		170	MADDR[01]	
15	ATMOUTP[8]		67	JTAG_TMS		119	BWEN[1]		171	Vcc I/O	
16	ATMOUTP[9]		68	GPIOP[25]	2	120	Vss		172	MADDR[12]	
17	Vss		69	GPIOP[26]		121	BWEN[2]		173	Vss	
18	ATMINP[06]		70	Vss		122	Vcc Core		174	MADDR[02]	
19	Vcc Core		71	GPIOP[27]	1	123	BWEN[3]		175	MADDR[13]	
20	GPIOP[00]	1	72	COLDRSTN		124	MDATA[00]		176	MADDR[03]	
21	GPIOP[01]	1	73	GPIOP[28]	1	125	MDATA[16]		177	MADDR[14]	
22	ATMINP[07]		74	GPIOP[29]	1	126	MDATA[01]		178	MADDR[04]	
23	GPIOP[02]	2	75	GPIOP[30]	1	127	MDATA[17]		179	MADDR[15]	
24	GPIOP[03]	1	76	GPIOP[31]	2	128	MDATA[02]		180	Vcc I/O	
25	ATMINP[08]		77	USBCLKP		129	Vcc I/O		181	MADDR[05]	
26	Vcc I/O		78	Vcc I/O		130	MDATA[18]		182	Vcc Core	
27	GPIOP[04]	2	79	USBDN		131	Vss		183	SYSCLKP	
28	GPIOP[05]	1	80	USBDP		132	MDATA[03]		184	Vss	
29	ATMINP[09]		81	Vss		133	MDATA[19]		185	MADDR[16]	
30	VccP[1]		82	MIICRSP		134	MDATA[04]		186	MADDR[06]	
31	VssP[1]		83	MIICOLP		135	MDATA[20]		187	MADDR[17]	
32	ATMINP[10]		84	MIITXDP[0]		136	MDATA[05]		188	MADDR[07]	
33	GPIOP[06]	1	85	MIITXDP[1]		137	MDATA[21]		189	MADDR[18]	
34	Vss		86	Vcc Core		138	Vcc Core		190	MADDR[08]	
35	GPIOP[07]	1	87	MIITXDP[2]		139	MDATA[06]		191	Vcc I/O	
36	ATMINP [11]		88	MIITXDP[3]		140	Vcc I/O		192	MADDR[19]	
37	GPIOP[08]	2	89	MIITXENP		141	MDATA[22]		193	Vss	

Table 20: 208-pin QFP Package Pin-Out (Part 1 of 2)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
29253	00	INITIAL RELEASE	08/20/96	T. VU
61476	01	ADD "DH" PACKAGE OPTION	09/20/98	T. VU
61829	02	ADD "DR" PACKAGE OPTION	01/30/99	

SYMBOL	JEDEC VARIATION FA-1			NOTE
	MIN	NOM	MAX	
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.60	
D	30.60 BSC			4
D1	28.00 BSC			5,2
E	30.60 BSC			4
E1	28.00 BSC			5,2
N	208			
e	.50 BSC			
b	.17	–	.27	7
b1	.17	.20	.23	
ddd	–	–	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.20	31.40
P1	27.80	28.00
P2	25.50 BSC	
X	.30	.40
e	.50 BSC	
N	208	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE –C–
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–143, VARIATION FA–1

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727–6116
FAX: (408) 492–8674 TWX: 910–338–2070

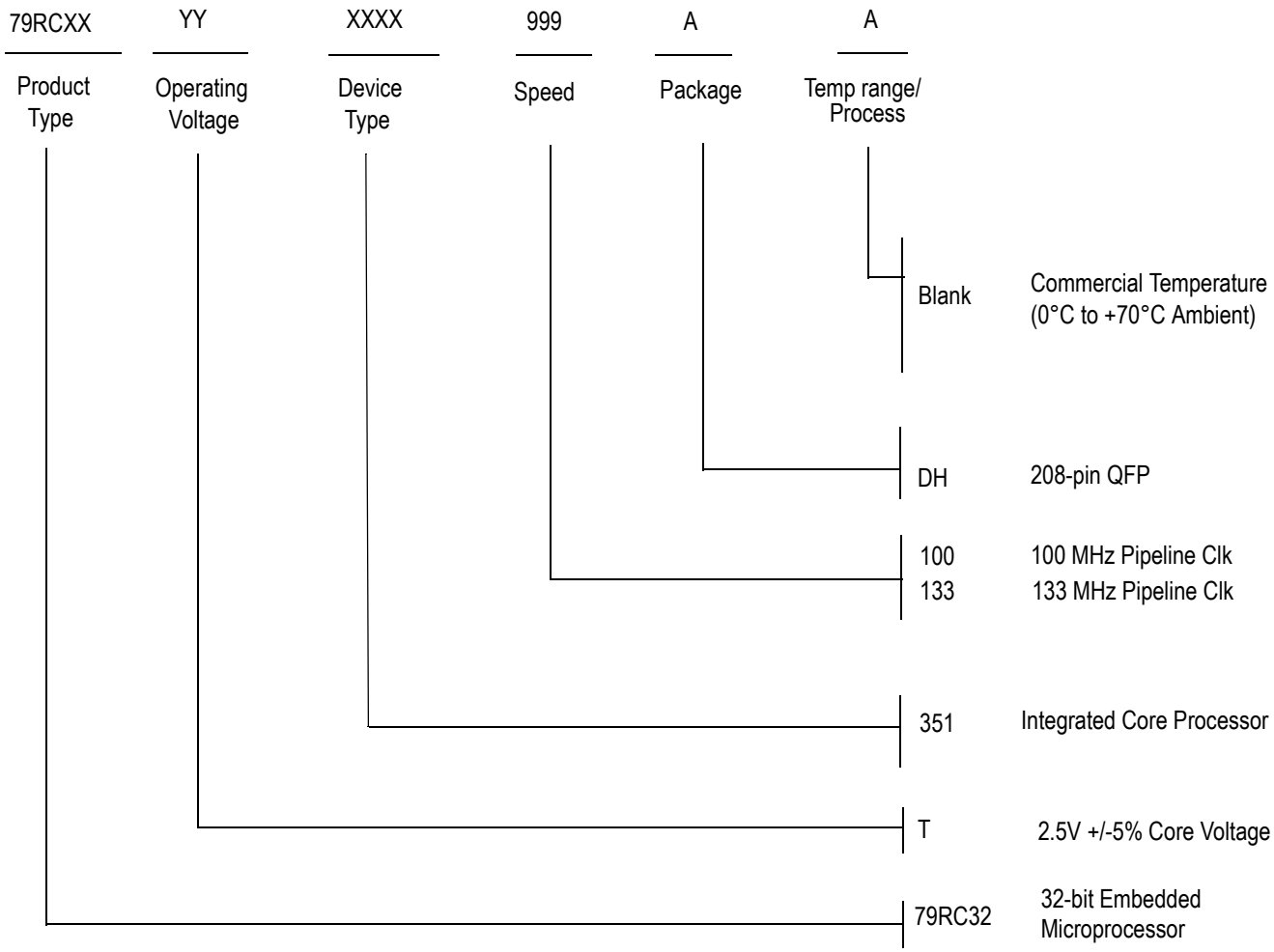
APPROVALS	DATE
DRAWN TV	08/20/96
CHECKED	

TITLE: DS/DH/DR PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.30/.25 MIN FORM

SIZE	DRAWING No.	REV
C	PSC–4059	02

DO NOT SCALE DRAWING — SHEET 2 OF 2

Ordering Information



Valid Combinations

79RC32T351 -100DH	208-pin QFP package, Commercial Temperature
79RC32T351 -133DH	208-pin QFP package, Commercial Temperature

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