Renesas Electronics America Inc - IDT79RC32T351-133DH Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t351-133dh

- *Supports burst transfers*

◆ **USB**
- *Revision 1.1 compliant*
- *USB slave device controller*
- *Supports a 6th USB endpoint*
- *Full speed operation at 12 Mb/s*
- *Supports control, interrupt, bulk and isochronous endpoints*
- *Supports USB remote wakeup*
- *Integrated USB transceiver*

◆ **EJTAG**
- *Run-time Mode provides a standard JTAG interface*
- *Real-Time Mode provides additional pins for real-time trace information*

◆ **Ethernet**
- *Full duplex support for 10 and 100 Mb/s Ethernet*
- *IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface*
- *IEEE 802.3u auto-negotiation for automatic speed selection*
- *Flexible address filtering modes*
- *64-entry hash table based multicast address filtering*

◆ **ATM SAR**
- *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
- *Supports 25Mb/s and faster ATM*
- *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
- *Supports standard 53-byte ATM cells*
- *Performs HEC generation and checking*
- *Cell processing discards short cells and clips long cells*
- *16 cells worth of buffering*
- *UTOPIA modes: 8 cell input buffer and 8 cell output buffer*
- *Hardware support for CRC-32 generation and checking for AAL5*
- *Hardware support for CRC-10 generation and checking*
- *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
- *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention*

◆ **System Features**
- *JTAG interface (IEEE Std. 1149.1 compatible)*
- *208 pin PQFP package*
- *2.5V core supply and 3.3V I/O supply*
- *Up to 133 MHz pipeline frequency and up to 66 MHz bus frequency*

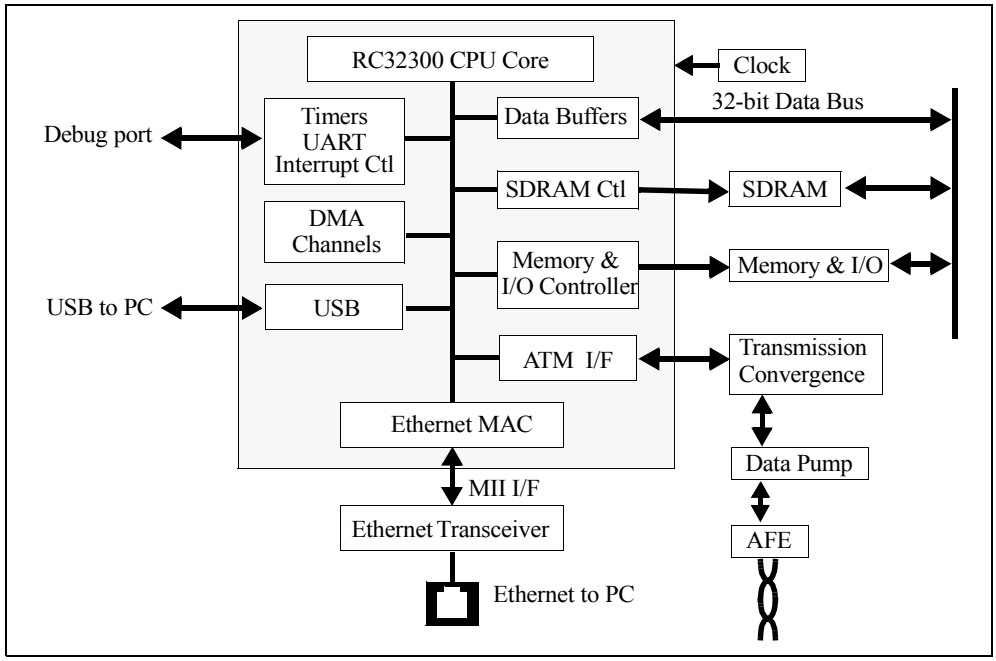


Figure 2 Example of xDSL Residential Gateway Using RC32351

Name	Type	I/O Type	Description
RWN	O	High Drive	**Read or Write.** This signal indicates if the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device, a low level indicates a write to an external device.
OEN	O	High Drive	**Output Enable.** This signal is asserted low when data should be driven by an external device during device read transactions on the memory and peripheral bus.
BWEN[3:0]	O	High Drive	**SDRAM Byte Enable Mask or Memory and I/O Byte Write Enables.** These signals are used as data input/output masks during SDRAM transactions and as byte write enable signals during device controller transactions on the memory and peripheral bus. They are active low. BWEN[0] corresponds to byte lane MDATA[7:0]. BWEN[1] corresponds to byte lane MDATA[15:8]. BWEN[2] corresponds to byte lane MDATA[23:16]. BWEN[3] corresponds to byte lane MDATA[31:24].
SDCSN[1:0]	O	High Drive	**SDRAM Chip Select.** These signals are used to select the SDRAM device on the memory and peripheral bus. Each bit is asserted low during an access to the selected SDRAM.
RASN	O	High Drive	**SDRAM Row Address Strobe**. The row address strobe asserted low during memory and peripheral bus SDRAM transactions.
CASN	O	High Drive	**SDRAM Column Address Strobe.** The column address strobe asserted low during memory and peripheral bus SDRAM transactions.
SDWEN	O	High Drive	**SDRAM Write Enable.** Asserted low during memory and peripheral bus SDRAM write transactions.
CKENP	O	Low Drive	**SDRAM Clock Enable.** Asserted high during active SDRAM clock cycles. Primary function: General Purpose I/O, GPIOP[21].
SDCLKINP	I	STI	**SDRAM Clock Input.** This clock input is a delayed version of SYSCLKP. SDRAM read data is sampled into the RC32351 on the rising edge of this clock.
ATM Interface			
ATMINP[11:0]	I	STI	**ATM PHY Inputs.** These pins are the inputs for the ATM interface.
ATMIOP[1:0]	I/O	Low Drive with STI	**ATM PHY Bidirectional Signals.** These pins are the bidirectional pins for the ATM interface.
ATMOUTP[9:0]	O	Low Drive	**ATM PHY Outputs.** These pins are the outputs for the ATM interface.
TXADDR[1:0]	O	Low Drive	**ATM Transmit Address [1:0]**. 2-bit address bus used for transmission in Utopia-2 mode. TXADDR[0] Primary function: General purpose I/O, GPIOP[22]. TXADDR[1] Primary function: General purpose I/O, GPIOP[23].
RXADDR[1:0]	O	Low Drive	**ATM Receive Address [1:0]**. 2-bit address bus for receiving in Utopia-2 mode. RXADDR[0] Primary function: General purpose I/O, GPIOP[24]. RXADDR[1] Primary function: General purpose I/O, GPIOP[25].
General Purpose Input/Output			
GPIOP[0]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial output, U0SOUTP.
GPIOP[1]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial input, U0SINP.
GPIOP[2]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 ring indicator, U0RIN. 2nd Alternate function: JTAG boundary scan tap controller reset, JTAG_TRST_N.
GPIOP[3]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data carrier detect, U0DCRN.
GPIOP[4]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 data terminal ready, U0DTRN. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.

Table 1 Pin Descriptions (Part 2 of 7)

Name	Type	I/O Type	Description
MIIMDIOP	I/O	Low Drive with STI	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
MIIRXCLKP	I	STI	**MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data.
MIIRXDP[3:0]	I	STI	**MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY.
MIIRXDVP	I	STI	**MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MIIRXERP	I	STI	**MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MIITXCLKP	I	STI	**MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MIITXDP[3:0]	O	Low Drive	**MII Transmit Data.** This nibble wide data bus contains the data to be transmitted.
MIITXENP	O	Low Drive	**MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission.
MIITXERP	O	Low Drive	**MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
EJTAG			
JTAG_TCK	I	STI	**JTAG Clock.** This is an input test clock, used to shift data into or out of the boundary scan logic. This signal requires an external resistor, listed in Table 14.
JTAG_TDI	I	STI	**JTAG Data Input.** This is the serial data shifted into the boundary scan logic. This signal requires an external resistor, listed in Table 14. This is also used to input EJTAG_DINTN during EJTAG/ICE mode. EJTAG_DINTN is an interrupt to switch the PC trace mode off.
JTAG_TDO	O	Low Drive	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic. When no data is being shifted out, this signal is tri-stated. This signal requires an external resistor, listed in Table 14. This is also used to output the EJTAG_TPC during EJTAG/ICE mode. EJTAG_TPC is the non-sequential program counter output.
JTAG_TMS	I	STI	**JTAG Mode Select**. This input signal is decoded by the tap controller to control test operation. This signal requires an external resistor, listed in Table 14.
EJTAG_PCST[0]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[10]. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN.
EJTAG_PCST[1]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11]. 1st Alternate function: UART channel 1 data set ready, U1DSRN.
EJTAG_PCST[2]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[12]. 1st Alternate function: UART channel 1 request to send, U1RTSN.
EJTAG_DCLK	O	Low Drive	**PC trace clock.** This is used to capture address and data during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[13]. 1st Alternate function: UART channel 1 clear to send, U1CTSN.

Table 1 Pin Descriptions (Part 5 of 7)

Logic Diagram

The following Logic Diagram shows the primary pin functions of the RC32351.

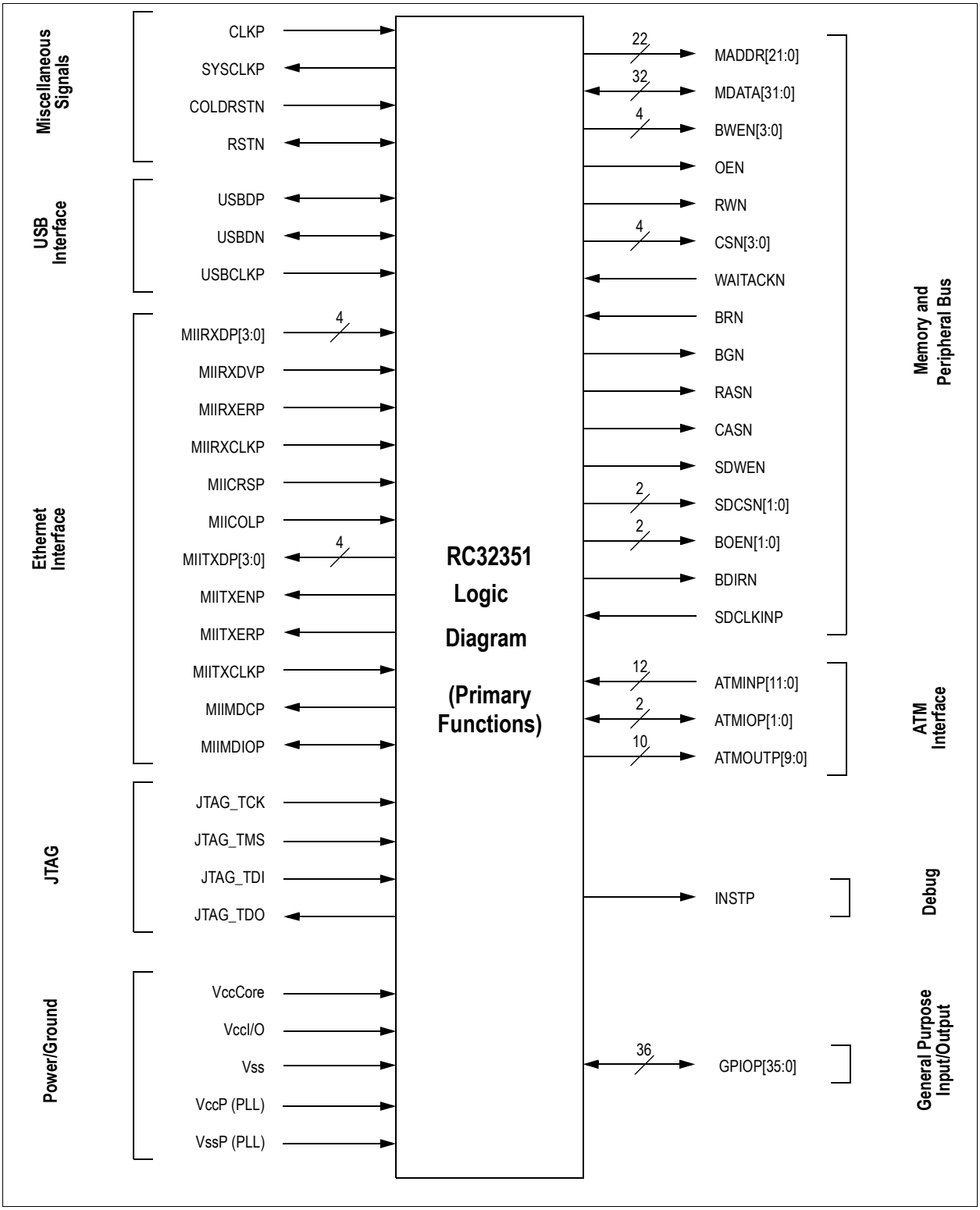


Figure 3 Logic Diagram

Clock Parameters

(Ta = 0°C to +70°C Commercial, Vcc I/O = +3.3V±5%, V_{cc} Core and $V_{cc}P$ = +2.5V±5%)

Parameter	Symbol	Reference Edge	RC32351 100MHz		RC32351 133MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max		
Internal CPU pipeline clock[1]	Frequency	none	100	100	100	133	MHz	Figure 4
CLKP[2,3,4]	Frequency	none	25	50	25	67	MHz	
	Tperiod1		20	40	15	40	ns	
	Thigh1		10	—	6	—	ns	
	Tlow1		10	—	6	—	ns	
	Trise1		—	3	—	3	ns	
	Tfall1		—	3	—	3	ns	
	Tjitter		—	±250	—	±250	ps	

[1] The CPU pipeline clock speed is selected during cold reset by the boot configuration vector (see Table 2).
[2] Ethernet clock (MIIRXCLKP and MIITXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.
[3] USB clock (USBCLKP) frequency must be less than CLKP frequency.
[4] ATM Utopia clock (RXCLKP and TXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.

Table 3 Clock Parameters

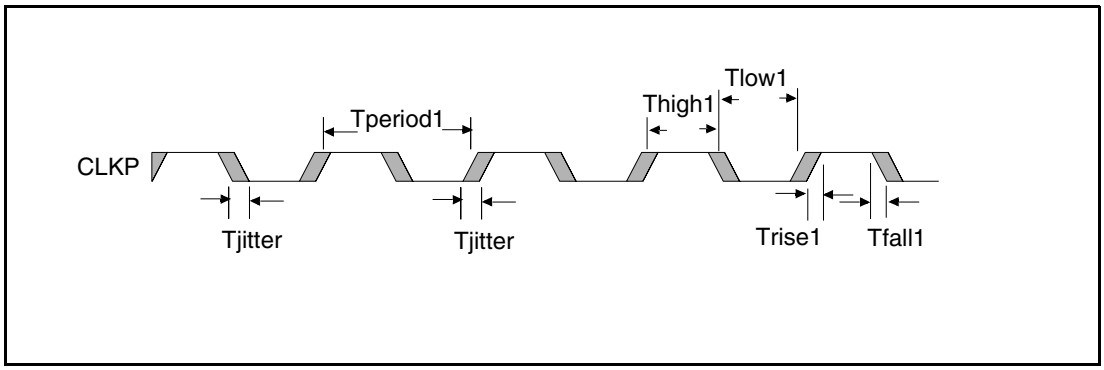


Figure 4 Clock Parameters Waveform

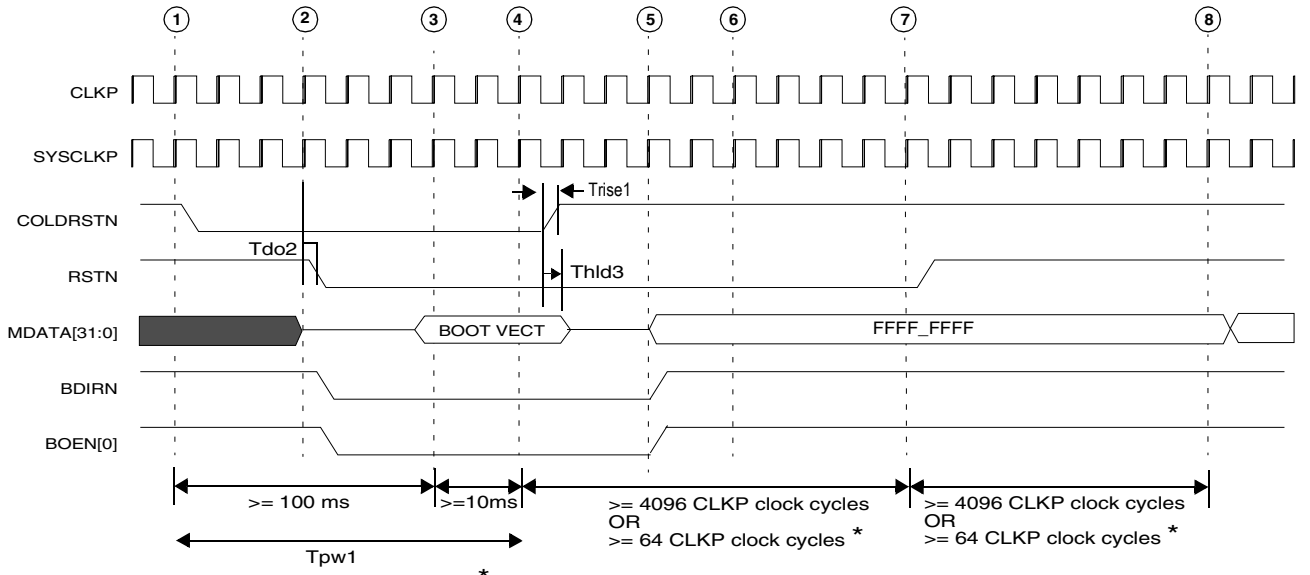
AC Timing Characteristics

(Ta = 0°C to +70°C Commercial, Vcc I/O = +3.3V±5%,V_{cc} Core = +2.5V±5%, V_{cc}P = +2.5V±5%)

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
Reset and System									
COLDRSTN	Tpw1	none	110	—	110	—	ms		Figure 6 Figure 7
	Trise1	none	—	5.0	—	5.0	ns		
RSTN[1]	Tdo2	CLKP rising	4.0	10.7	4.0	10.7	ns		
MDATA[15:0] Boot Configuration Vector	Thld3	COLDRSTN rising	3	—	3	—	ns		
INSTP	Tdo	CLKP rising	5	8	5.0	8.0	ns		
CPUP	Tdo	CLKP rising	3.5	7	3.5	7.0	ns		
DMAP	Tdo	CLKP rising	3.5	6.6	3.5	6.6	ns		
DMAREQN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	ns		
DMADONEN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	ns		
DMAFIN	Tdo	CLKP rising	3.5	5.9	3.5	5.9	ns		
BRN	Tsu	CLKP rising	1.6	—	1.6	—	ns		
	Thld		0	—	0	—	ns		
BGN	Tdo	CLKP rising	3.3	5.8	3.3	5.8	ns		

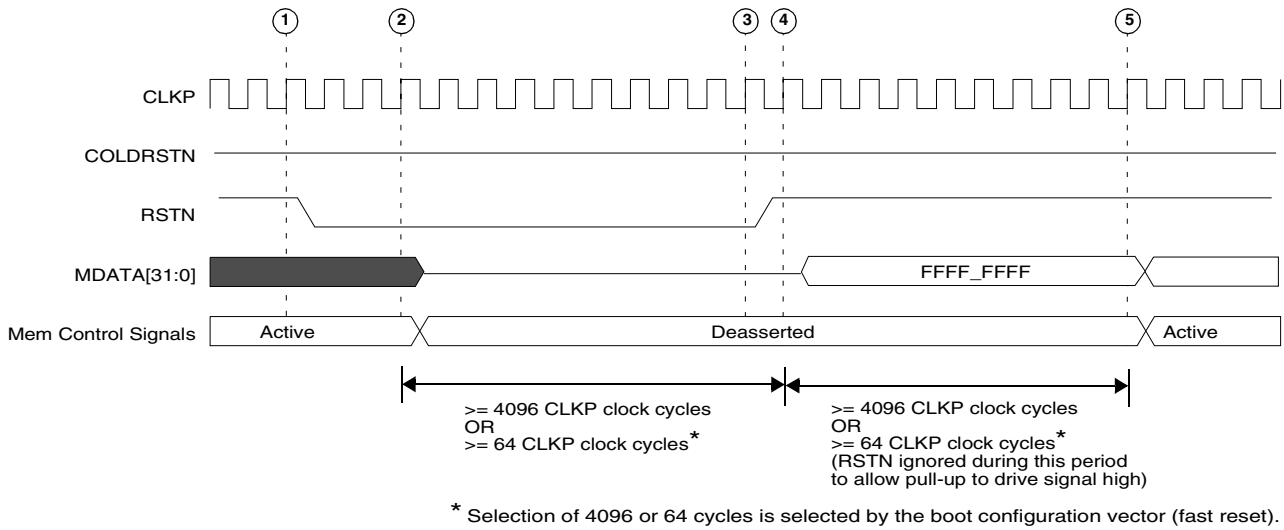
[1] RSTN is a bidirectional signal. It is treated as an asynchronous input.
[2] DMAREQN and DMADONEN minimum pulse width equals the CLKP period plus 7ns.

Table 5 Reset and System AC Timing Characteristics



1. COLDRSTN asserted by external logic.
2. The RC32351 asserts RSTN, asserts BOEN[0] low, drives BDIRN low, and tri-states the data bus in response.
3. External logic begins driving valid boot configuration vector on the data bus, and the RC32351 starts sampling it.
4. External logic negates COLDRSTN and tri-states the boot configuration vector on MDATA[15:0]. The boot configuration vector must not be tri-stated before COLDRSTN is deasserted. The RC32351 stops sampling the boot configuration vector.
5. The RC32351 starts driving the data bus, MDATA[31:0], deasserts BOEN[0] high, and drives BDIRN high.
6. SYSCLKP may be held constant after this point if Hold SYSCLKP Constant is selected in the boot configuration vector.
7. RSTN negated by RC32351.
8. CPU begins executing by taking MIPS reset exception, and the RC32351 starts sampling RSTN as a warm reset input.

Figure 6 Cold Reset AC Timing Waveform



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32351 asserts RSTN output low in response.
2. The RC32351 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32351 deasserts RSTN.
4. The RC32351 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 7 Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
Memory and Peripheral Bus - Device Access									
MDATA[31:0]	Tsu1	CLKP rising	2.5	—	2.5	—	ns		Figure 11 Figure 12
	Thld1		1.5	—	1.5	—	ns		
	Tdo1		2.0	6.5	2.0	6.5	ns		
	Tdz1		—	9.0	—	9.0	ns		
	Tzd1		2.0	—	2.0	—	ns		
WAITACKN, BRN	Tsu	CLKP rising	2.5	—	2.5	—	ns		
	Thld		1.5	—	1.5	—	ns		
MADDR[21:0]	Tdo2	CLKP rising	2.0	6.0	2.0	6.0	ns		
	Tdz2		—	9.0	—	9.0	ns		
	Tzd2		2.0	—	2.0	—	ns		
MADDR[25:22]	Tdo3	CLKP rising	2.5	6.5	2.5	6.5	ns		
	Tdz3		—	9.0	—	9.0	ns		
	Tzd3		2.0	—	2.0	—	ns		
BDIRN, BOEN[0]	Tdo4	CLKP rising	2.0	6.0	2.0	6.0	ns		
	Tdz4		—	9.0	—	9.0	ns		
	Tzd4		2.0	—	2.0	—	ns		
BGN, BWEN[3:0], OEN, RWN	Tdo5	CLKP rising	2.0	6.0	2.0	6.0	ns		
	Tdz5		—	9.0	—	9.0	ns		
	Tzd5		2.0	—	2.0	—	ns		
CSN[3:0]	Tdo6	CLKP rising	1.7	5.0	1.7	5.0	ns		
	Tdz6		—	9.0	—	9.0	ns		
	Tzd6		2.0	—	2.0	—	ns		
CSN[5:4]	Tdo7	CLKP rising	2.5	6.0	2.5	6.0	ns		
	Tdz7		—	9.0	—	9.0	ns		
	Tzd7		2.0	—	2.0	—	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

Note: The RC32351 provides bus turnaround cycles to prevent bus contention when going from a read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32351 are both driving. See Chapter 10, “Device Controller,” Chapter 11, “Synchronous DRAM Controller,” and Chapter 12, “Bus Arbitration” in the RC32351 User Reference Manual.

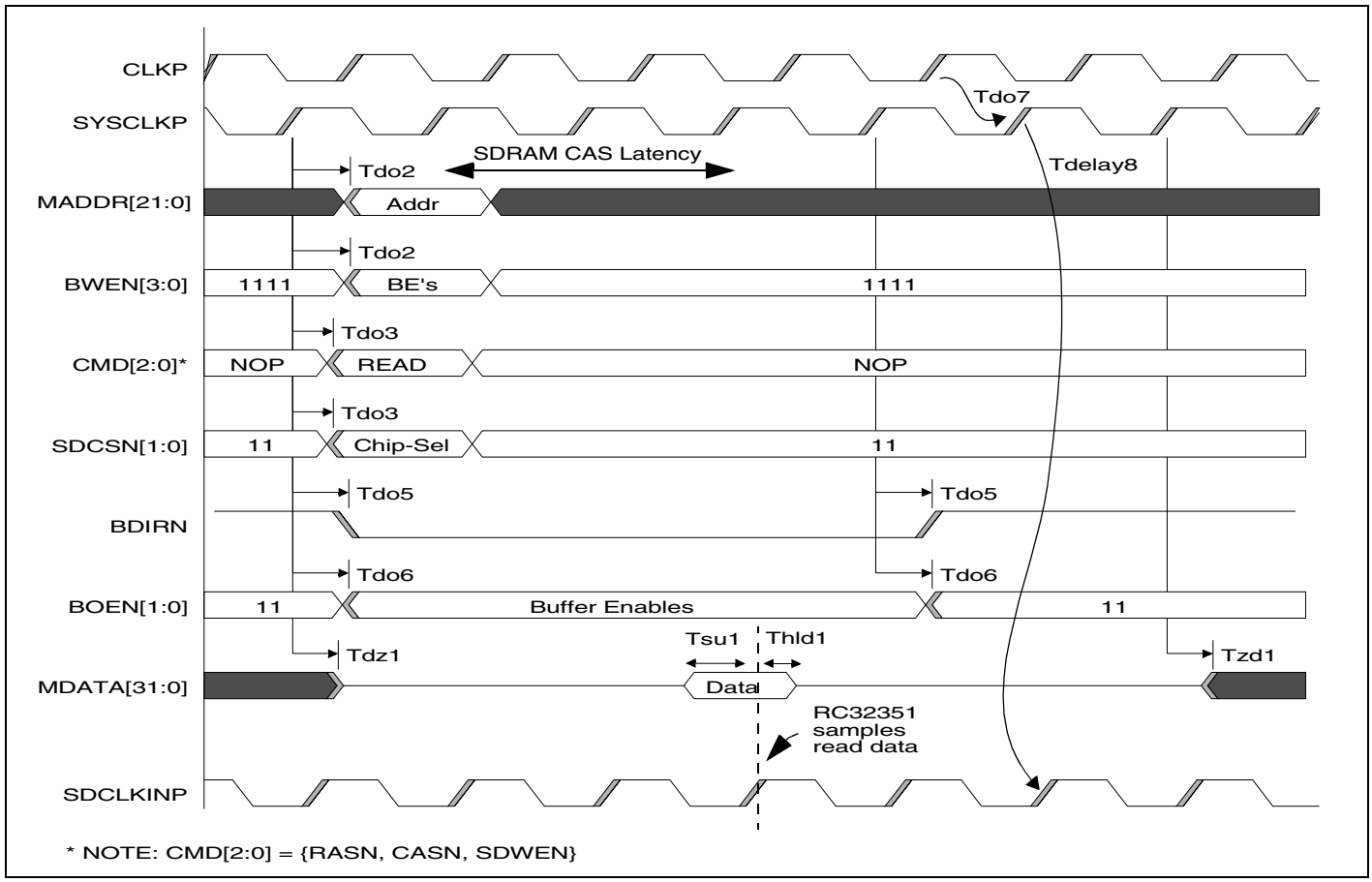


Figure 8 Memory and Peripheral Bus AC Timing Waveform - SDRAM Read Access

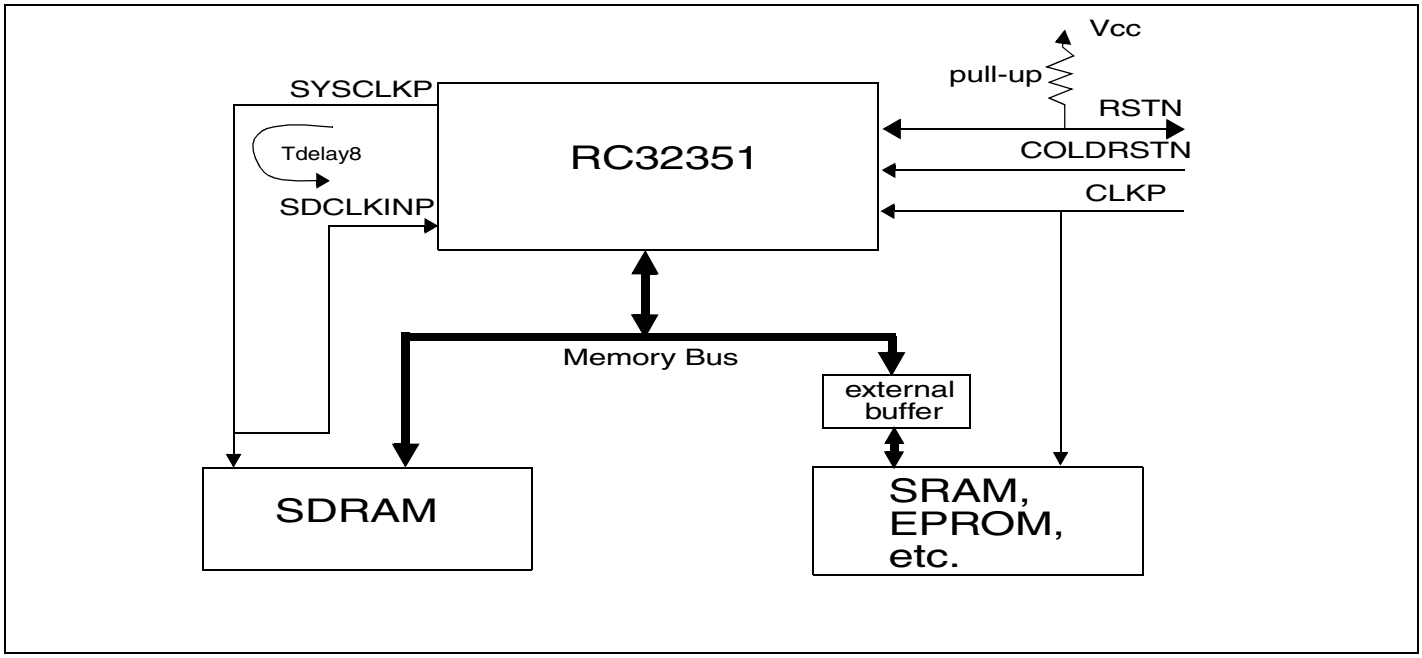


Figure 9 SYSCLKP - SDCLKINP Relationship

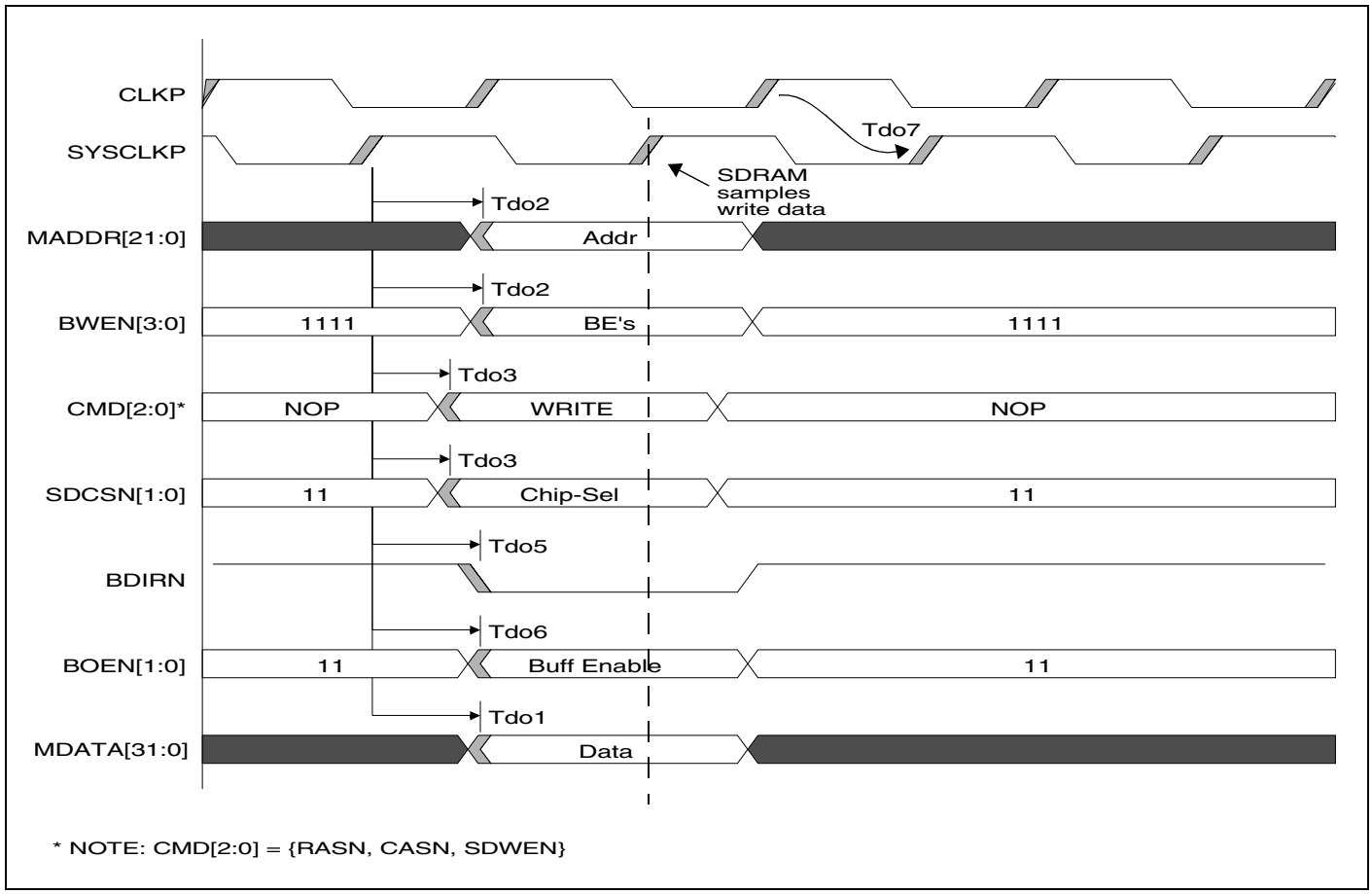


Figure 10 Memory and Peripheral Bus AC Timing Waveform - SDRAM Write Access

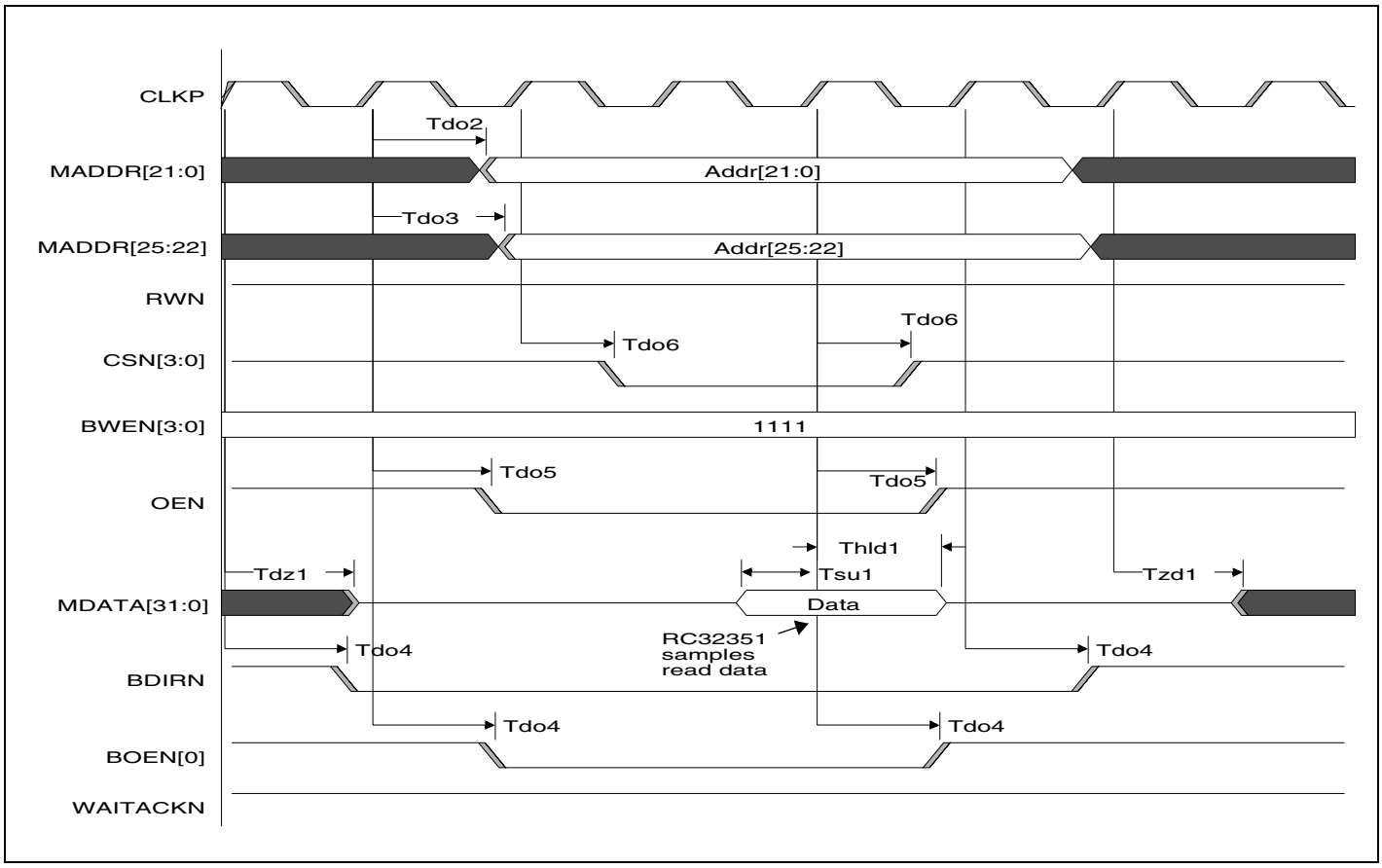


Figure 11 Memory and Peripheral Bus AC Timing Waveform - Device Read Access

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
Ethernet[1,2]									
MIIRXCLKP, MIITXCLKP	Tperiod1	none	399.96	400.04	399.96	400.04	ns	10 Mbps	Figure 13
	Thigh1,Tlow1		140	260	140	260	ns		
	Trise1,Tfall1		—	3	—	3	ns		
MIIRXCLKP, MIITXCLKP	Tperiod1	none	39.996	40.004	39.996	40.004	ns	100 Mbps	
	Thigh1,Tlow1		14	26	14	26	ns		
	Trise1,Tfall1		—	2	—	2	ns		
MIIRXDP[3:0], MIIRXDVP, MIIRXERP	Tsu2	MIIRXCLKP rising	5	—	5	—	ns		
	Thld2		3	—	3	—	ns		
MIITXDP[3:0], MIITXENP, MIITXERP	Tdo3	MIITXCLKP rising	7	13	7	13	ns		
MIIMDCP	Tperiod4	none	30	—	30	—	ns		
	Thigh4,Tlow4		14	—	14	—	ns		
	Trise4		—	11	—	11	ns		
	Tfall4		—	8	—	8	ns		
MIIMDIOP	Tsu5	MIIMDCP rising	6	—	6	—	ns		
	Thld5		0.5	—	0.5	—	ns		
	Tdo5		3	7	3	7	ns		

[1] Ethernet clock (MIIRXCLKP and MIITXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.
[2] MIICOLP and MIICRSP are asynchronous signals.

Table 7 Ethernet AC Timing Characteristics

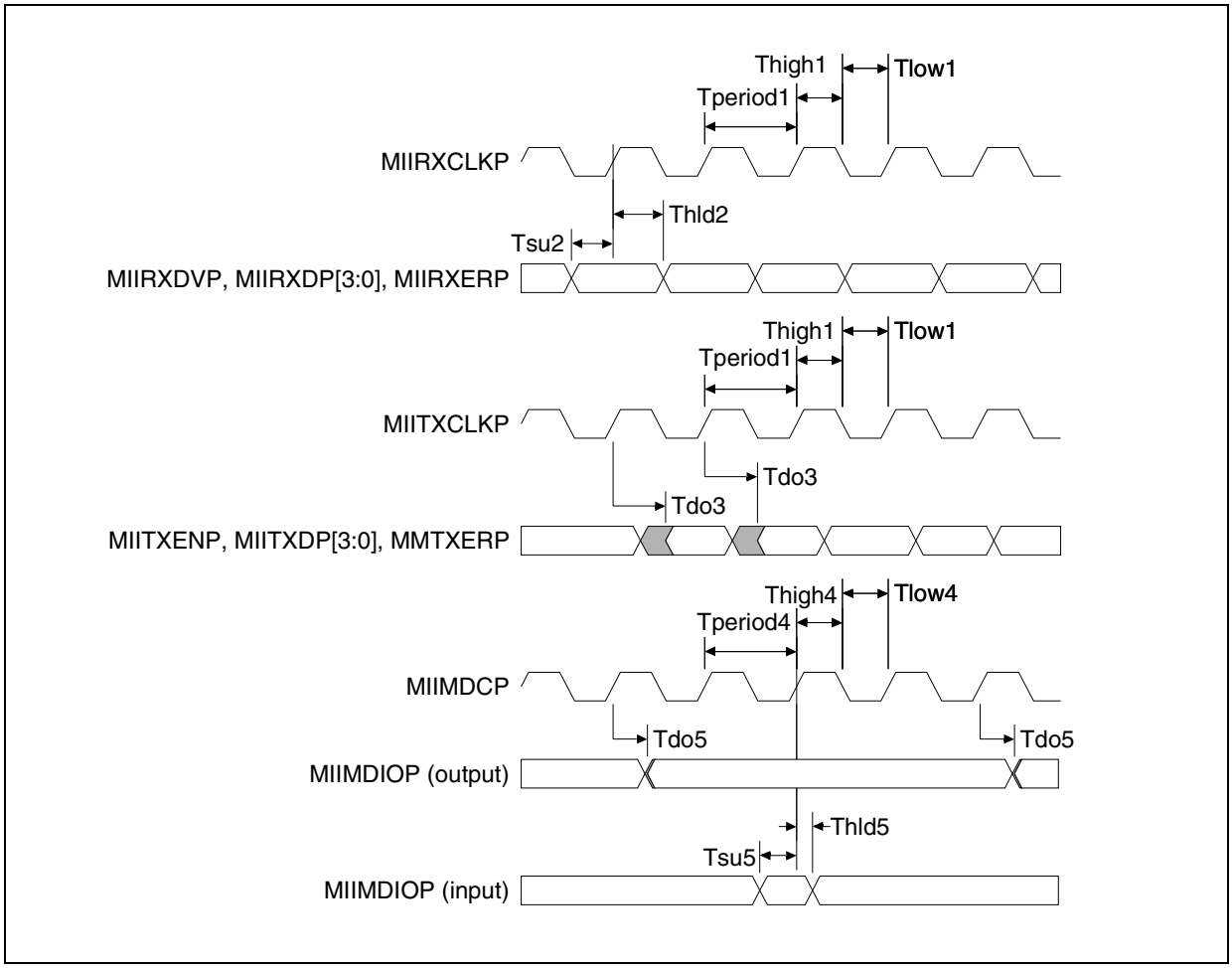


Figure 13 Ethernet AC Timing Waveform

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
ATM Interface, Utopia Mode[1,2]									
RXCLKP, TXCLKP[1]	Tperiod1	none	—	40	—	40	ns	25 MHz Utopia	Figure 14
	Thigh1,Tlow1		16	—	16	—	ns		
	Trise1,Tfall1		—	4	—	4	ns		
RXCLKP, TXCLKP[1]	Tperiod1	none	—	30	—	30	ns	33 MHz Utopia	
	Thigh1,Tlow1		12	—	12	—	ns		
	Trise1,Tfall1		—	3	—	3	ns		
RXCLKP, TXCLKP	Tperiod1	none	—	20	—	20	ns	50 MHz Utopia	
	Thigh,Tlow1		8	—	8	—	ns		
	Trise1,Tfall1		—	2	—	2	ns		
TXFULLN	Tsu2	TXCLKP rising	2	—	2	—	ns		
	Thld2		2	—	2	—	ns		
TXDATA[7:0], TXSOC, TXENBN, TXADDR[1:0]	Tdo3	TXCLKP rising	4	8	4	8	ns		
RXDATA[7:0], RXEMP-TYN, RXSOC	Tsu4	RXCLKP rising	3	—	3	—	ns		
	Thld4		2	—	2	—	ns		
RXADDR[1:0], RXENBN	Tdo5	RXCLKP rising	3	8	3	8	ns		

Table 8 ATM AC Timing Characteristics

1. ATM Utopia clock (RXCLKP and TXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.
2. All Utopia Mode pins are multiplexed on the ATM interface pins as described in Table 9.

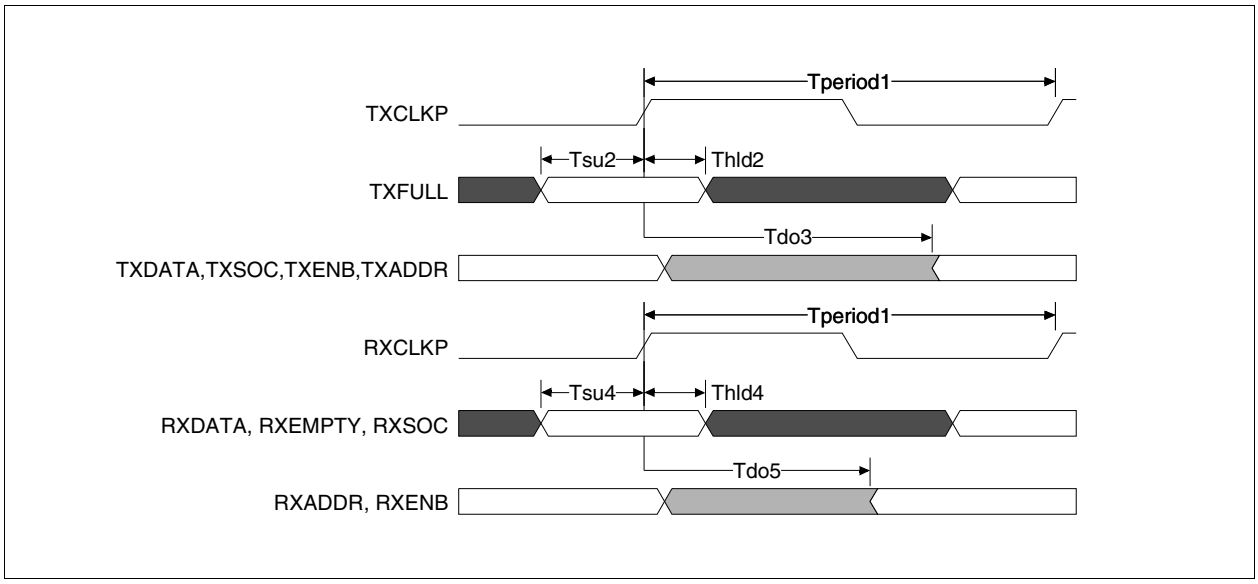


Figure 14 ATM AC Timing Waveform

ATM Pin Name	Utopia Level 1	Utopia Level 2
ATMINP[0]	RXDATA[0]	RXDATA[0]
ATMINP[1]	RXDATA[1]	RXDATA[1]
ATMINP[2]	RXDATA[2]	RXDATA[2]
ATMINP[3]	RXDATA[3]	RXDATA[3]
ATMINP[4]	RXDATA[4]	RXDATA[4]
ATMINP[5]	RXDATA[5]	RXDATA[5]
ATMINP[6]	RXDATA[6]	RXDATA[6]
ATMINP[7]	RXDATA[7]	RXDATA[7]
ATMINP[8]	RXCLKP	RXCLKP
ATMINP[9]	RXEMPTYN	RXEMPTYN
ATMINP[10]	RXSOC	RXSOC
ATMINP[11]	TXFULLN	TXFULLN
ATMIOP[0]	RXENBN	RXENBN
ATMIOP[1]	TXCLKP	TXCLKP
ATMOUTP[0]	TXDATA[0]	TXDATA[0]
ATMOUTP[1]	TXDATA[1]	TXDATA[1]
ATMOUTP[2]	TXDATA[2]	TXDATA[2]
ATMOUTP[3]	TXDATA[3]	TXDATA[3]
ATMOUTP[4]	TXDATA[4]	TXDATA[4]
ATMOUTP[5]	TXDATA[5]	TXDATA[5]
ATMOUTP[6]	TXDATA[6]	TXDATA[6]
ATMOUTP[7]	TXDATA[7]	TXDATA[7]
ATMOUTP[8]	TXSOC	TXSOC
ATMOUTP[9]	TXENBN	TXENBN
GPIOP[22]		TXADDR[0]
GPIOP[23]		TXADDR[1]
GPIOP[24]		RXADDR[0]
GPIOP[25]		RXADDR[1]

Table 9 ATM I/O Pin Description

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
USB									
USBCLKP[1]	Tperiod1	none	19.79	21.87	19.79	21.87	ns		Figure 15
	Thigh1,Tlow1		8.3	—	8.3	—	ns		
	Trise1,Tfall1		—	3	—	3	ns		
	Tjitter1		—	0.8	—	0.8	ns	1/4th of the minimum Source data jitter	
USBDN, USBDP	Trise2		4	20	4	20	ns	Universal Serial Bus Specification (USBS) Revision 1.1: Figures 7.6 and 7.7.	
	Tfall2		4	20	4	20	ns	USBS Revision 1.1: Figures 7.6 and 7.7.	
USBDN and USBDP Rise and Fall Time Matching			90	111.11	90	111.11	%	USBS Revision 1.1: Note 10, Section 7.1.2.	
Data valid period	Tstate		60	—	60	—	ns		
Skew between USBDN and USBDP			—	0.4	—	0.4	ns	USBS Revision 1.1: Section 7.1.3	
Source data jitter			—	3.5	—	3.5	ns	USBS Revision 1.1: Table 7-6	
Receive data jitter			—	12	—	12	ns		
Source EOP length	Tseop		160	175	160	175	ns		
Receive EOP length	Treop		82	—	82	—	ns		
EOP jitter			-2	5	-2	5	ns		
Full-speed Data Rate	Tfdrate		11.97	12.03	11.97	12.03	MHz	Average bit rate, USBS Section 7.1.11.	
Frame Interval			0.9995	1.0005	0.9995	1.0005	ms	USBS Section 7.1.12.	
Consecutive Frame Interval Jitter			—	42	—	42	ns	Without frame adjustment.	
			—	126	—	126	ns	With frame adjustment.	

[1] USB clock (USBCLKP) frequency must be less than CLKP frequency.

Table 10 USB AC Timing Characteristics

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
GPIOP									
GPIOP[31:0][1]	Tsu1	CLKP rising	4	—	4	—	ns		Figure 16
	Thld1		1.4	—	1.4	—	ns		
	Tdo1		2	8	2	8	ns		
GPIOP[35:32][2]	Tsu1		3	—	3	—	ns		
	Thld1		1	—	1	—	ns		
	Tdo1		3	8	3	8	ns		

[1] GPIO[31:0] can be asynchronous signals; the values are provided for ATE (test) only.
[2] GPIOP[35:32] are synchronous signals.

Table 12 GPIOP AC Timing Characteristics

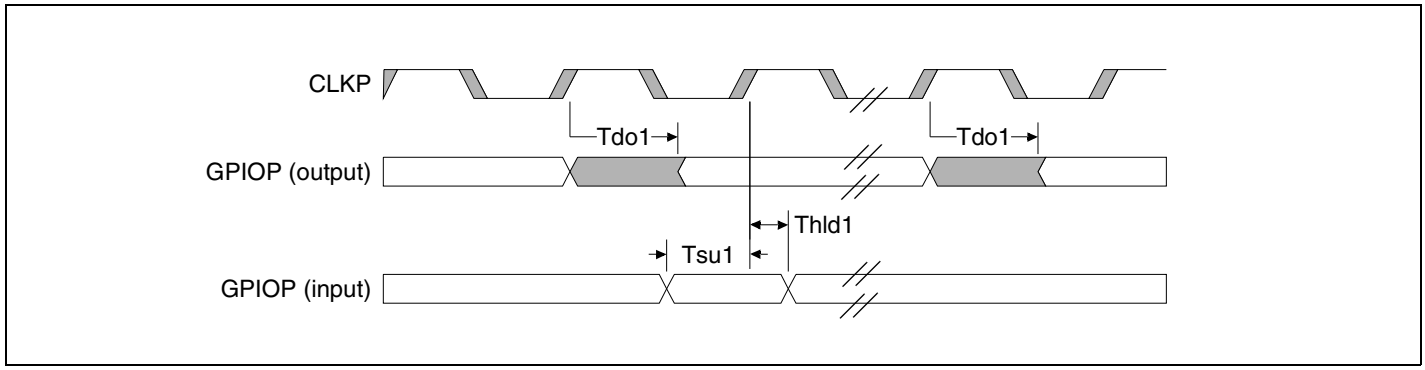


Figure 16 GPIOP AC Timing Waveform

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
EJTAG and JTAG									
JTAG_TCK	Tperiod1	none	100	—	100	—	ns		Figure 17
	Thigh1,Tlow1		40	—	40	—	ns		
	Trise1,Tfall1		—	5	—	5	ns		
EJTAG_DCLK[1]	Tperiod2	none	10.0	10.0	7.5	10.0	ns		
	Thigh2,Tlow2		2.5	—	2.5	—	ns		
	Trise2,Tfall2		—	3.5	—	3.5	ns		
JTAG_TMS, JTAG_TDI, JTAG_TRST_N	Tsu3	JTAG_TCK rising	3.0	—	3.0	—	ns		
	Thld3		1.0	—	1.0	—	ns		
JTAG_TDO	Tdo4	JTAG_TCK falling	2.0	12.0	2.0	12.0	ns		
	Tdo5	EJTAG_DCLK rising	-0.7[2]	1.0	-0.7[2]	1.0	ns		
JTAG_TRST_N	Tpw6	none	100	—	100	—	ns		
	Tsu6	JTAG_TCK rising	2	—	2	—	ns		
EJTAG_PCST[2:0]	Tdo7	EJTAG_DCLK rising	-0.3[2]	3.3	-0.3[2]	3.3	ns		

1. EJTAG_DCLK is equal to the internal CPU pipeline clock.

2. A negative delay denotes the amount of time before the reference clock edge.

Table 13 JTAG AC Timing Characteristics

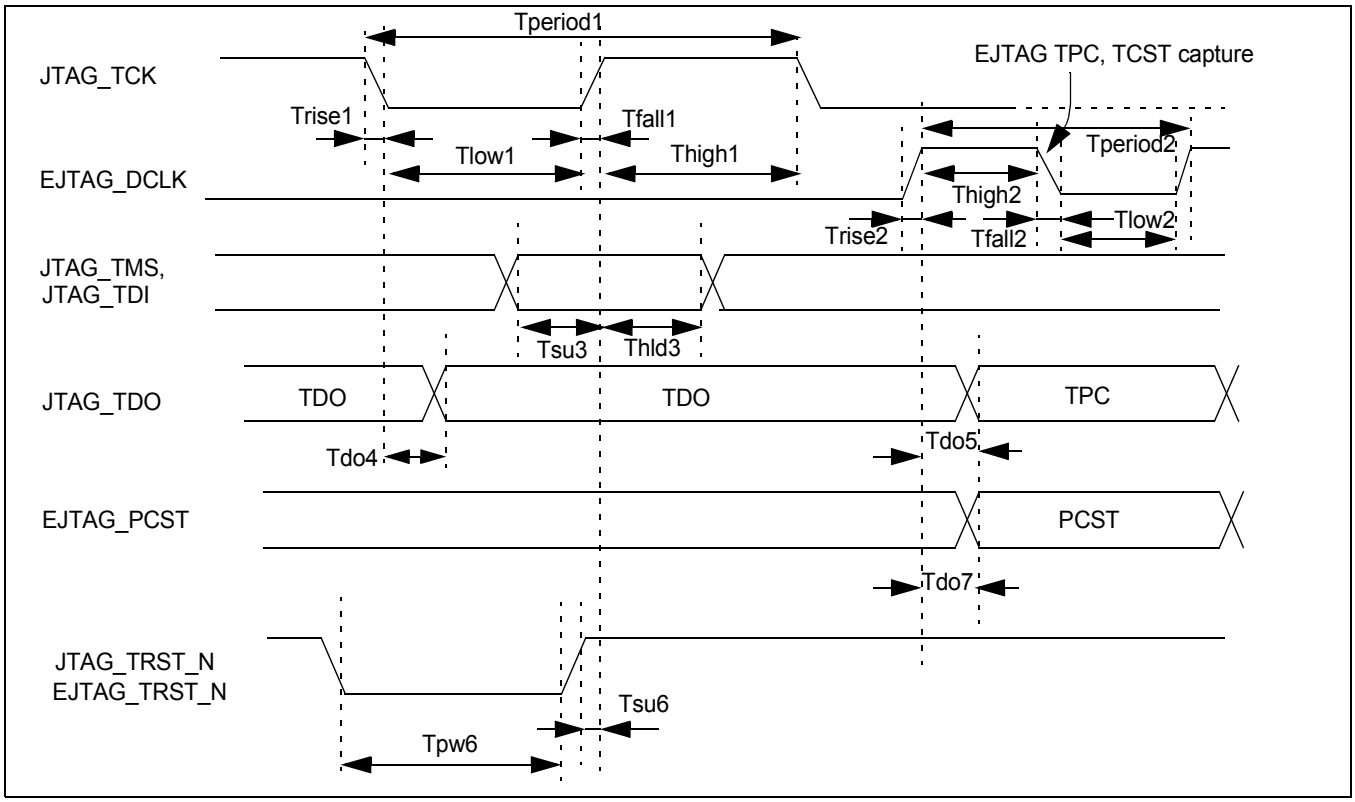


Figure 17 JTAG AC Timing Waveform

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
38	Vcc Core		90	MIITXCLKP		142	Vss		194	MADDR[09]	
39	GPIOP[09]	2	91	MIITXERP		143	MDATA[07]		195	MADDR[20]	
40	GPIOP[10]	2	92	MIIRXERP		144	MDATA[23]		196	MADDR[10]	
41	GPIOP[11]	2	93	MIIRXCLKP		145	SDCLKINP		197	MADDR[21]	
42	GPIOP[12]	2	94	MIIRXDVP		146	MDATA[08]		198	CASN	
43	Vcc I/O		95	Vcc I/O		147	MDATA[24]		199	RASN	
44	GPIOP[13]	2	96	MIIRXDP[0]		148	MDATA[09]		200	SDWEN	
45	Vss		97	MIIRXDP[1]		149	MDATA[25]		201	Vcc I/O	
46	GPIOP[14]		98	MIIRXDP[2]		150	MDATA[10]		202	SDCSN[0]	
47	GPIOP[15]		99	MIIRXDP[3]		151	Vcc I/O		203	Vss	
48	GPIOP[35]		100	Vss		152	MDATA[26]		204	SDCSN[1]	
49	GPIOP[34]		101	MIIDCP		153	Vss		205	ATMINP[00]	
50	GPIOP[33]		102	MIIDIOP		154	MDATA[11]		206	ATMIOP[0]	
51	GPIOP[32]		103	RSTN		155	MDATA[27]		207	ATMIOP[1]	
52	INSTP		104	BRN		156	MDATA[12]		208	ATMINP[01]	

[1] VccP and VssP are the Phase Lock Loop (PLL) power and ground. PLL power and ground should be supplied through a special filter circuit.

Table 20: 208-pin QFP Package Pin-Out (Part 2 of 2)

Alternate Pin Functions

Pin	Primary	Alt #1	Alt #2	Pin	Primary	Alt #1	Alt #2
20	GPIOP[00]	U0SOUTP		55	GPIOP[17]	CSN[5]	
21	GPIOP[01]	U0SINP		56	GPIOP[18]	DMAREQN	
23	GPIOP[02]	U0RIN	JTAG_TRST_N	59	GPIOP[19]	DMADONEN	
24	GPIOP[03]	U0DCRN		60	GPIOP[20]	USBSOF	
27	GPIOP[04]	U0DTRN	CPUP	62	GPIOP[21]	CKENP	
28	GPIOP[05]	U0DSRN		64	GPIOP[22]	TXADDR[0]	
33	GPIOP[06]	U0RTSN		65	GPIOP[23]	TXADDR[1]	DMAP[0]
35	GPIOP[07]	U0CTSN		66	GPIOP[24]	RXADDR[0]	
37	GPIOP[08]	U1SOUTP	DMAP[3]	68	GPIOP[25]	RXADDR[1]	DMAP[1]
39	GPIOP[09]	U1SINP	DMAP[2]	71	GPIOP[27]	MADDR[22]	
40	GPIOP[10]	U1DTRN	EJTAG_PCST[0]	73	GPIOP[28]	MADDR[23]	
41	GPIOP[11]	U1DSRN	EJTAG_PCST[1]	74	GPIOP[29]	MADDR[24]	
42	GPIOP[12]	U1RTSN	EJTAG_PCST[2]	75	GPIOP[30]	MADDR[25]	
44	GPIOP[13]	U1CTSN	EJTAG_DCLK	76	GPIOP[31]	DMAFIN	EJTAG_TRST_N
54	GPIOP[16]	CSN[4]					

Table 21 Alternate Pin Functions