Renesas Electronics America Inc - IDT79RC32T351-133DHG Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 1.1 (1)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t351-133dhg

- *Supports burst transfers*

◆ **USB**
- *Revision 1.1 compliant*
- *USB slave device controller*
- *Supports a 6th USB endpoint*
- *Full speed operation at 12 Mb/s*
- *Supports control, interrupt, bulk and isochronous endpoints*
- *Supports USB remote wakeup*
- *Integrated USB transceiver*

◆ **EJTAG**
- *Run-time Mode provides a standard JTAG interface*
- *Real-Time Mode provides additional pins for real-time trace information*

◆ **Ethernet**
- *Full duplex support for 10 and 100 Mb/s Ethernet*
- *IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface*
- *IEEE 802.3u auto-negotiation for automatic speed selection*
- *Flexible address filtering modes*
- *64-entry hash table based multicast address filtering*

◆ **ATM SAR**
- *Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)*
- *Supports 25Mb/s and faster ATM*
- *Supports UTOPIA data path interface operation at speeds up to 33 MHz*
- *Supports standard 53-byte ATM cells*
- *Performs HEC generation and checking*
- *Cell processing discards short cells and clips long cells*
- *16 cells worth of buffering*
- *UTOPIA modes: 8 cell input buffer and 8 cell output buffer*
- *Hardware support for CRC-32 generation and checking for AAL5*
- *Hardware support for CRC-10 generation and checking*
- *Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels*
- *Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention*

◆ **System Features**
- *JTAG interface (IEEE Std. 1149.1 compatible)*
- *208 pin PQFP package*
- *2.5V core supply and 3.3V I/O supply*
- *Up to 133 MHz pipeline frequency and up to 66 MHz bus frequency*

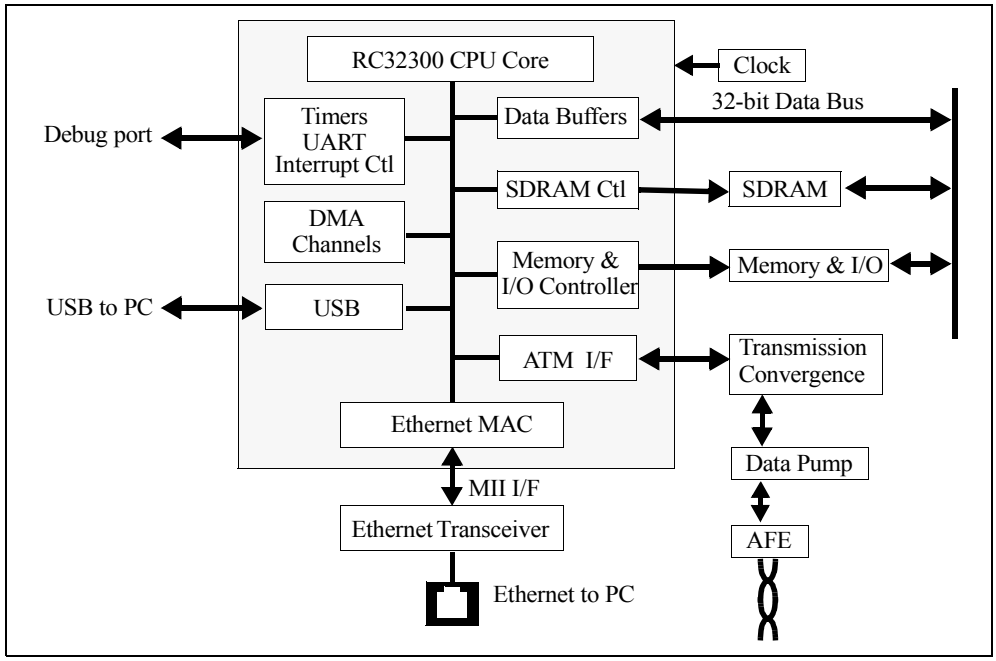


Figure 2 Example of xDSL Residential Gateway Using RC32351

Thermal Considerations

The RC32351 consumes less than 1.5 W peak power and is guaranteed in an ambient temperature range of 0° to +70° C (commercial).

Revision History

January 7, 2002: Initial publication.

May 20, 2002: Added values (in place of TBD) to Table 18, Power Consumption.

September 19, 2002: Added COLDRSTN Trise1 parameter to Table 5, Reset and System AC Timing Characteristics.

December 6, 2002: In Features section, changed UART speed from 115 Kb/s to 1.5 Mb/s.

December 17, 2002: Added V_{OH} parameter to Table 16, DC Electrical Characteristics.

May 25, 2004: In Table 7, signals MIIRXCLK and MIITXCLK, the Min and Max values for 10 Mbps Thigh1/Tlow1 were changed to 140 and 260 respectively and the Min and Max values for 100 Mbps Thigh1/Tlow1 were changed to 14.0 and 26.0 respectively.

Name	Type	I/O Type	Description
RWN	O	High Drive	**Read or Write.** This signal indicates if the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device, a low level indicates a write to an external device.
OEN	O	High Drive	**Output Enable.** This signal is asserted low when data should be driven by an external device during device read transactions on the memory and peripheral bus.
BWEN[3:0]	O	High Drive	**SDRAM Byte Enable Mask or Memory and I/O Byte Write Enables.** These signals are used as data input/output masks during SDRAM transactions and as byte write enable signals during device controller transactions on the memory and peripheral bus. They are active low. BWEN[0] corresponds to byte lane MDATA[7:0]. BWEN[1] corresponds to byte lane MDATA[15:8]. BWEN[2] corresponds to byte lane MDATA[23:16]. BWEN[3] corresponds to byte lane MDATA[31:24].
SDCSN[1:0]	O	High Drive	**SDRAM Chip Select.** These signals are used to select the SDRAM device on the memory and peripheral bus. Each bit is asserted low during an access to the selected SDRAM.
RASN	O	High Drive	**SDRAM Row Address Strobe**. The row address strobe asserted low during memory and peripheral bus SDRAM transactions.
CASN	O	High Drive	**SDRAM Column Address Strobe.** The column address strobe asserted low during memory and peripheral bus SDRAM transactions.
SDWEN	O	High Drive	**SDRAM Write Enable.** Asserted low during memory and peripheral bus SDRAM write transactions.
CKENP	O	Low Drive	**SDRAM Clock Enable.** Asserted high during active SDRAM clock cycles. Primary function: General Purpose I/O, GPIOP[21].
SDCLKINP	I	STI	**SDRAM Clock Input.** This clock input is a delayed version of SYSCLKP. SDRAM read data is sampled into the RC32351 on the rising edge of this clock.
ATM Interface			
ATMINP[11:0]	I	STI	**ATM PHY Inputs.** These pins are the inputs for the ATM interface.
ATMIOP[1:0]	I/O	Low Drive with STI	**ATM PHY Bidirectional Signals.** These pins are the bidirectional pins for the ATM interface.
ATMOUTP[9:0]	O	Low Drive	**ATM PHY Outputs.** These pins are the outputs for the ATM interface.
TXADDR[1:0]	O	Low Drive	**ATM Transmit Address [1:0]**. 2-bit address bus used for transmission in Utopia-2 mode. TXADDR[0] Primary function: General purpose I/O, GPIOP[22]. TXADDR[1] Primary function: General purpose I/O, GPIOP[23].
RXADDR[1:0]	O	Low Drive	**ATM Receive Address [1:0]**. 2-bit address bus for receiving in Utopia-2 mode. RXADDR[0] Primary function: General purpose I/O, GPIOP[24]. RXADDR[1] Primary function: General purpose I/O, GPIOP[25].
General Purpose Input/Output			
GPIOP[0]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial output, U0SOUTP.
GPIOP[1]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial input, U0SINP.
GPIOP[2]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 ring indicator, U0RIN. 2nd Alternate function: JTAG boundary scan tap controller reset, JTAG_TRST_N.
GPIOP[3]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data carrier detect, U0DCRN.
GPIOP[4]	I/O	Low Drive with STI	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 data terminal ready, U0DTRN. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.

Table 1 Pin Descriptions (Part 2 of 7)

Name	Type	I/O Type	Description
MIIMDIOP	I/O	Low Drive with STI	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
MIIRXCLKP	I	STI	**MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data.
MIIRXDP[3:0]	I	STI	**MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY.
MIIRXDVP	I	STI	**MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MIIRXERP	I	STI	**MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MIITXCLKP	I	STI	**MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MIITXDP[3:0]	O	Low Drive	**MII Transmit Data.** This nibble wide data bus contains the data to be transmitted.
MIITXENP	O	Low Drive	**MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission.
MIITXERP	O	Low Drive	**MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
EJTAG			
JTAG_TCK	I	STI	**JTAG Clock.** This is an input test clock, used to shift data into or out of the boundary scan logic. This signal requires an external resistor, listed in Table 14.
JTAG_TDI	I	STI	**JTAG Data Input.** This is the serial data shifted into the boundary scan logic. This signal requires an external resistor, listed in Table 14. This is also used to input EJTAG_DINTN during EJTAG/ICE mode. EJTAG_DINTN is an interrupt to switch the PC trace mode off.
JTAG_TDO	O	Low Drive	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic. When no data is being shifted out, this signal is tri-stated. This signal requires an external resistor, listed in Table 14. This is also used to output the EJTAG_TPC during EJTAG/ICE mode. EJTAG_TPC is the non-sequential program counter output.
JTAG_TMS	I	STI	**JTAG Mode Select**. This input signal is decoded by the tap controller to control test operation. This signal requires an external resistor, listed in Table 14.
EJTAG_PCST[0]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[10]. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN.
EJTAG_PCST[1]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11]. 1st Alternate function: UART channel 1 data set ready, U1DSRN.
EJTAG_PCST[2]	O	Low Drive	**PC trace status.** This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[12]. 1st Alternate function: UART channel 1 request to send, U1RTSN.
EJTAG_DCLK	O	Low Drive	**PC trace clock.** This is used to capture address and data during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[13]. 1st Alternate function: UART channel 1 clear to send, U1CTSN.

Table 1 Pin Descriptions (Part 5 of 7)

Signal	Name/Description
MDATA[2:0]	**Clock Multiplier**. This field specifies the value by which the system clock (CLKP) is multiplied internally to generate the CPU pipeline clock. 0x0 - multiply by 2 0x1 - multiply by 3 0x2 - multiply by 4 0x3 - reserved 0x4 - reserved 0x5 - reserved 0x6 - reserved 0x7 - reserved
MDATA[3]	**Endian.** This bit specifies the endianness of RC32351. 0x0 - little endian 0x1 - big endian
MDATA[4]	**Reserved.** Must be set to 0.
MDATA[5]	**Debug Boot Mode**. When this bit is set, the RC32351 begins executing from address 0xFF20_0200 rather than 0xBFC0_0000 following a reset. 0x0 - regular mode (processor begins executing at 0xBFC0_0000) 0x1 - debug boot mode (processor begins executing at 0xFF20_0200)
MDATA[7:6]	**Boot Device Width**. This field specifies the width of the boot device. 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width 0x2 - 32-bit boot device width 0x3 - reserved
MDATA[8]	**EJTAG/ICE Interface Enable**. When this bit is set, Alternate 2 pin functions EJTAG_PCST[2:0], EJTAG_DCLK, and EJTAG_TRST_N are selected. 0x0 - GPIOP[31, 13:10] pins behaves as GPIOP 0x1 - GPIOP[31] pin behaves as EJTAG_TRST_N, GPIOP[12:10] pins behave as EJTAG_PCST[2:0], and GPIOP[13] pin behaves as EJTAG_DCLK
MDATA[9]	**Fast Reset**. When this bit is set, RC32351 drives RSTN for 64 clock cycles, used during test only. Clear this bit for normal operation. 0x0 - Normal reset: RC32351 drives RSTN for minimum of 4096 clock cycles 0x1 - Fast Reset: RC32351 drives RSTN for 64 clock cycles (test only)
MDATA[10]	**DMA Debug Enable**. When this bit is set, Alternate 2 pin function, DMAP is selected. DMAP provides the DMA channel number during memory and peripheral bus DMA transactions. 0x0 - GPIOP[8, 9, 25, 23] pins behave as GPIOP 0x1 - GPIOP[8, 9, 25, 23] pins behave as DMAP[3:0]
MDATA[11]	**Hold SYSCLKP Constant**. For systems that do not require a SYSCLKP output and can instead use CLKP, setting this bit to a one causes the SYSCLKP output to be held at a constant level. This may be used to reduce EMI. 0x0 - Allow SYSCLKP to toggle 0x1 - Hold SYSCLKP constant
MDATA[12]	**JTAG Boundary Scan Reset Enable**. When this bit is set, Alternate 2 pin function, JTAG_TRST_N is selected. 0x0 - GPIOP[2] pin behaves as GPIOP 0x1 - GPIOP[2] pin behaves as JTAG_TRST_N
MDATA[13]	**CPU / DMA Transaction Indicator Enable**. When this bit is set, Alternate 2 pin function, CPUP is selected. 0x0 - GPIOP[4] pin behaves as GPIOP 0x1 - GPIOP[4] pin behaves as CPUP
MDATA[15:14]	**Reserved**. These pins must be driven low during boot configuration.

Table 2 Boot Configuration Vector Encoding

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

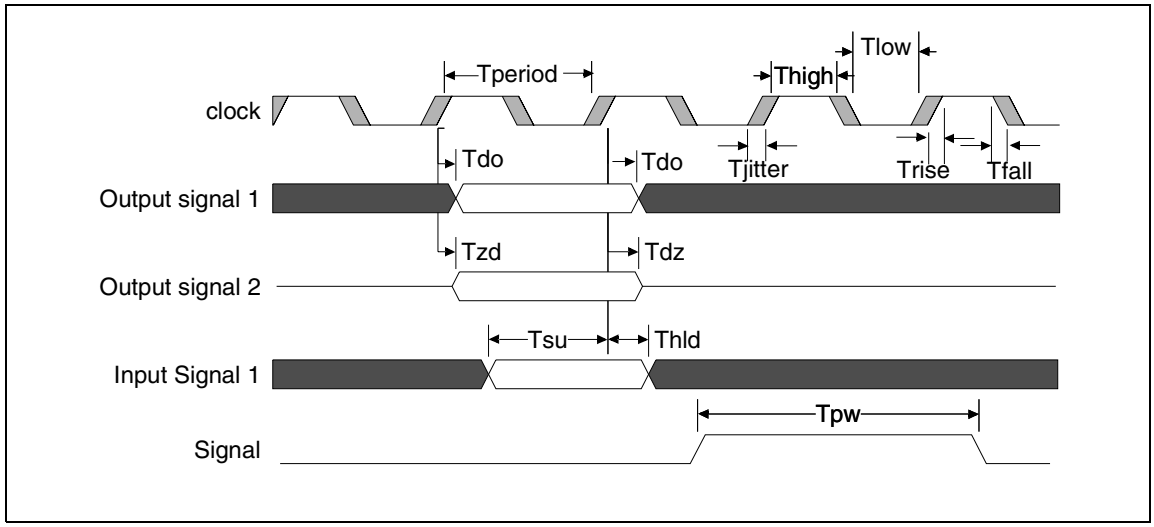


Figure 5 AC Timing Definitions Waveform

Symbol	Definition
Tperiod	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active.

Table 4 AC Timing Definitions

AC Timing Characteristics

(Ta = 0°C to +70°C Commercial, Vcc I/O = +3.3V±5%,V_{cc} Core = +2.5V±5%, V_{cc}P = +2.5V±5%)

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
Reset and System									
COLDRSTN	Tpw1	none	110	—	110	—	ms		Figure 6 Figure 7
	Trise1	none	—	5.0	—	5.0	ns		
RSTN[1]	Tdo2	CLKP rising	4.0	10.7	4.0	10.7	ns		
MDATA[15:0] Boot Configuration Vector	Thld3	COLDRSTN rising	3	—	3	—	ns		
INSTP	Tdo	CLKP rising	5	8	5.0	8.0	ns		
CPUP	Tdo	CLKP rising	3.5	7	3.5	7.0	ns		
DMAP	Tdo	CLKP rising	3.5	6.6	3.5	6.6	ns		
DMAREQN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	ns		
DMADONEN[2]	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	ns		
DMAFIN	Tdo	CLKP rising	3.5	5.9	3.5	5.9	ns		
BRN	Tsu	CLKP rising	1.6	—	1.6	—	ns		
	Thld		0	—	0	—	ns		
BGN	Tdo	CLKP rising	3.3	5.8	3.3	5.8	ns		

[1] RSTN is a bidirectional signal. It is treated as an asynchronous input.
[2] DMAREQN and DMADONEN minimum pulse width equals the CLKP period plus 7ns.

Table 5 Reset and System AC Timing Characteristics

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
Memory and Peripheral Bus - SDRAM Access									
MDATA[31:0]	Tsu1	SDCLKINP rising	2.5	—	2.5	—	ns		Figure 8 Figure 9 Figure 10
	Thld1		1.2	—	1.2	—	ns		
	Tdo1	SYSCLKP rising	1.2	5.8	1.2	5.8	ns		
	Tdz1		—	5.0	—	5.0	ns		
	Tzd1		1.0	—	1.0	—	ns		
MADDR[20:2], BWEN[3:0]	Tdo2	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
CASN, RASN, SDCSN[1:0], SDWEN	Tdo3	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
CKENP	Tdo4	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
BDIRN	Tdo5	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
BOEN[1:0]	Tdo6	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
SYSCLKP rising	Tdo7	CLKP rising	0.5	5.0	0.5	5.0	ns		
SDCLKINP	Tperiod8	none	20	50	15	50	ns		
	Thigh8,Tlow8		10	—	6.0	—	ns		
	Trise8,Tfall8		—	3.0	—	3.0	ns		
	Tdelay8	SYSCLKP rising	0	4.8	0	4.8	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

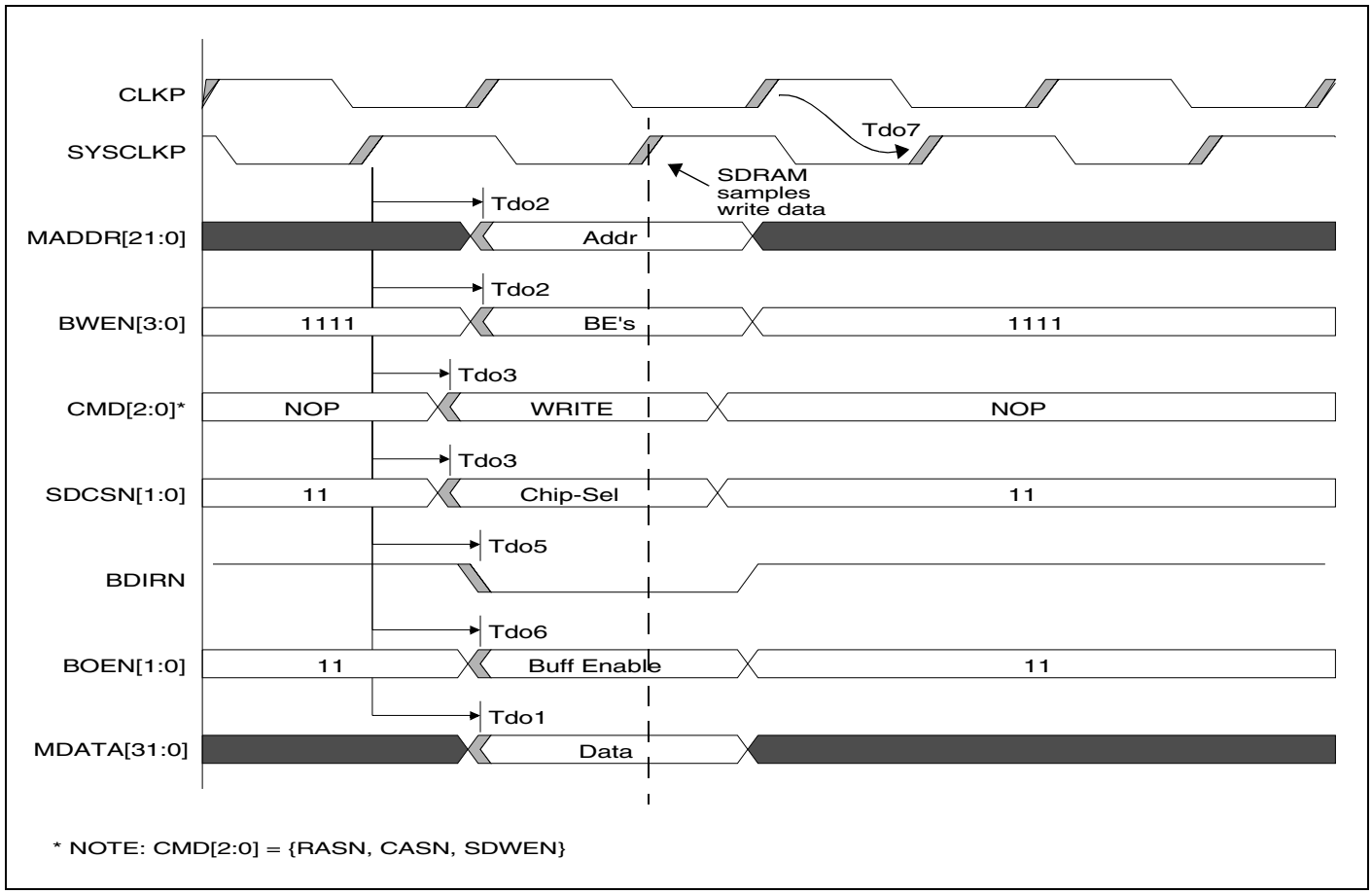


Figure 10 Memory and Peripheral Bus AC Timing Waveform - SDRAM Write Access

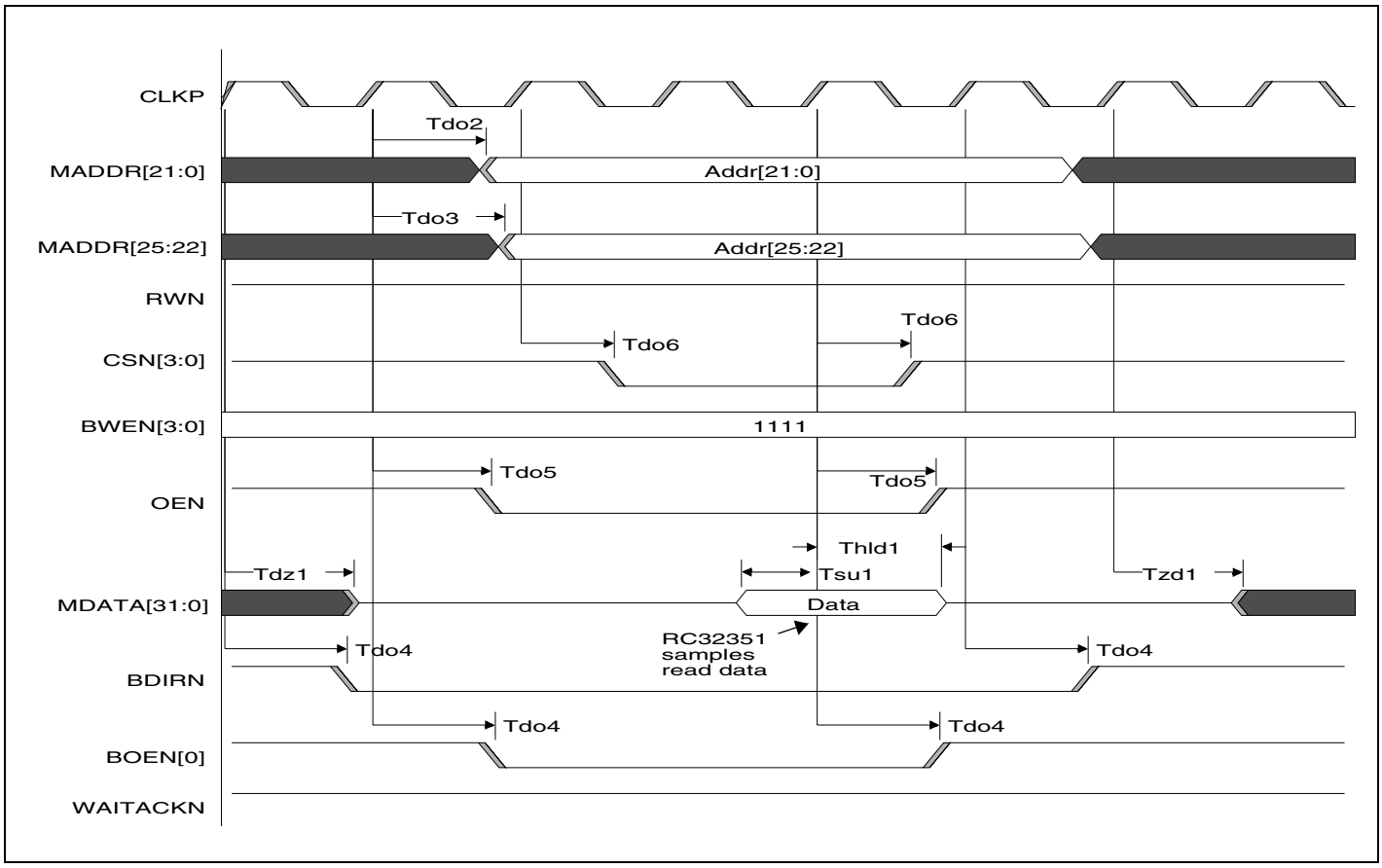


Figure 11 Memory and Peripheral Bus AC Timing Waveform - Device Read Access

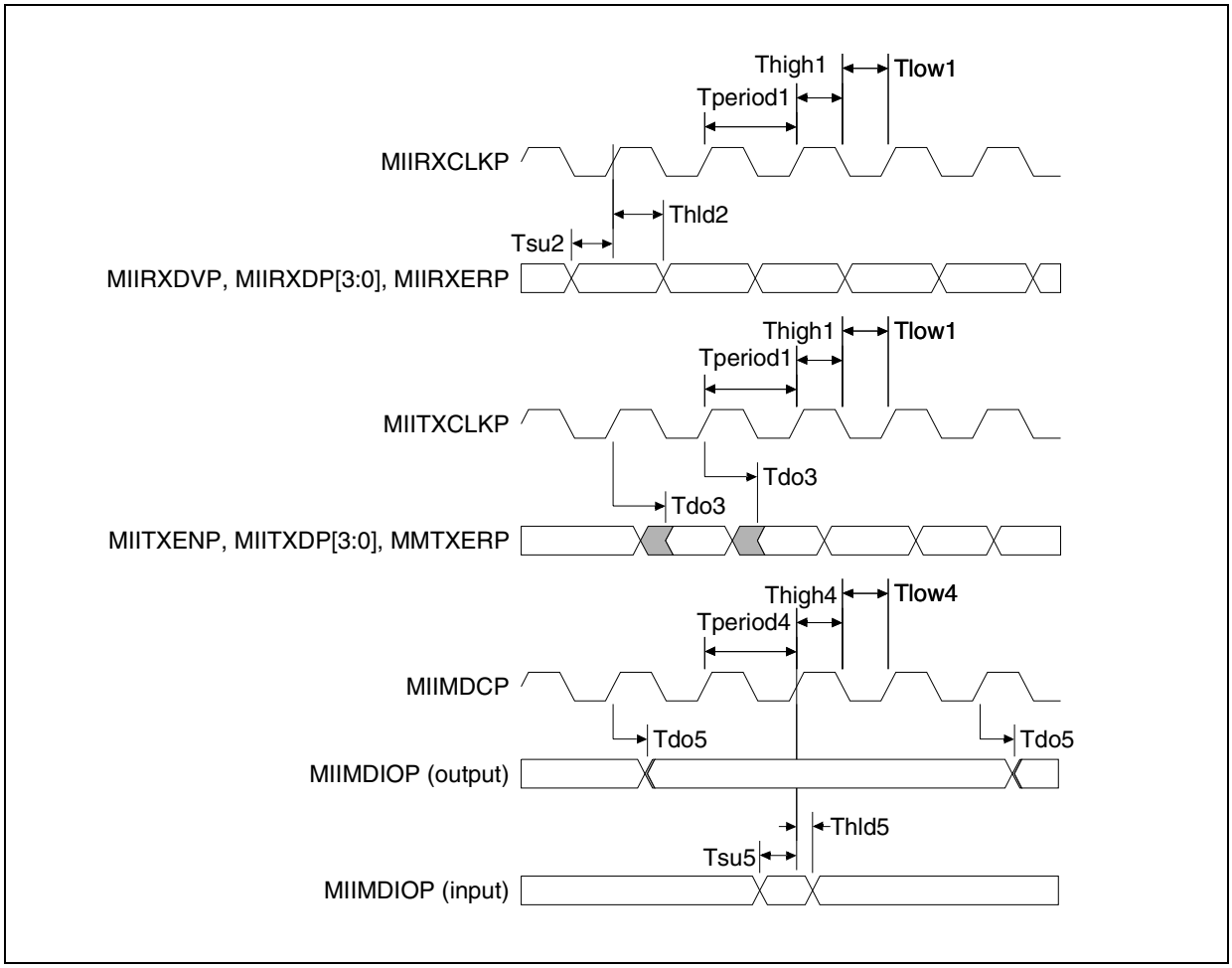


Figure 13 Ethernet AC Timing Waveform

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
GPIOP									
GPIOP[31:0][1]	Tsu1	CLKP rising	4	—	4	—	ns		Figure 16
	Thld1		1.4	—	1.4	—	ns		
	Tdo1		2	8	2	8	ns		
GPIOP[35:32][2]	Tsu1		3	—	3	—	ns		
	Thld1		1	—	1	—	ns		
	Tdo1		3	8	3	8	ns		

[1] GPIO[31:0] can be asynchronous signals; the values are provided for ATE (test) only.
[2] GPIOP[35:32] are synchronous signals.

Table 12 GPIOP AC Timing Characteristics

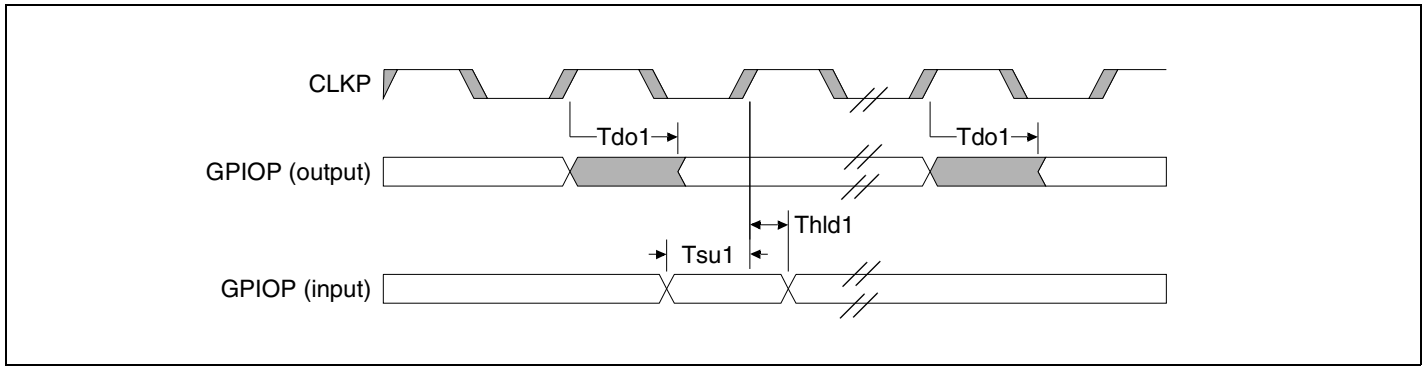


Figure 16 GPIOP AC Timing Waveform

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
EJTAG and JTAG									
JTAG_TCK	Tperiod1	none	100	—	100	—	ns		Figure 17
	Thigh1,Tlow1		40	—	40	—	ns		
	Trise1,Tfall1		—	5	—	5	ns		
EJTAG_DCLK[1]	Tperiod2	none	10.0	10.0	7.5	10.0	ns		
	Thigh2,Tlow2		2.5	—	2.5	—	ns		
	Trise2,Tfall2		—	3.5	—	3.5	ns		
JTAG_TMS, JTAG_TDI, JTAG_TRST_N	Tsu3	JTAG_TCK rising	3.0	—	3.0	—	ns		
	Thld3		1.0	—	1.0	—	ns		
JTAG_TDO	Tdo4	JTAG_TCK falling	2.0	12.0	2.0	12.0	ns		
	Tdo5	EJTAG_DCLK rising	-0.7[2]	1.0	-0.7[2]	1.0	ns		
JTAG_TRST_N	Tpw6	none	100	—	100	—	ns		
	Tsu6	JTAG_TCK rising	2	—	2	—	ns		
EJTAG_PCST[2:0]	Tdo7	EJTAG_DCLK rising	-0.3[2]	3.3	-0.3[2]	3.3	ns		

1. EJTAG_DCLK is equal to the internal CPU pipeline clock.

2. A negative delay denotes the amount of time before the reference clock edge.

Table 13 JTAG AC Timing Characteristics

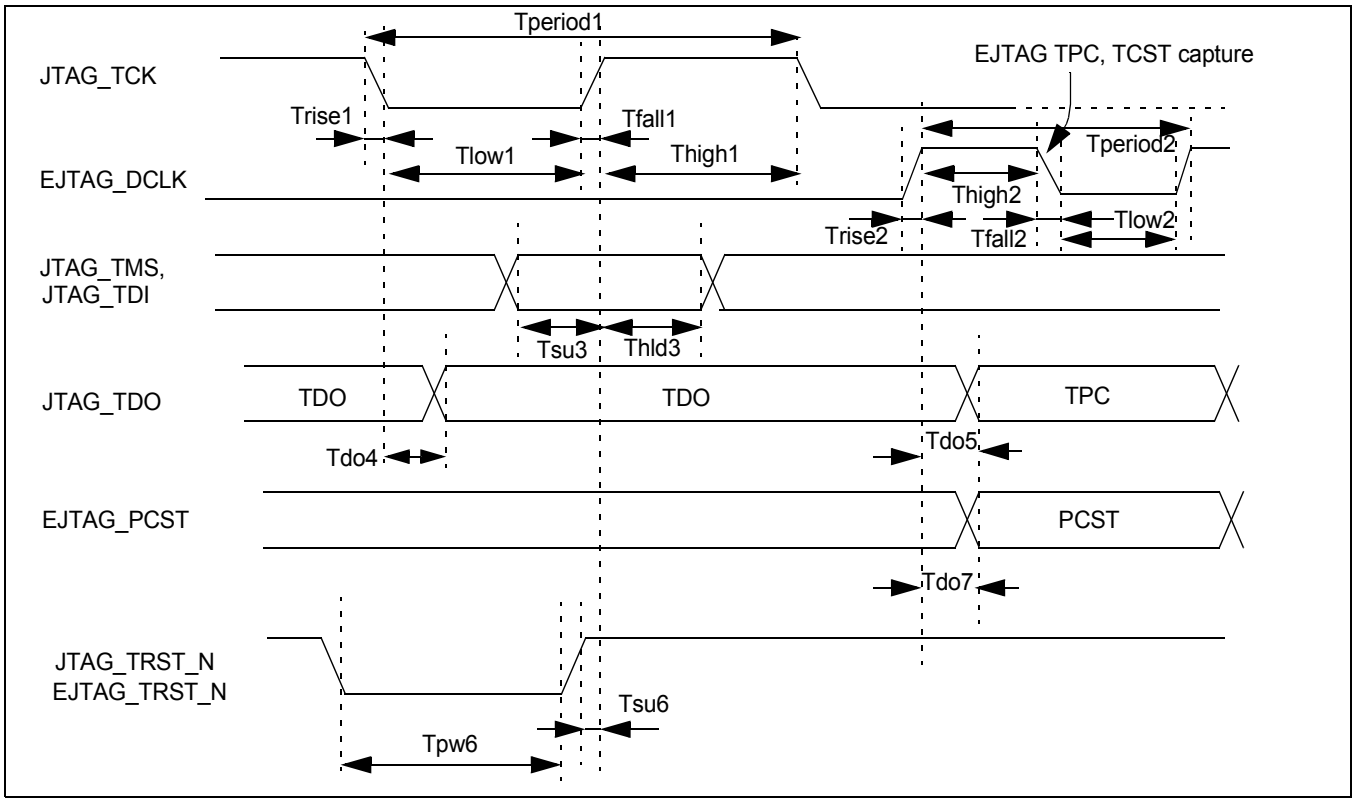


Figure 17 JTAG AC Timing Waveform

Table 14 shows the pin numbering for the Standard EJTAG connector. All the even numbered pins are connected to ground. Multiplexing of pin functions should be considered when connecting EJTAG_TRST_N and EJTAG_PCST.

For details on using the JTAG connector, see the JTAG chapters in the RC32351 user reference manual.

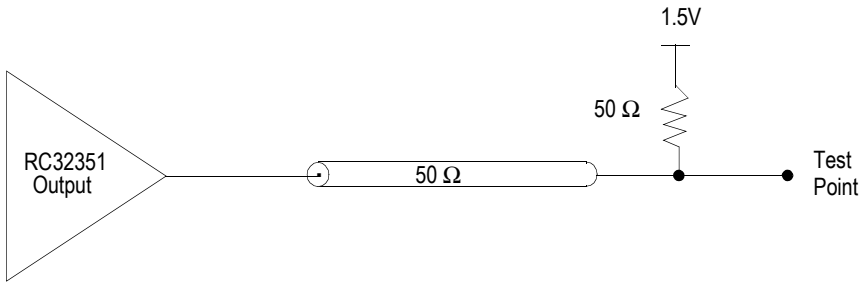
PIN	SIGNAL	RC32351 I/O	TERMINATION[1]
1	EJTAG_TRST_N	Input	10 kΩ pull-down resistor. A pull-down resistor will hold the EJTAG controller in reset when not in use if the EJTAG_TRST_N function is selected with the boot configuration vector. Refer to the User Manual.
3	JTAG_TDI	Input	10 kΩ pull-up resistor
5	JTAG_TDO	Output	33 Ω series resistor
7	JTAG_TMS	Input	10 kΩ pull-up resistor
9	JTAG_TCK	Input	10 kΩ pull-up resistor[2]
11	System Reset	Input	10 kΩ pull-up resistor is used if it is combined with the system cold reset control, COLDRSTN.
13	EJTAG_PCST[0]	Output	33 Ω series resistor
15	EJTAG_PCST[1]	Output	33 Ω series resistor
17	EJTAG_PCST[2]	Output	33 Ω series resistor
19	EJTAG_DCLK	Output	33 Ω series resistor
21	Debug Boot	Input	This can be connected to the boot configuration vector to control debug boot mode if desired. Refer to Table 2 on page 12 and the RC32351 user reference manual.
23	VccI/O	Output	Used to sense the circuit board power. Must be connected to the VCC I/O supply of the circuit board.

Table 14 Pin Numbering of the JTAG and EJTAG Target Connector

1. The value of the series resistor may depend on the actual printed circuit board layout situation.

2. JTAG_TCK pull-up resistor is not required according to the JTAG (IEEE1149) standard. It is indicated here to prevent a floating CMOS input when the EJTAG connector is unconnected.

Output Loading for AC Timing



Signal	Equivalent Lump Capacitance
All High Drive Signals	50 pF[1]
All Low Drive Signals	25 pF

1. An equivalent load of 50 pF is derived from the tester load plus an external load.

Figure 18 Output Loading for AC Timing

USB Electrical Characteristics

	Parameter	Min	Max	Unit	Conditions
USB Interface					
V_{di}	Differential Input Sensitivity	-0.2		V	I(D+)-(D-)I
V_{cm}	Differential Input Common Mode Range	0.8	2.5	V	
V_{se}	Single ended Receiver Threshold	0.8	2.0	V	
C_{in}	Transceiver Capacitance		20	pF	
I_{li}	Hi-Z State Data Line Leakage	-10	10	µs	$0V < V_{in} < 3.3V$
USB Upstream/Downstream Port					
V_{oh}	Static Output High	2.8	3.6	V	15km ± 5% to Gnd[7]
V_{ol}	Static Output Low		0.3	V	
Z_o	USB Driver Output Impedance	28	44	Ω	Including $R_{ext} = 20\ \Omega$

Table 17 USB Interface Characteristics

Power Consumption

Note: This table is based on a 2:1 CPU bus (PClock to CLKP) clock ratio.

Parameter		100MHz		133MHz		Unit	Conditions
		Typical	Max.	Typical	Max.		
I_{CC} I/O		60	110	80	130	mA	
$I_{CC\ core}$	Normal mode	300	350	400	450	mA	$C_L = 0$ $T_a = 25^oC$ VccP = 2.625V (for max. values) V_{cc} core = 2.625V (for max. values) V_{cc} I/O = 3.46V (for max. values) VccP = 2.5V (for typical values) V_{cc} core = 2.5V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	240	290	320	370	mA	
Power Dissipation	Normal mode	0.95	1.30	1.26	1.63	W	
	Standby mode[1]	0.80	1.09	1.06	1.42	W	

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions; however, other logic continues to function. Standby mode reduces power consumption by 0.6 mA per MHz of the CPU pipeline clock, PClock.

Table 18 RC32351 Power Consumption

Power Curve

The following graph contains a power curve that shows power consumption at various bus frequencies.

Note: The system clock (CLKP) can be multiplied by 2, 3, or 4 to obtain the CPU pipeline clock (PClock) speed.

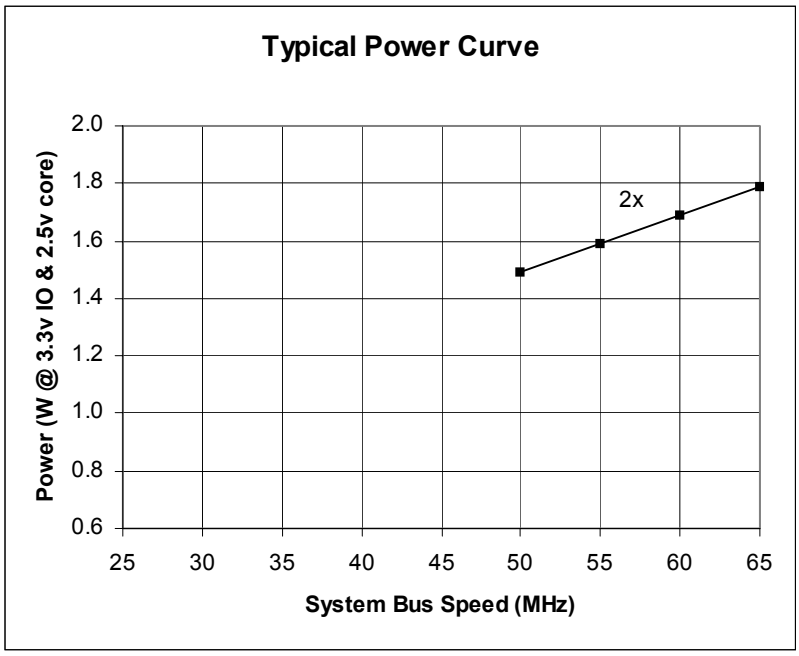


Figure 20 Typical Power Usage

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O Supply Voltage	-0.3	4.0	V
V_{CC}Core	Core Supply Voltage	-0.3	3.0	V
V_{CC}P	PLL Supply Voltage	-0.3	3.0	V
Vimin	Input Voltage - undershoot	-0.6	—	V
Vi	I/O Input Voltage	Gnd	V_{CC}I/O+0.5	V
Ta, Commercial	Ambient Operating Temperature	0	70	degrees C
Tstg	Storage Temperature	-40	125	degrees C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
38	Vcc Core		90	MIITXCLKP		142	Vss		194	MADDR[09]	
39	GPIOP[09]	2	91	MIITXERP		143	MDATA[07]		195	MADDR[20]	
40	GPIOP[10]	2	92	MIIRXERP		144	MDATA[23]		196	MADDR[10]	
41	GPIOP[11]	2	93	MIIRXCLKP		145	SDCLKINP		197	MADDR[21]	
42	GPIOP[12]	2	94	MIIRXDVP		146	MDATA[08]		198	CASN	
43	Vcc I/O		95	Vcc I/O		147	MDATA[24]		199	RASN	
44	GPIOP[13]	2	96	MIIRXDP[0]		148	MDATA[09]		200	SDWEN	
45	Vss		97	MIIRXDP[1]		149	MDATA[25]		201	Vcc I/O	
46	GPIOP[14]		98	MIIRXDP[2]		150	MDATA[10]		202	SDCSN[0]	
47	GPIOP[15]		99	MIIRXDP[3]		151	Vcc I/O		203	Vss	
48	GPIOP[35]		100	Vss		152	MDATA[26]		204	SDCSN[1]	
49	GPIOP[34]		101	MIIDCP		153	Vss		205	ATMINP[00]	
50	GPIOP[33]		102	MIIDIOP		154	MDATA[11]		206	ATMIOP[0]	
51	GPIOP[32]		103	RSTN		155	MDATA[27]		207	ATMIOP[1]	
52	INSTP		104	BRN		156	MDATA[12]		208	ATMINP[01]	

[1] VccP and VssP are the Phase Lock Loop (PLL) power and ground. PLL power and ground should be supplied through a special filter circuit.

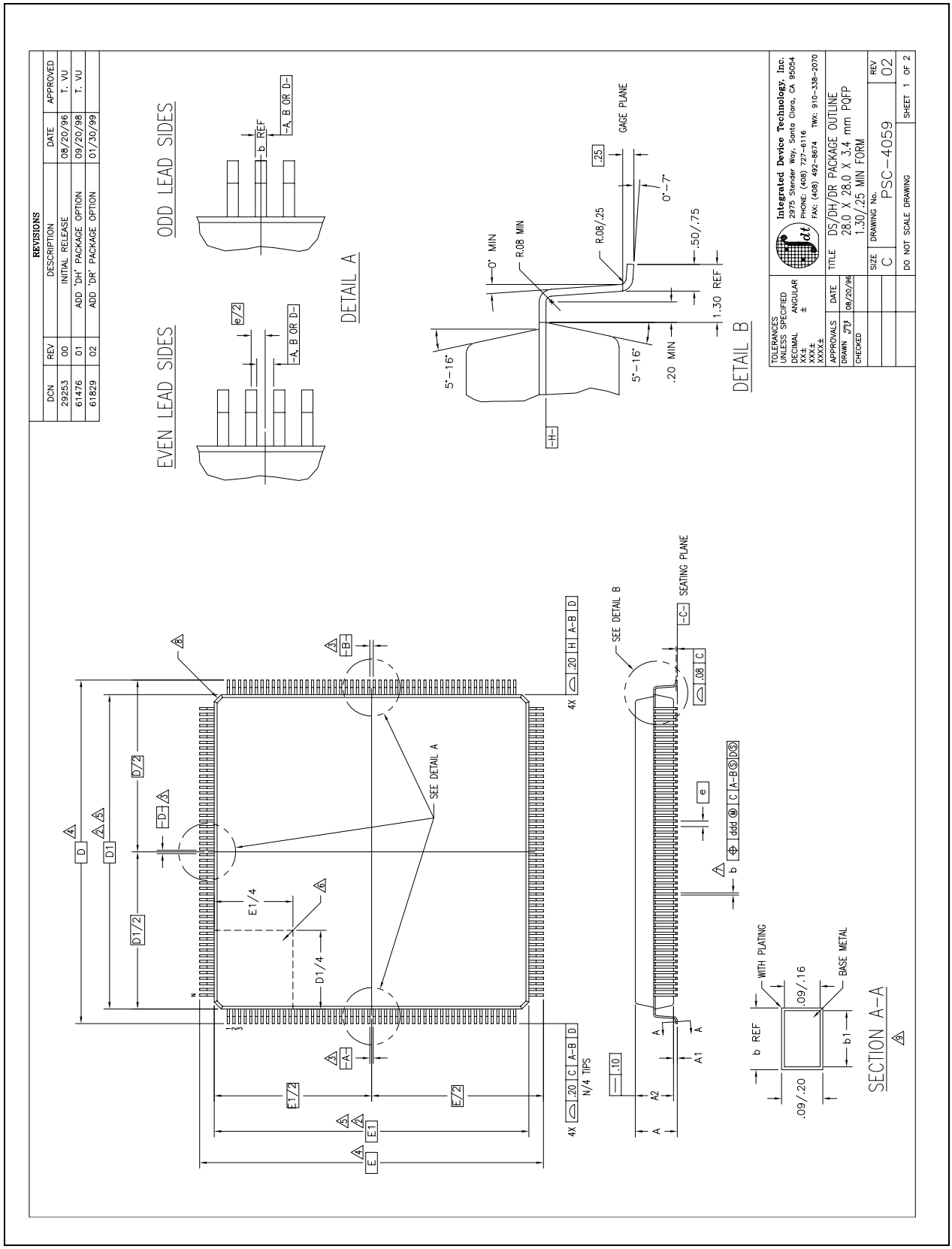
Table 20: 208-pin QFP Package Pin-Out (Part 2 of 2)

Alternate Pin Functions

Pin	Primary	Alt #1	Alt #2	Pin	Primary	Alt #1	Alt #2
20	GPIOP[00]	U0SOUTP		55	GPIOP[17]	CSN[5]	
21	GPIOP[01]	U0SINP		56	GPIOP[18]	DMAREQN	
23	GPIOP[02]	U0RIN	JTAG_TRST_N	59	GPIOP[19]	DMADONEN	
24	GPIOP[03]	U0DCRN		60	GPIOP[20]	USBSOF	
27	GPIOP[04]	U0DTRN	CPUP	62	GPIOP[21]	CKENP	
28	GPIOP[05]	U0DSRN		64	GPIOP[22]	TXADDR[0]	
33	GPIOP[06]	U0RTSN		65	GPIOP[23]	TXADDR[1]	DMAP[0]
35	GPIOP[07]	U0CTSN		66	GPIOP[24]	RXADDR[0]	
37	GPIOP[08]	U1SOUTP	DMAP[3]	68	GPIOP[25]	RXADDR[1]	DMAP[1]
39	GPIOP[09]	U1SINP	DMAP[2]	71	GPIOP[27]	MADDR[22]	
40	GPIOP[10]	U1DTRN	EJTAG_PCST[0]	73	GPIOP[28]	MADDR[23]	
41	GPIOP[11]	U1DSRN	EJTAG_PCST[1]	74	GPIOP[29]	MADDR[24]	
42	GPIOP[12]	U1RTSN	EJTAG_PCST[2]	75	GPIOP[30]	MADDR[25]	
44	GPIOP[13]	U1CTSN	EJTAG_DCLK	76	GPIOP[31]	DMAFIN	EJTAG_TRST_N
54	GPIOP[16]	CSN[4]					

Table 21 Alternate Pin Functions

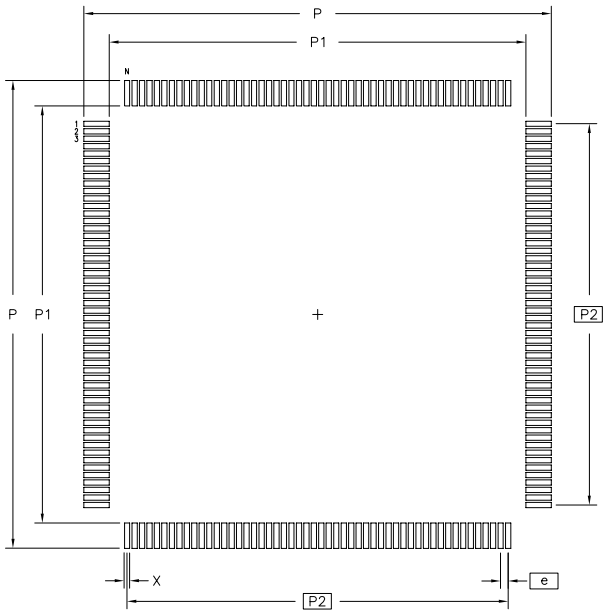
Package Drawing - 208-pin QFP



REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
29253	00	INITIAL RELEASE	08/20/96	T. VU
61476	01	ADD "DH" PACKAGE OPTION	09/20/98	T. VU
61829	02	ADD "DR" PACKAGE OPTION	01/30/99	

SYMBOL	JEDEC VARIATION FA-1			NOTE
	MIN	NOM	MAX	
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.60	
D	30.60 BSC			4
D1	28.00 BSC			5,2
E	30.60 BSC			4
E1	28.00 BSC			5,2
N	208			
e	.50 BSC			
b	.17	–	.27	7
b1	.17	.20	.23	
ddd	–	–	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.20	31.40
P1	27.80	28.00
P2	25.50 BSC	
X	.30	.40
e	.50 BSC	
N	208	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE –C–
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–143, VARIATION FA–1

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727–6116
FAX: (408) 492–8674 TWX: 910–338–2070

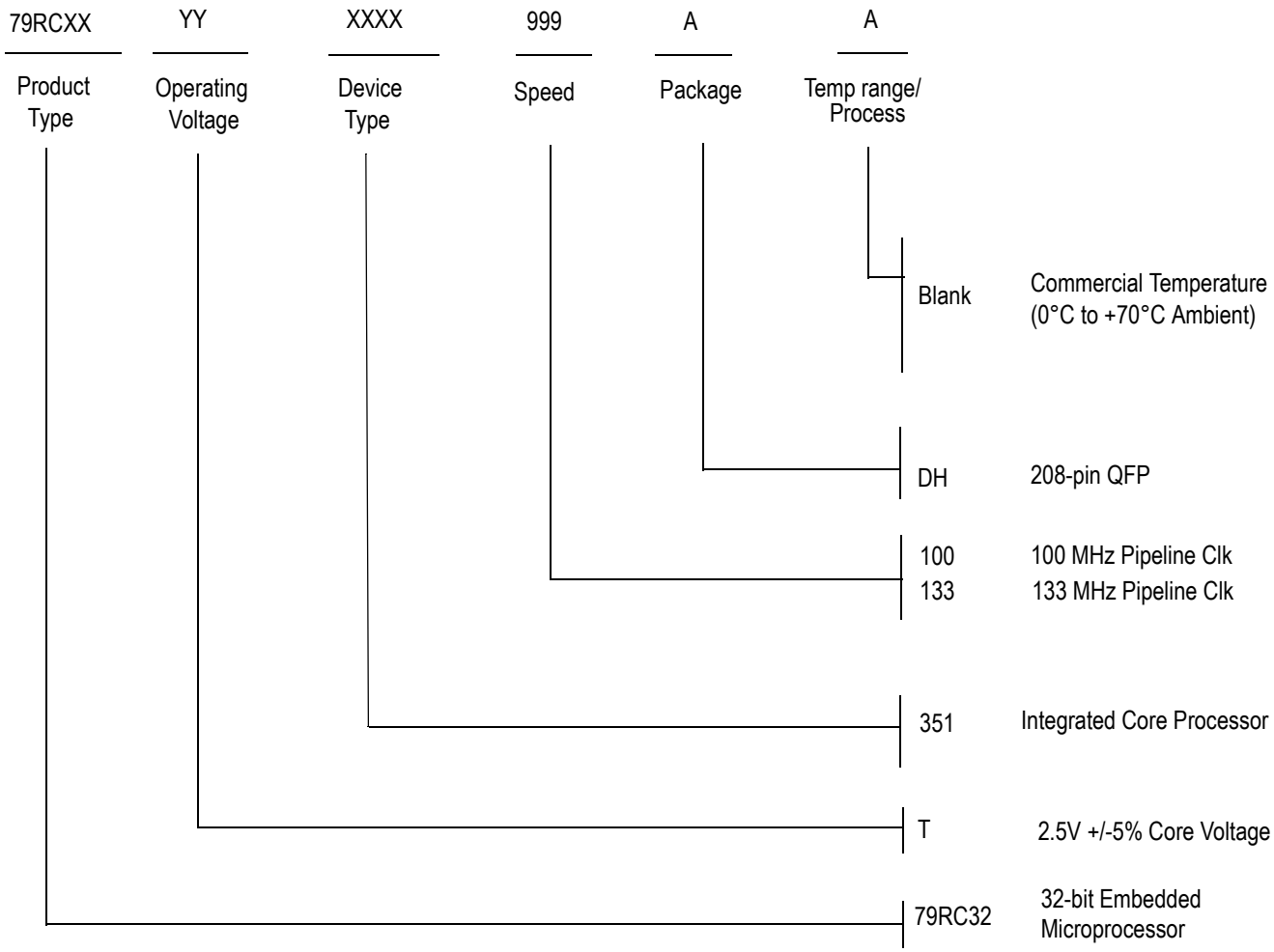
APPROVALS	DATE
DRAWN TV	08/20/96
CHECKED	

TITLE: DS/DH/DR PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.30/.25 MIN FORM

SIZE	DRAWING No.	REV
C	PSC–4059	02

DO NOT SCALE DRAWING — SHEET 2 OF 2

Ordering Information



Valid Combinations

79RC32T351 -100DH	208-pin QFP package, Commercial Temperature
79RC32T351 -133DH	208-pin QFP package, Commercial Temperature

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