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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART, USB, USB OTG |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 31 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 18x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mk51dx128clh7 |

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PK51 and MK51.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| K## | Kinetis family | • K51 |
| A | Key attribute | • D = Cortex-M4 w/ DSP<br>• F = Cortex-M4 w/ DSP and FPU |
| M | Flash memory type | • N = Program flash only<br>• X = Program flash and FlexMemory |

*Table continues on the next page...*

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

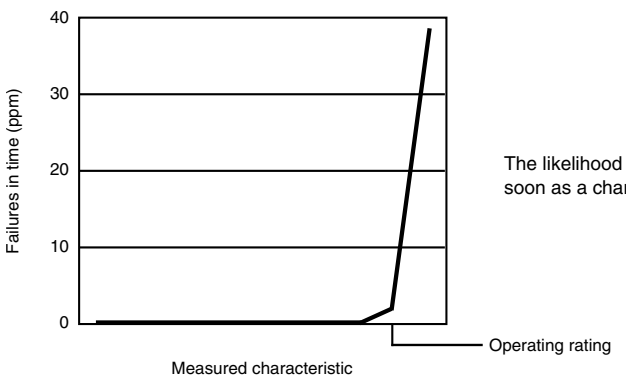
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 3.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

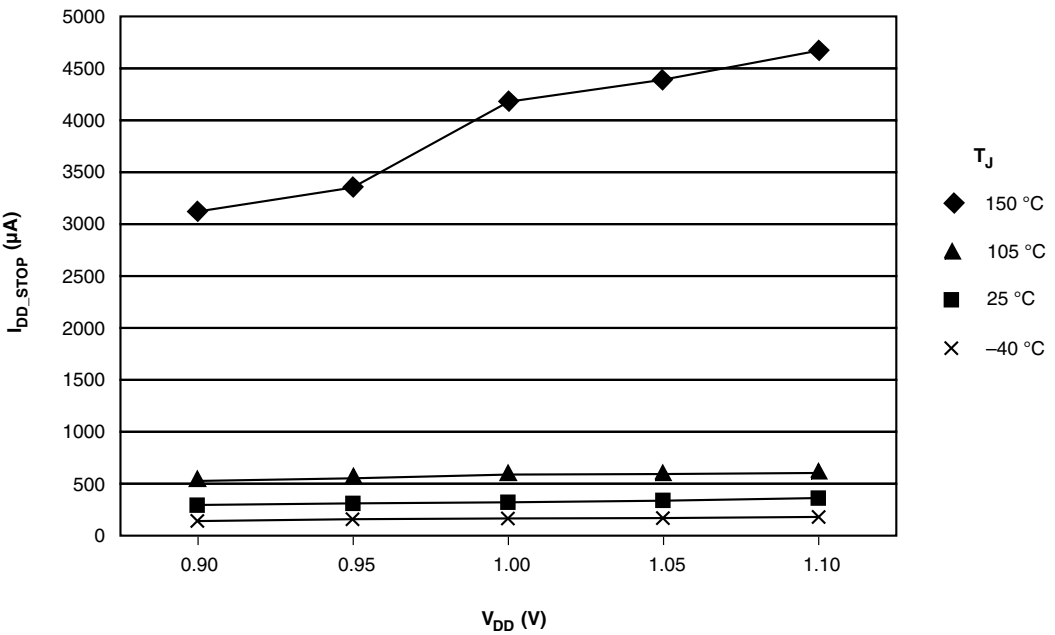
### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{DD}$ | Digital supply current | — | 185 | mA |
| $V_{DIO}$ | Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL) | –0.3 | 5.5 | V |
| $V_{AIO}$ | Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Maximum current single pin limit (applies to all digital pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{USB\_DP}$ | USB_DP input voltage | –0.3 | 3.63 | V |
| $V_{USB\_DM}$ | USB_DM input voltage | –0.3 | 3.63 | V |
| VREGIN | USB regulator input | –0.3 | 6.0 | V |
| $V_{BAT}$ | RTC battery supply voltage | –0.3 | 3.8 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 5 General

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

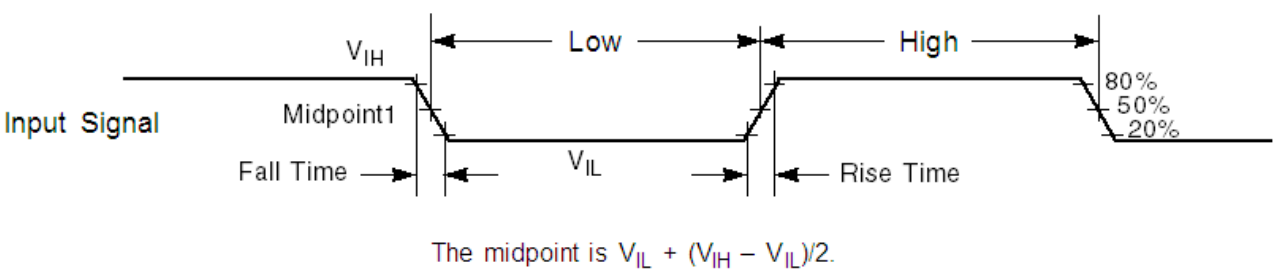



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics assume:

1. output pins
   - have $C_L$=30pF loads,
   - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
   - are configured for high drive strength (PORTx_PCRn[DSE]=1)
2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

## 5.2 Nonswitching electrical specifications

## 5.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} – V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{SS} – V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{BAT}$ | RTC battery supply voltage | 1.71 | 3.6 | V | |
| $V_{IH}$ | Input high voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | <br>0.7 × $V_{DD}$<br>0.75 × $V_{DD}$ | <br>—<br>— | <br>V<br>V | |
| $V_{IL}$ | Input low voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | <br>—<br>— | <br>0.35 × $V_{DD}$<br>0.3 × $V_{DD}$ | <br>V<br>V | |
| $V_{HYS}$ | Input hysteresis | 0.06 × $V_{DD}$ | — | V | |
| $I_{ICDIO}$ | Digital pin negative DC injection current — single pin<br>• $V_{IN}$ < $V_{SS}$-0.3V | -5 | — | mA | 1 |
| $I_{ICAIO}$ | Analog[2], EXTAL, and XTAL pin DC injection current — single pin<br>• $V_{IN}$ < $V_{SS}$-0.3V (Negative current injection)<br>• $V_{IN}$ > $V_{DD}$+0.3V (Positive current injection) | <br>-5<br>— | <br>—<br>+5 | mA | 3 |
| $I_{ICcont}$ | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins<br>• Negative current injection<br>• Positive current injection | <br>-25<br>— | <br>—<br>+25 | mA | |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | |
| $V_{RFVBAT}$ | $V_{BAT}$ voltage required to retain the VBAT register file | $V_{POR\_VBAT}$ | — | V | |

1. All 5 V tolerant digital I/O pins are internally clamped to $V_{SS}$ through a ESD protection diode. There is no diode connection to $V_{DD}$. If $V_{IN}$ greater than $V_{DIO\_MIN}$ (=$V_{SS}$-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=($V_{DIO\_MIN}$-$V_{IN}$)/|$I_{IC}$|.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
3. All analog pins are internally clamped to $V_{SS}$ and $V_{DD}$ through ESD protection diodes. If $V_{IN}$ is greater than $V_{AIO\_MIN}$ (=$V_{SS}$-0.3V) and $V_{IN}$ is less than $V_{AIO\_MAX}$(=$V_{DD}$+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=($V_{AIO\_MIN}$-$V_{IN}$)/|$I_{IC}$|. The positive injection current limiting resistor is calculated as R=($V_{IN}$-$V_{AIO\_MAX}$)/|$I_{IC}$|. Select the larger of these two calculated resistances.

## 5.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -9mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -3mA | $V_{DD}$ – 0.5 | — | V | |
| | Output high voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -2mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -0.6mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 9mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 3mA | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 2mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 0.6mA | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) for full temperature range except TRI0_DM, TRI0_DP, TRI1_DM, TRI1_DP | — | 1 | µA | 1 |
| $I_{IN}$ | Input leakage current (per pin) at 25°C except TRI0_DM, TRI0_DP, TRI1_DM, TRI1_DP | — | 0.025 | µA | 1 |
| $I_{ILKG\_A}$ | Input leakage current (per pin) for TRI0_DM, TRI0_DP, TRI1_DM, TRI1_DP | — | 5 | nA | 1 |
| $I_{OZ}$ | Hi-Z (off-state) leakage current (per pin) | — | 1 | µA | |
| $R_{PU}$ | Internal pullup resistors | 20 | 50 | kΩ | 2 |
| $R_{PD}$ | Internal pulldown resistors | 20 | 50 | kΩ | 3 |

1. Measured at VDD=3.6V
2. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{SS}$
3. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{DD}$

## 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- Flash clock = 24 MHz

## Table 6. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLPW}$ | Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled | — | 0.61 | — | mA | 8 |
| $I_{DD\_STOP}$ | Stop mode current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 0.35 | 0.567 | mA | |
| | • @ 70°C | — | 0.384 | 0.793 | mA | |
| | • @ 105°C | — | 0.628 | 1.2 | mA | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 5.9 | 32.7 | µA | |
| | • @ 70°C | — | 26.1 | 59.8 | µA | |
| | • @ 105°C | — | 98.1 | 188 | µA | |
| $I_{DD\_LLS}$ | Low leakage stop mode current at 3.0 V | | | | | 9 |
| | • @ –40 to 25°C | — | 2.6 | 8.6 | µA | |
| | • @ 70°C | — | 10.3 | 29.1 | µA | |
| | • @ 105°C | — | 42.5 | 92.5 | µA | |
| $I_{DD\_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | | | | | 9 |
| | • @ –40 to 25°C | — | 1.9 | 5.8 | µA | |
| | • @ 70°C | — | 6.9 | 12.1 | µA | |
| | • @ 105°C | — | 28.1 | 41.9 | µA | |
| $I_{DD\_VLLS2}$ | Very low-leakage stop mode 2 current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 1.59 | 5.5 | µA | |
| | • @ 70°C | — | 4.3 | 9.5 | µA | |
| | • @ 105°C | — | 17.5 | 34 | µA | |
| $I_{DD\_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 1.47 | 5.4 | µA | |
| | • @ 70°C | — | 2.97 | 8.1 | µA | |
| | • @ 105°C | — | 12.41 | 32 | µA | |
| $I_{DD\_VBAT}$ | Average current with RTC and 32kHz disabled at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 0.19 | 0.22 | µA | |
| | • @ 70°C | — | 0.49 | 0.64 | µA | |
| | • @ 105°C | — | 2.2 | 3.2 | µA | |

*Table continues on the next page...*

# 6.1 Core modules

## 6.1.1 Debug trace timing specifications

**Table 11. Debug trace operating behaviors**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{cyc}$ | Clock period | Frequency dependent | | MHz |
| $T_{wl}$ | Low pulse width | 2 | — | ns |
| $T_{wh}$ | High pulse width | 2 | — | ns |
| $T_r$ | Clock and data rise time | — | 3 | ns |
| $T_f$ | Clock and data fall time | — | 3 | ns |
| $T_s$ | Data setup | 3 | — | ns |
| $T_h$ | Data hold | 2 | — | ns |

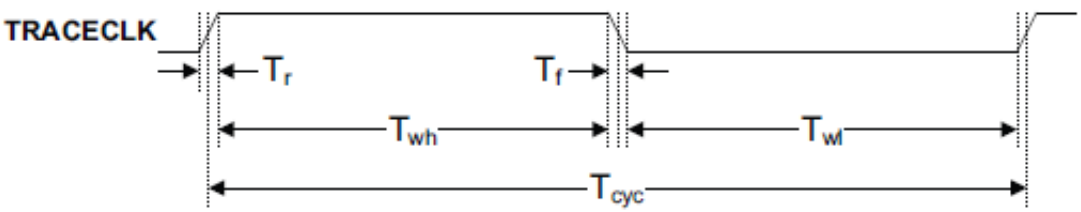



**Figure 4. TRACE_CLKOUT specifications**

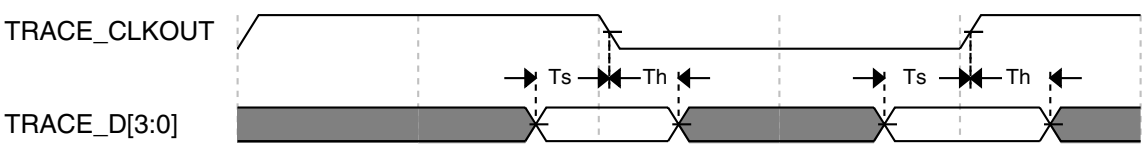



**Figure 5. Trace data specifications**

## 6.1.2 JTAG electricals

**Table 12. JTAG limited voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |

*Table continues on the next page...*

## Table 12. JTAG limited voltage range electricals (continued)

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| J1 | TCLK frequency of operation | | | MHz |
| | • Boundary Scan | 0 | 10 | |
| | • JTAG and CJTAG | 0 | 25 | |
| | • Serial Wire Debug | 0 | 50 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 20 | — | ns |
| | • Serial Wire Debug | 10 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1 | — | ns |
| J11 | TCLK low to TDO data valid | — | 17 | ns |
| J12 | TCLK low to TDO high-Z | — | 17 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

## Table 13. JTAG full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | TCLK frequency of operation | | | MHz |
| | • Boundary Scan | 0 | 10 | |
| | • JTAG and CJTAG | 0 | 20 | |
| | • Serial Wire Debug | 0 | 40 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 25 | — | ns |
| | • Serial Wire Debug | 12.5 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |

*Table continues on the next page...*

4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

**NOTE**

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

## 6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

### 6.3.3.1 32 kHz oscillator DC electrical specifications

**Table 17. 32kHz oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BAT}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $R_F$ | Internal feedback resistor | — | 100 | — | MΩ |
| $C_{para}$ | Parasitical capacitance of EXTAL32 and XTAL32 | — | 5 | 7 | pF |
| $V_{pp}$[1] | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.3.2 32kHz oscillator frequency specifications

**Table 18. 32kHz oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal | — | 32.768 | — | kHz | |
| $t_{start}$ | Crystal start-up time | — | 1000 | — | ms | 1 |
| $v_{ec\_extal32}$ | Externally provided input clock amplitude | 700 | — | $V_{BAT}$ | mV | 2, 3 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and $V_{IH}$ and $V_{IL}$ specifications do not apply. The voltage of the applied clock must be within the range of $V_{SS}$ to $V_{BAT}$.

# 6.4 Memories and memory interfaces

## 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 6.6.1.1 16-bit ADC operating conditions

**Table 24. 16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$ - $V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS}$ - $V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br>• All other modes | VREFL<br>VREFL | —<br>— | 31/32 * VREFH<br>VREFH | V | |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br>• 8-/10-/12-bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 13-/12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 13 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 5 |
| $C_{rate}$ | ADC conversion rate | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | Ksps | 5 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool

### 6.6.1.3 16-bit ADC with PGA operating conditions

**Table 26. 16-bit ADC with PGA operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $V_{REFPGA}$ | PGA ref voltage | | VREF_OUT | VREF_OUT | VREF_OUT | V | 2, 3 |
| $V_{ADIN}$ | Input voltage | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $V_{CM}$ | Input Common Mode range | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $R_{PGAD}$ | Differential input impedance | Gain = 1, 2, 4, 8<br>Gain = 16, 32<br>Gain = 64 | —<br>—<br>— | 128<br>64<br>32 | —<br>—<br>— | kΩ | IN+ to IN-[4] |
| $R_{AS}$ | Analog source resistance | | — | 100 | — | Ω | 5 |
| $T_S$ | ADC sampling time | | 1.25 | — | — | µs | 6 |
| $C_{rate}$ | ADC conversion rate | ≤ 13 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled<br>Peripheral clock = 50 MHz | 18.484 | — | 450 | Ksps | 7 |
| | | 16 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled<br>Peripheral clock = 50 MHz | 37.037 | — | 250 | Ksps | 8 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is $R_{PGAD}/2$
5. The analog source resistance ($R_{AS}$), external to MCU, should be kept as minimum as possible. Increased $R_{AS}$ causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for $F_{in}$=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

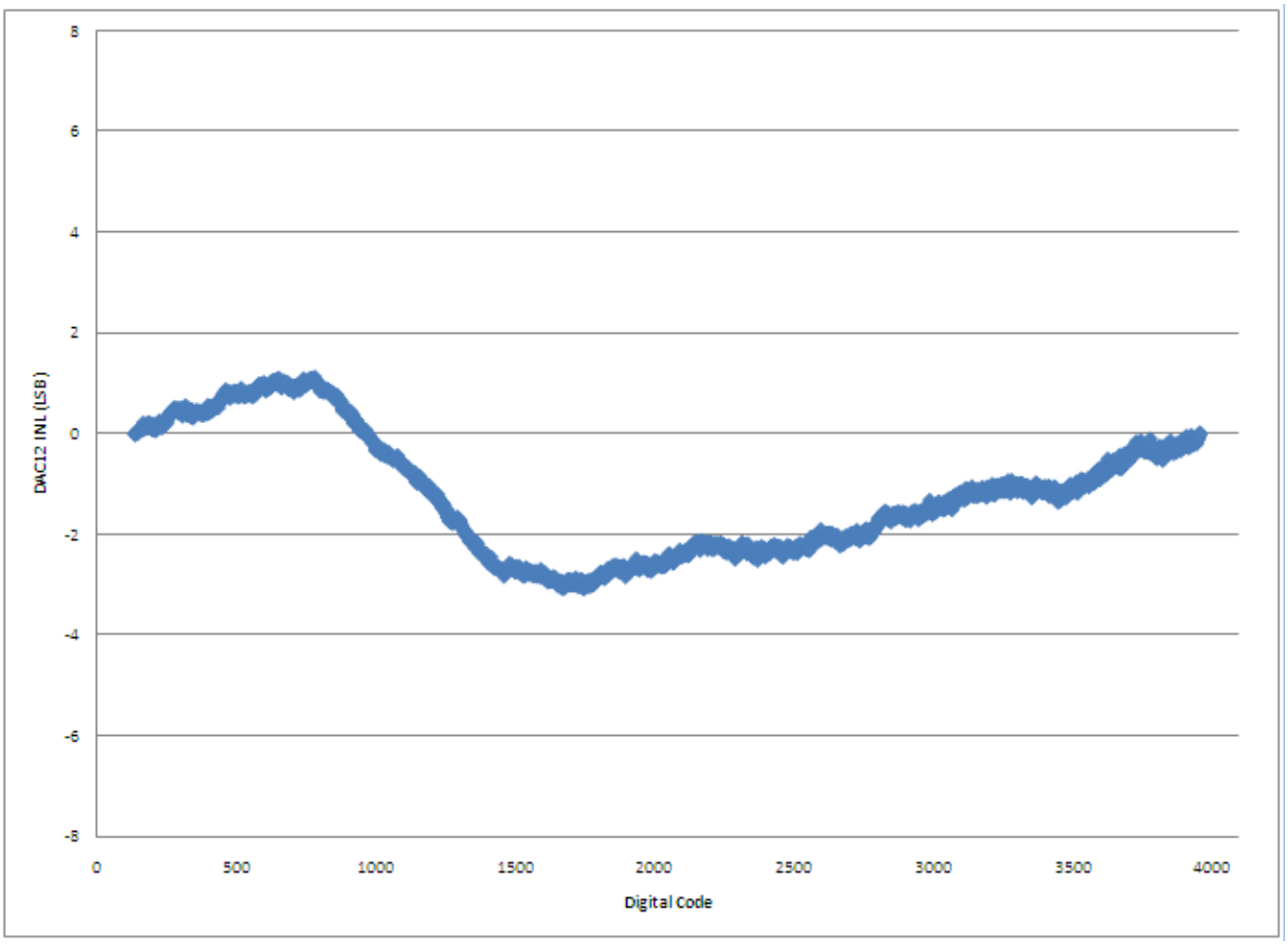



**Figure 17. Typical INL error vs. digital code**

**Table 31. Op-amp electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{BIAS}$ | Typical input bias current across the following temp range (0–50°C) | — | ±500 | — | pA |
| $I_{BIAS}$ | Typical input bias current across the following temp range (-40–105°C) | — | ±4 | — | nA |
| $V_{CML}$ | Input common mode voltage low | 0 | — | — | V |
| $V_{CMH}$ | Input common mode voltage high | — | — | VDD | V |
| $R_{IN}$ | Input resistance | — | 500 | — | MΩ |
| $C_{IN}$ | Input capacitance | — | 17[1] | — | pF |
| $\|X_{IN}\|$ | AC input impedance ($f_{IN}$=100kHz) | — | 50 | — | MΩ |
| CMRR | Input common mode rejection ratio | 60 | — | — | dB |
| PSRR | Power supply rejection ratio | 60 | — | — | dB |
| SR | Slew rate ($\Delta V_{IN}$=500mV), low-power mode | 0.1 | — | — | V/µs |
| SR | Slew rate ($\Delta V_{IN}$=500mV), high-speed mode | 1.5 | 4 | — | V/µs |
| GBW | Unity gain bandwidth, low-power mode | 0.15 | — | — | MHz |
| GBW | Unity gain bandwidth, high-speed mode | 1 | — | — | MHz |
| $A_V$ | DC open-loop voltage gain | 80 | 90 | — | dB |
| CL(max) | Load capacitance driving capability | — | 100 | — | pF |
| $R_{OUT}$ | Output resistance @ 100 kHz, high speed mode | — | 1500 | — | Ω |
| $V_{OUT}$ | Output voltage range | 0.12 | — | VDD - 0.12 | V |
| $I_{OUT}$ | Output load current | — | ±0.5 | — | mA |
| GM | Gain margin | — | 20 | — | dB |
| PM | Phase margin | 45 | 56 | — | deg |
| $T_{settle}$ | Settling time[2] (Buffer mode, low-power mode) (To<0.1%, $V_{in}$=1.65V) | — | 5.7 | — | µs |
| $T_{settle}$ | Settling time[2] (Buffer mode, high-speed mode) (To<0.1%, $V_{in}$=1.65V) | — | 3.0 | — | µs |
| Vn | Voltage noise density (noise floor) 1kHz | — | 350 | — | nV/√Hz |
| Vn | Voltage noise density (noise floor) 10kHz | — | 90 | — | nV/√Hz |

1. The input capacitance is dependant on the package type used.
2. Settling time is measured from the time the Op-amp is enabled until the output settles to within 0.1% of final value. This time includes Op-amp startup time, output slew, and settle time.

## 6.6.5 Transimpedance amplifier electrical specifications — full range

**Table 32. TRIAMP full range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{IN}$ | Input voltage range | -0.1 | $V_{DDA}$-1.4 | V | |
| $C_L$ | Output load capacitance | — | 100 | pf | |

## 6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 42. Master mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 25 | MHz | |
| DS1 | DSPI_SCK output cycle time | 2 x $t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns | |
| DS3 | DSPI_PCS*n* valid to DSPI_SCK delay | ($t_{BUS}$ x 2) – 2 | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | ($t_{BUS}$ x 2) – 2 | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | –2 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 15 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

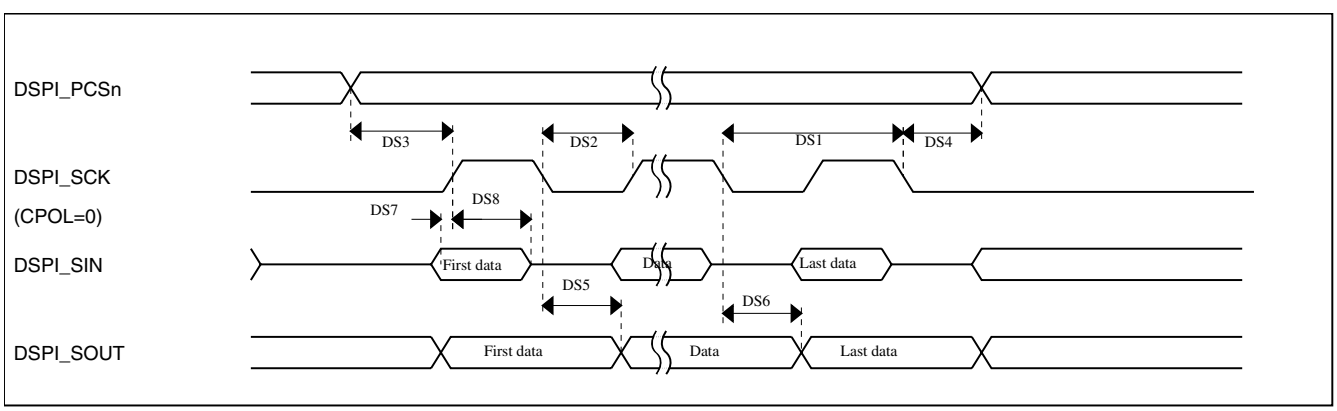



**Figure 19. DSPI classic SPI timing — master mode**

**Table 43. Slave mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | | 12.5 | MHz |
| DS9 | DSPI_SCK input cycle time | 4 x $t_{BUS}$ | — | ns |

*Table continues on the next page...*

**Table 50. TSI electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{ELE}$ | Electrode oscillator current source base current<br>• 2 µA setting (EXTCHRG = 0)<br>• 32 µA setting (EXTCHRG = 15) | —<br>— | 2<br>36 | 3<br>50 | µA | 2, 7 |
| Pres5 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | fF/count | 8 |
| Pres20 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | fF/count | 9 |
| Pres100 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | fF/count | 10 |
| MaxSens | Maximum sensitivity | 0.008 | 1.46 | — | fF/count | 11 |
| Res | Resolution | — | — | 16 | bits | |
| $T_{Con20}$ | Response time @ 20 pF | 8 | 15 | 25 | µs | 12 |
| $I_{TSI\_RUN}$ | Current added in run mode | — | 55 | — | µA | |
| $I_{TSI\_LP}$ | Low power mode current adder | — | 1.3 | 2.5 | µA | 13 |

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. REFCHRG = 2, EXTCHRG=0.
4. REFCHRG = 0, EXTCHRG = 10.
5. $V_{DD}$ = 3.0 V.
6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: $(C_{ref} * I_{ext})/( I_{ref} * PS * NSCN)$

    The typical value is calculated with the following configuration:

    $I_{ext} = 6$ µA (EXTCHRG = 2), PS = 128, NSCN = 2, $I_{ref} = 16$ µA (REFCHRG = 7), $C_{ref}$ = 1.0 pF

    The minimum value is calculated with the following configuration:

    $I_{ext} = 2$ µA (EXTCHRG = 0), PS = 128, NSCN = 32, $I_{ref} = 32$ µA (REFCHRG = 15), $C_{ref}$ = 0.5 pF

    The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.
12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

## 6.9.2 LCD electrical characteristics

**Table 51. LCD electricals**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{Frame}$ | LCD frame frequency | 28 | 30 | 58 | Hz | |
| $C_{LCD}$ | LCD charge pump capacitance — nominal value | — | 100 | — | nF | 1 |
| $C_{BYLCD}$ | LCD bypass capacitance — nominal value | — | 100 | — | nF | 1 |
| $C_{Glass}$ | LCD glass capacitance | — | 2000 | 8000 | pF | 2 |

*Table continues on the next page...*

# 8 Pinout

## 8.1 K51 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 64 LQFP _QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VDD | VDD | VDD | | | | | | | | |
| 2 | VSS | VSS | VSS | | | | | | | | |
| 3 | USB0_DP | USB0_DP | USB0_DP | | | | | | | | |
| 4 | USB0_DM | USB0_DM | USB0_DM | | | | | | | | |
| 5 | VOUT33 | VOUT33 | VOUT33 | | | | | | | | |
| 6 | VREGIN | VREGIN | VREGIN | | | | | | | | |
| 7 | ADC1_DP1/ OP1_DP0/ OP1_DM1 | ADC1_DP1/ OP1_DP0/ OP1_DM1 | ADC1_DP1/ OP1_DP0/ OP1_DM1 | | | | | | | | |
| 8 | ADC1_DM1/ OP1_DM0 | ADC1_DM1/ OP1_DM0 | ADC1_DM1/ OP1_DM0 | | | | | | | | |
| 9 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | | | | | | | | |
| 10 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | | | | | | | | |
| 11 | VDDA | VDDA | VDDA | | | | | | | | |
| 12 | VREFH | VREFH | VREFH | | | | | | | | |
| 13 | VREFL | VREFL | VREFL | | | | | | | | |
| 14 | VSSA | VSSA | VSSA | | | | | | | | |
| 15 | ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2 | ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2 | ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2 | | | | | | | | |
| 16 | ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1 | ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1 | ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1 | | | | | | | | |
| 17 | VREF_OUT/ CMP1_IN5/ | VREF_OUT/ CMP1_IN5/ | VREF_OUT/ CMP1_IN5/ | | | | | | | | |

| 64 LQFP _QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | CMP0_IN5/ ADC1_SE18 | CMP0_IN5/ ADC1_SE18 | CMP0_IN5/ ADC1_SE18 | | | | | | | | |
| 18 | TRI0_OUT/ OP1_DM2 | TRI0_OUT/ OP1_DM2 | TRI0_OUT/ OP1_DM2 | | | | | | | | |
| 19 | TRI0_DM | TRI0_DM | TRI0_DM | | | | | | | | |
| 20 | TRI0_DP | TRI0_DP | TRI0_DP | | | | | | | | |
| 21 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4 | | | | | | | | |
| 22 | XTAL32 | XTAL32 | XTAL32 | | | | | | | | |
| 23 | EXTAL32 | EXTAL32 | EXTAL32 | | | | | | | | |
| 24 | VBAT | VBAT | VBAT | | | | | | | | |
| 25 | PTA0 | JTAG_TCLK/ SWD_CLK/ EZP_CLK | TSI0_CH1 | PTA0 | UART0_CTS_ b/ UART0_COL_b | FTM0_CH5 | | | | JTAG_TCLK/ SWD_CLK | EZP_CLK |
| 26 | PTA1 | JTAG_TDI/ EZP_DI | TSI0_CH2 | PTA1 | UART0_RX | FTM0_CH6 | | | | JTAG_TDI | EZP_DI |
| 27 | PTA2 | JTAG_TDO/ TRACE_SWO/ EZP_DO | TSI0_CH3 | PTA2 | UART0_TX | FTM0_CH7 | | | | JTAG_TDO/ TRACE_SWO | EZP_DO |
| 28 | PTA3 | JTAG_TMS/ SWD_DIO | TSI0_CH4 | PTA3 | UART0_RTS_b | FTM0_CH0 | | | | JTAG_TMS/ SWD_DIO | |
| 29 | PTA4/ LLWU_P3 | NMI_b/ EZP_CS_b | TSI0_CH5 | PTA4/ LLWU_P3 | | FTM0_CH1 | | | | NMI_b | EZP_CS_b |
| 30 | VDD | VDD | VDD | | | | | | | | |
| 31 | VSS | VSS | VSS | | | | | | | | |
| 32 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | | |
| 33 | PTA19 | XTAL0 | XTAL0 | PTA19 | | FTM1_FLT0 | FTM_CLKIN1 | | LPTMR0_ALT1 | | |
| 34 | RESET_b | RESET_b | RESET_b | | | | | | | | |
| 35 | PTB0/ LLWU_P5 | LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | | | FTM1_QD_ PHA | LCD_P0 | |
| 36 | PTB1 | LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6 | LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSI0_CH6 | PTB1 | I2C0_SDA | FTM1_CH1 | | | FTM1_QD_ PHB | LCD_P1 | |
| 37 | PTB2 | LCD_P2/ ADC0_SE12/ TSI0_CH7 | LCD_P2/ ADC0_SE12/ TSI0_CH7 | PTB2 | I2C0_SCL | UART0_RTS_b | | | FTM0_FLT3 | LCD_P2 | |
| 38 | PTB3 | LCD_P3/ ADC0_SE13/ TSI0_CH8 | LCD_P3/ ADC0_SE13/ TSI0_CH8 | PTB3 | I2C0_SDA | UART0_CTS_ b/ UART0_COL_b | | | FTM0_FLT0 | LCD_P3 | |
| 39 | PTB16 | LCD_P12/ TSI0_CH9 | LCD_P12/ TSI0_CH9 | PTB16 | | UART0_RX | | | EWM_IN | LCD_P12 | |

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