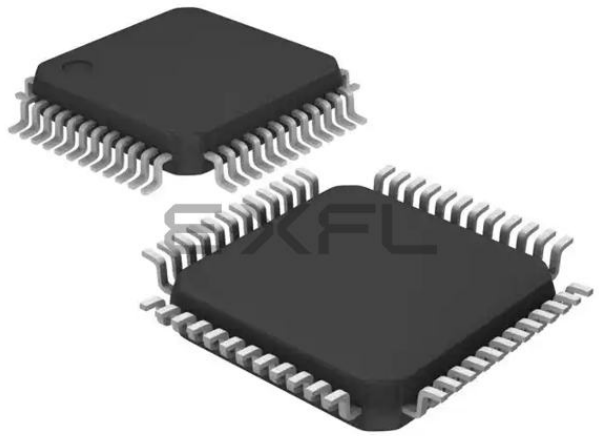


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	10MHz
Connectivity	SIO, UART/USART
Peripherals	PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-30°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-SQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f5g32auwa-2h

■PWM: Multifrequency 12-bit PWM × 2-channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts
- 22 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority Levels: X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 512 levels (the stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16-bits × 8-bits (5 tCYC execution time)
- 24-bits × 16-bits (12 tCYC execution time)
- 16-bits ÷ 8-bits (8 tCYC execution time)
- 24-bits ÷ 16-bits (12 tCYC execution time)

■Oscillation Circuits
- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, with internal Rf
- Crystal oscillation circuit: For low-speed system clock, with internal Rf
- Frequency variable RC oscillation circuit (internal): For system clock

■System Clock Divider Function
- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■Standby Function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode : Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, and crystal oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level.
     (3) Having an interrupt source established at port 0.
- X'tal HOLD mode : Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF and RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are four ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level.
     (3) Having an interrupt source established at port.
     (4) Having an interrupt source established in the base timer circuit.

■Onchip Debugger

- Supports software debugging with the IC mounted on the target board.

■Package Form

- QIP48E(14×14): “Lead-free type”
- SQFP48(7×7): “Lead-free type”

■Development Tools

- Evaluation chip: LC87EV690
- Emulator: EVA62S + ECB876600D + SUB875G00 + POD48QFP
  ICE-B877300 + SUB875G00 + POD48QFP
- Onchip debugger: TCB87 TypeA + LC87F5G32A
  TCB87 TypeB + LC87F5G32A

■Flash ROM Programming boards

Package	Programming boards
QIP48E(14×14)	W87F55256Q
SQFP48(7×7)	W87F55256SQ

■Flash ROM programmer

Maker	Model		Supported version (Note)	Device
Flash Support Group, Inc. (Formerly Ando Electric Co., Ltd.)	Single	AF9708/AF9709/ AF9709B	After 02.40	LC87F5G32A FAST
	Gang	AF9723 (Main body)	After 02.04	
		AF9833 (Unit)	After 01.84	
Our company	SKK (SANYO FWS)		After 1.02C (Install CD)	LC87F5G32A

Note: Please check the latest version.

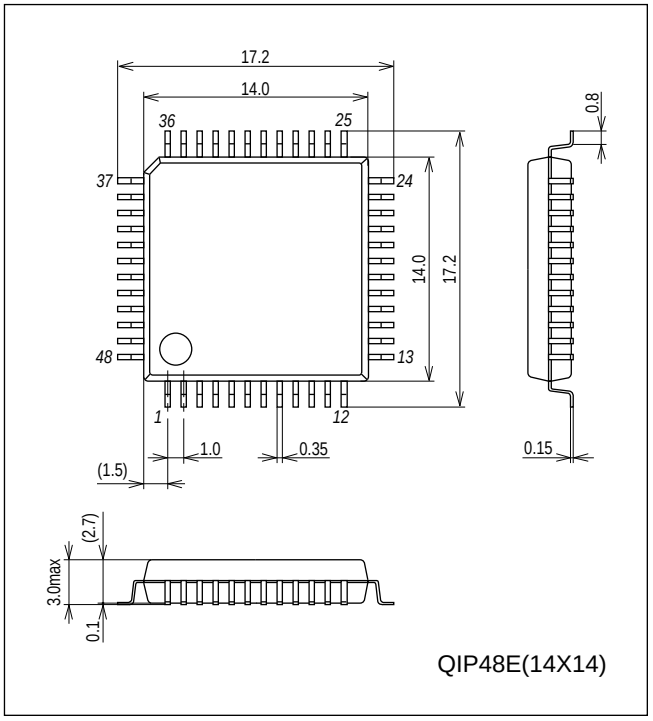
■Same package and pin assignment as mask ROM version.

1) LC875G00 series options can be set by using flash ROM data. Thus the board used for mass production can be used for debugging and evaluation without modifications.
2) If the program for the mask ROM version is used, the usable ROM/RAM capacity is the same as the mask ROM version.

Package Dimensions

unit : mm (typ)

3156A

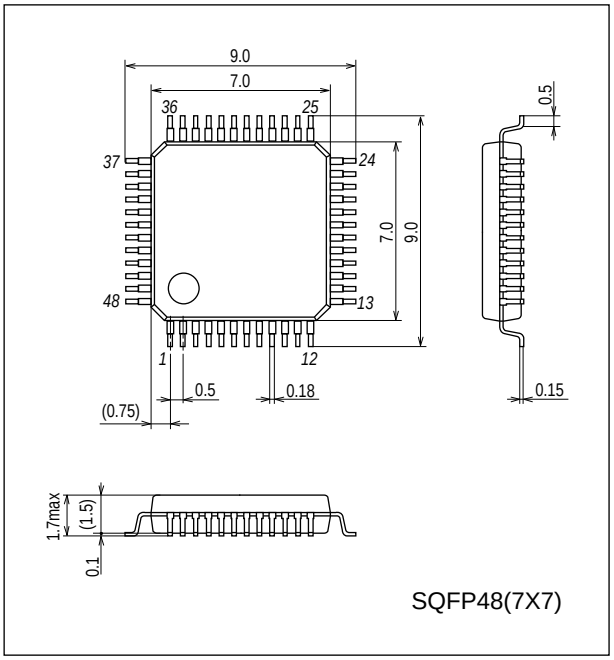


QIP48E(14X14)

Package Dimensions

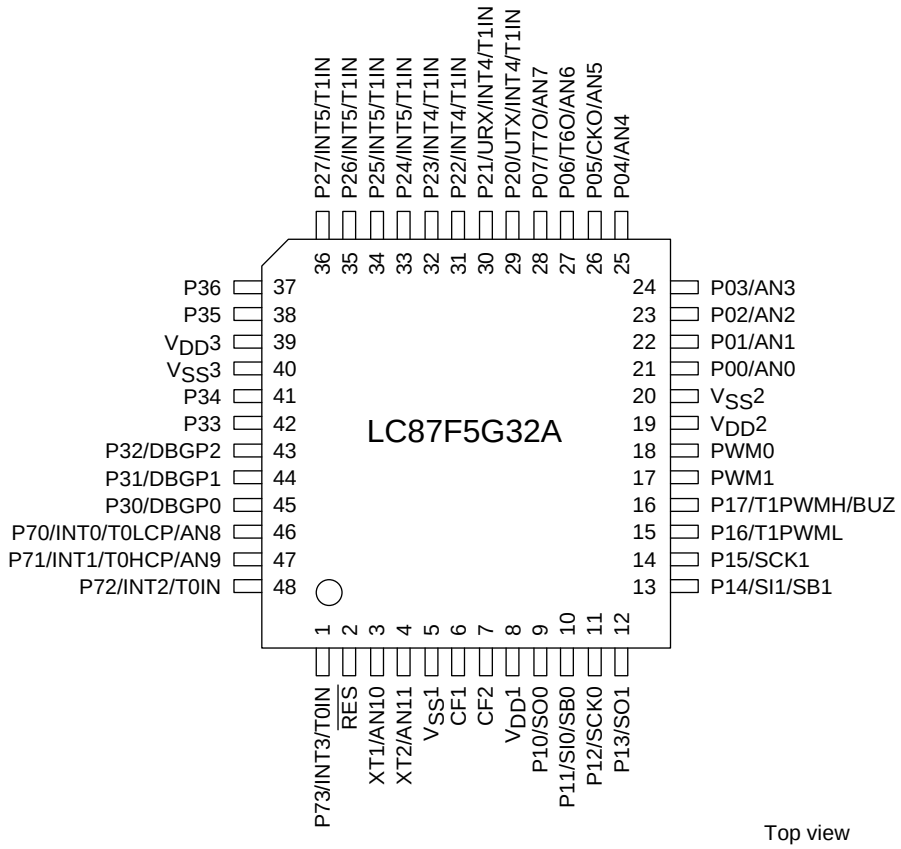
unit : mm (typ)

3163B



SQFP48(7X7)

Pin Assignment



Top view

QIP48E(14×14) "Lead-free Type"

SQFP48(7×7) "Lead-free Type"

SQFP/QIP	NAME
1	P73/INT3/T0IN
2	$\overline{RES}$
3	XT1/AN10
4	XT2/AN11
5	$V_{SS}1$
6	CF1
7	CF2
8	$V_{DD}1$
9	P10/SO0
10	P11/SI0/SB0
11	P12/SCK0
12	P13/SO1
13	P14/SI1/SB1
14	P15/SCK1
15	P16/T1PWML
16	P17/T1PWMH/BUZ
17	PWM1
18	PWM0
19	$V_{DD}2$
20	$V_{SS}2$
21	P00/AN0
22	P01/AN1
23	P02/AN2
24	P03/AN3

SQFP/QIP	NAME
25	P04/AN4
26	P05/CKO/AN5
27	P06/T6O/AN6
28	P07/T7O/AN7
29	P20/UTX/INT4/T1IN
30	P21/URX/INT4/T1IN
31	P22/INT4/T1IN
32	P23/INT4/T1IN
33	P24/INT5/T1IN
34	P25/INT5/T1IN
35	P26/INT5/T1IN
36	P27/INT5/T1IN
37	P36
38	P35
39	$V_{DD}3$
40	$V_{SS}3$
41	P34
42	P33
43	P32/DBGP2
44	P31/DBGP1
45	P30/DBGP0
46	P70/INT0/T0LCP/AN8
47	P71/INT1/T0HCP/AN9
48	P72/INT2/T0IN

Pin Function Chart

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$
$V_{SS}2$
$V_{SS}3$</td><td>-</td><td>- Power supply pin</td><td>Yes</td></tr>
<tr><td>$V_{DD}1$
$V_{DD}2$
$V_{DD}3$</td><td>-</td><td>+ Power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistors can be turned on and off in 4-bit units
• HOLD reset input
• Port 0 interrupt input
• Shared pins
P05: System clock output
P06: Timer 6 toggle output
P07: Timer 7 toggle output
AD converter input port: AN0 (P00) to AN7 (P07)</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units
• Pin functions
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: Timer 1PWML output
P17: Timer 1PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units
• Pin functions
P20: UART transmit
P21: UART receive
P20 to P23: INT4 input/HOLD reset input/timer 1 event input/
timer 0L capture input/timer 0H capture input
P24 to P27: INT5 input/HOLD reset input/timer 1 event input/
timer 0L capture input/timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
</td><td>Yes</td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 3
P30 to P36</td><td>I/O</td><td>• 7-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units
• Shared pins
On-chip debugger pins: DBGP0 to DBGP2 (P30 to P32)</td><td>Yes</td></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units
• Shared pins
AD converter input port : AN8 (P70), AN9 (P71)
P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD reset input/timer 0H capture input
P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input
P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>PWM0, PWM1</td><td>I/O</td><td>• PWM0 and PWM1 output ports
• General-purpose I/O available</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input pin
• Shared pins
General-purpose input port
AD converter input port: AN10
Must be connected to $V_{DD}1$ if not to be used</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output pin
• Shared pins
General-purpose I/O port
AD converter input port: AN11
Must be set for oscillation and kept open if not to be used</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>Ceramic resonator input pin</td><td>No</td></tr>
<tr><td>CF2</td><td>Output</td><td>Ceramic resonator output pin</td><td>No</td></tr>
</table>

Port Output Types

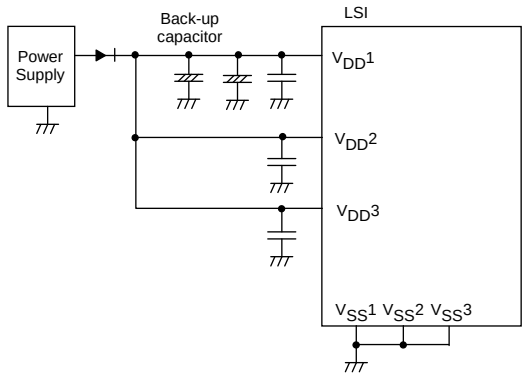
The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1-bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P36	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
PWM0, PWM1	-	No	CMOS	No
XT1	-	No	Input for 32.768kHz crystal oscillator (Input only)	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

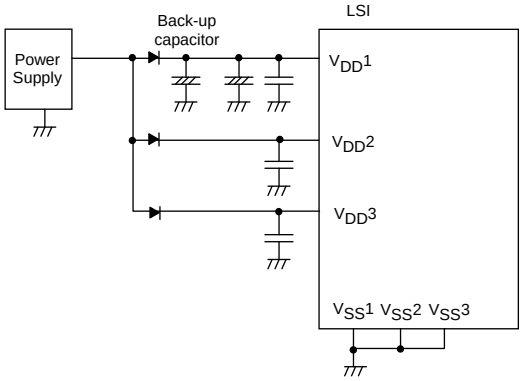
Note 1: Programmable pull-up resistor of Port 0 is specified in nibble units (P00 to P03, P04 to P07).

Note: To reduce V_{DD} signal noise and to increase the duration of the backup battery supply, $V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ should connect to each other and they should also be grounded.

Example 1: During backup in hold mode, port output 'H' level is supplied from the back-up capacitor.



Example 2: During backup in hold mode, output is not held high and its value in unsettled.



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+6.5	V
Input voltage		VI	XT1, CF1			-0.3		V_{DD}+0.3	
Input/output voltage		VIO	Ports 0, 1, 2, 3 Port 7, PWM0, PWM1, XT2			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-10			mA
		IOPH(2)	PWM0, PWM1	CMOS output select Per 1 applicable pin		-20			
		IOPH(3)	Ports P71 to P73	Per 1 applicable pin		-5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-7.5			
		IOMH(2)	PWM0, PWM1	CMOS output select Per 1 applicable pin		-15			
		IOMH(3)	Ports P71 to P73	Per 1 applicable pin		-3			
	Total output current	ΣIOAH(1)	Ports P71 to P73	Total of all applicable pins		-10			
		ΣIOAH(2)	Port 0	Total of all applicable pins		-25			
		ΣIOAH(3)	Ports 1, PWM0, PWM1	Total of all applicable pins		-25			
		ΣIOAH(4)	Ports 0, 1 PWM0, PWM1	Total of all applicable pins		-45			
		ΣIOAH(5)	Ports 2, P35, P36	Total of all applicable pins		-25			
		ΣIOAH(6)	Ports P30 to P34	Total of all applicable pins		-25			
		ΣIOAH(7)	Ports 2, 3	Total of all applicable pins		-45			
Low level output current	Peak output current	IOPL(1)	Ports P02 to P07 Ports 1, 2, 3 PWM0, PWM1	Per 1 applicable pin				20	
		IOPL(2)	Ports P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Port 7, XT2	Per 1 applicable pin				10	
	Mean output current (Note 1-1)	IOML(1)	Ports P02 to P07 Ports 1, 2, 3 PWM0, PWM1	Per 1 applicable pin				15	
		IOML(2)	Ports P00, P01	Per 1 applicable pin				20	
		IOML(3)	Port 7, XT2	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Port 7, XT2	Total of all applicable pins				15	
		ΣIOAL(2)	Port 0	Total of all applicable pins				45	
		ΣIOAL(3)	Ports 1, PWM0, PWM1	Total of all applicable pins				45	
		ΣIOAL(4)	Ports 0, 1 PWM0, PWM1	Total of all applicable pins				80	
		ΣIOAL(5)	Ports 2, P35, P36	Total of all applicable pins				45	
		ΣIOAL(6)	Ports P30 to P34	Total of all applicable pins				45	
		ΣIOAL(7)	Ports 2, 3	Total of all applicable pins				60	
Power dissipation		Pd max	SQFP48(7×7)	Ta= -30 to +70°C				190	mW
			QIP48E(14×14)					390	
Operating ambient temperature		Topr				-30		+70	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	0.294µs ≤ tCYC ≤ 200µs		4.0		5.5	V
	$V_{DD}(2)$		0.367µs ≤ tCYC ≤ 200µs		3.0		5.5	
	$V_{DD}(3)$		0.588µs ≤ tCYC ≤ 200µs		2.5		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}3$	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 3 P71 to P73 P70 port input/ interrupt side PWM0, PWM1		2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Port 0		2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	Port 70 watchdog timer side		2.5 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3 P71 to P73 P70 port input/ interrupt side PWM0, PWM1		4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
				2.5 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Port 0		4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
				2.5 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Port 70 watchdog timer side		2.5 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(4)$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-1)	tCYC (Note 2-2)			4.0 to 5.5	0.294		200	µs
				3.0 to 5.5	0.367		200	
				2.5 to 5.5	0.588		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	4.0 to 5.5	0.1		10	MHz
				2.5 to 5.5	0.1		5	
			• CF2 pin open • System clock frequency division ratio=1/2	4.0 to 5.5	0.2		20.4	
				2.5 to 5.5	0.1		10	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	10MHz ceramic oscillation See Fig 1.	4.0 to 5.5		10		MHz
	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig 1.	3.0 to 5.5		8		
	FmCF(3)	CF1, CF2	5MHz ceramic oscillation See Fig 1.	2.5 to 5.5		5		
	FmRC		Internal RC oscillation	2.5 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.5 to 5.5		16		
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig 2.	2.5 to 5.5		32.768		kHz

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$ PWM0, PWM1	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.5 to 5.5			1	μA
	$I_{IH}(2)$	XT1, XT2	For input port specification $V_{IN}=V_{DD}$	2.5 to 5.5			1	
	$I_{IH}(3)$	CF1	$VIN=V_{DD}$	2.5 to 5.5			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$ PWM0, PWM1	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.5 to 5.5	-1			
	$I_{IL}(2)$	XT1, XT2	For input port specification $V_{IN}=V_{SS}$	2.5 to 5.5	-1			
	$I_{IL}(3)$	CF1	$V_{IN}=V_{SS}$	2.5 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3	I_{OH}= -1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}= -0.1mA	2.5 to 5.5	V_{DD}-0.5			
	$V_{OH}(3)$	P71 to P73	I_{OH}= -0.4mA	4.5 to 5.5	V_{DD}-1			
	$V_{OH}(4)$	PWM0, PWM1, P05(System clock output function used)	I_{OH}= -6mA	4.5 to 5.5	V_{DD}-1			
	$V_{OH}(5)$		I_{OH}= -1.6mA	4.5 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$		I_{OH}= -1mA	2.5 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3, PWM0, PWM1, XT2	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.6mA	4.5 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=1mA	2.5 to 5.5			0.4	
	$V_{OL}(4)$	P00, P01	I_{OL}=30mA	4.5 to 5.5			1.5	
	$V_{OL}(5)$	Port 7	I_{OL}=1mA	2.5 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$	2.5 to 4.5	18	50	150	
Hysteresis voltage	VHYS	$\overline{RES}$ Ports 1, 2, 7		2.5 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.5 to 5.5		10		pF

Serial Input/Output Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. • (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.5 to 5.5	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(1)			2.5 to 5.5	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.5 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.5 to 5.5			1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)	2.5 to 5.5			(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.5 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(2)			2.5 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.5 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Resetting is enabled.	2.5 to 5.5	200			µs

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12-bits AD Converter Mode / Ta= -10°C to +50°C>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		4.75 to 5.25		12		bit
Absolute accuracy	ET		(Note 6-1)	4.75 to 5.25			T.B.D	LSB
Conversion time	TCAD		See conversion time calculation formulas. (Note 6-2)	4.75 to 5.25	38.5		90	µs
Analog input voltage range	VAIN			4.75 to 5.25	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	4.75 to 5.25			1	µA
	IAINL		VAIN=V_{SS}	4.75 to 5.25	-1			

<8-bits AD Converter Mode / Ta= -30°C to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		See conversion time calculation formulas. (Note 6-2)	4.5 to 5.5	22.5		90	µs
				3.0 to 5.5	45		90	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Conversion time calculation formulas:

12-bits AD Converter Mode: TCAD (Conversion time) = ((52/(division ratio))+2) × (1/3) × tCYC

8-bits AD Converter Mode: TCAD (Conversion time) = ((32/(division ratio))+2) × (1/3) × tCYC

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Consumption Current Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	Max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1 = V_{DD}2 = V_{DD}3$	• FmCF=10MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio	4.0 to 5.5		7.7	20	mA
	IDDOP(2)		• CF1=20MHz external clock • FsX'tal=32.768kHz crystal oscillation mode • System clock set to CF1 side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio	4.0 to 5.5		8.7	20	
	IDDOP(3)		• FmCF=5MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 5MHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		5.2	12	
	IDDOP(4)			4.5 to 5.5		3.5	10	
	IDDOP(5)		• FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		0.7	2.9	
	IDDOP(6)			2.5 to 4.5		0.4	2.1	
	IDDOP(7)		• FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped • System clock set to 1MHz with frequency variable RC oscillation • 1/2 frequency division ratio	4.5 to 5.5		1.4	5.3	
	IDDOP(8)			2.5 to 4.5		0.9	3.9	
	IDDOP(9)		• FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		34	90	µA
	IDDOP(10)			2.5 to 4.5		23	70	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• HALT mode • FmCF=10MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio	4.0 to 5.5		3.1	6	mA
	IDDHALT(2)		• HALT mode • CF1=20MHz external clock • FsX'tal=32.768kHz crystal oscillation mode • System clock set to CF1 side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio	4.0 to 5.5		4	9	
	IDDHALT(3)		• HALT mode • FmCF=5MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 5MHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		1.9	4.1	
	IDDHALT(4)			2.5 to 4.5		1.3	3.0	
	IDDHALT(5)		• HALT mode • FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		0.35	1.4	
	IDDHALT(6)			2.5 to 4.5		0.25	0.95	
	IDDHALT(7)		• HALT mode • FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped • System clock set to 1MHz with frequency variable RC oscillation • 1/2 frequency division ratio	4.5 to 5.5		1.1	4	
	IDDHALT(8)			2.5 to 4.5		0.8	3.0	
	IDDHALT(9)		• HALT mode • FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		20	51	μA
	IDDHALT(10)			2.5 to 4.5		18	35	
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	HOLD mode • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.04	11	
	IDDHOLD(2)			2.5 to 4.5		0.01	8	
Timer HOLD mode consumption current	IDDHOLD(3)	$V_{DD}1$	Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		17	50	
	IDDHOLD(4)			2.5 to 4.5		12	30	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

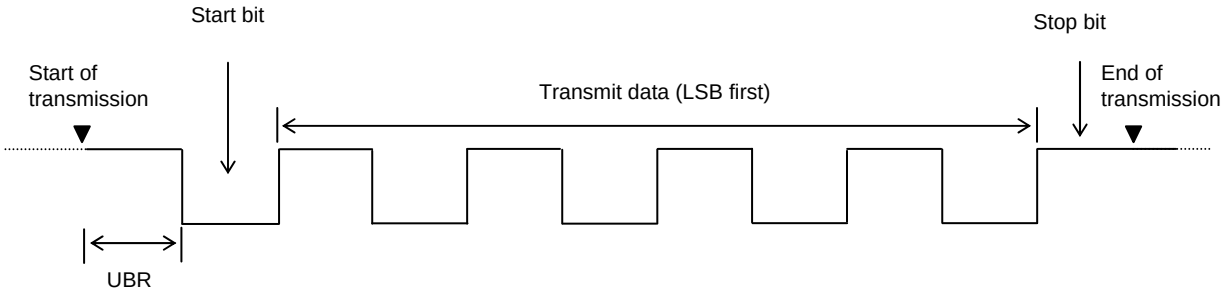
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW	$V_{DD}1$	• 128-byte programming • Erasing current included	3.0 to 5.5		25	40	mA
Programming time	tFW		• 128-byte programming • Erasing current included • Time for setting up 128-byte data is excluded.	3.0 to 5.5		22.5	45	ms

UART (Full duplex) Operating Conditions at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

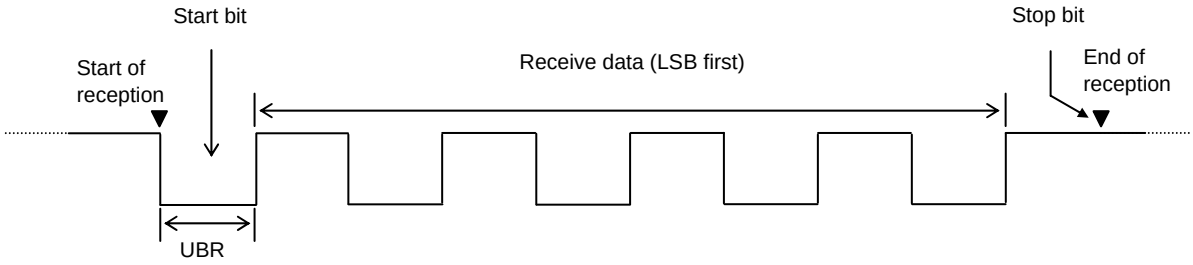
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	P20, P21		2.5 to 5.5	16/3		8192/3	tCYC

Data length: 7, 8, and 9 bits (LSB first)
Stop bits: 1-bit (2-bit in continuous data transmission)
Parity bits: Non

Example of Continuous 8-bit Data Transmission Mode Processing (first transmit data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (first receive data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
10MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	Open	680	4.0 to 5.5	0.1	0.5	Internal C1, C2 (SMD type)
		CSTCE10M0G52-B0	(10)	(10)	Open	680	4.0 to 5.5	0.1	0.5	
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	1.0k	3.0 to 5.5	0.1	0.5	Internal C1, C2 (SMD type)
		CSTCE8M00G52-B0	(10)	(10)	Open	1.0k	3.0 to 5.5	0.1	0.5	
5MHz	MURATA	CSTCR5M00G53-R0	(15)	(15)	Open	2.2k	2.5 to 5.5	0.2	0.6	Internal C1, C2 (SMD type)
		CSTCR5M00G53-B0	(15)	(15)	Open	2.2k	2.5 to 5.5	0.2	0.6	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).
It is recommended to insert feedback resister(Rf:1MΩ) when power supply voltage is used around 2.5V.

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	Open	510k	2.5 to 5.5	1.1	3.0	Applicable CL value=12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

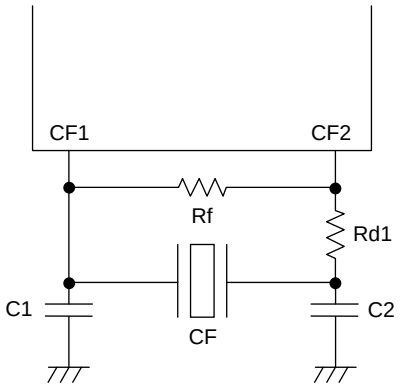


Figure 1 CF Oscillator Circuit

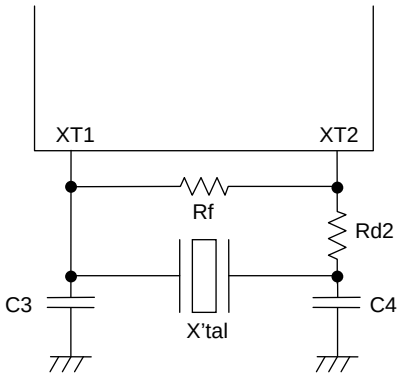


Figure 2 XT Oscillator Circuit

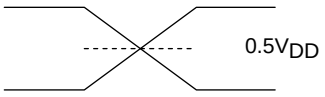
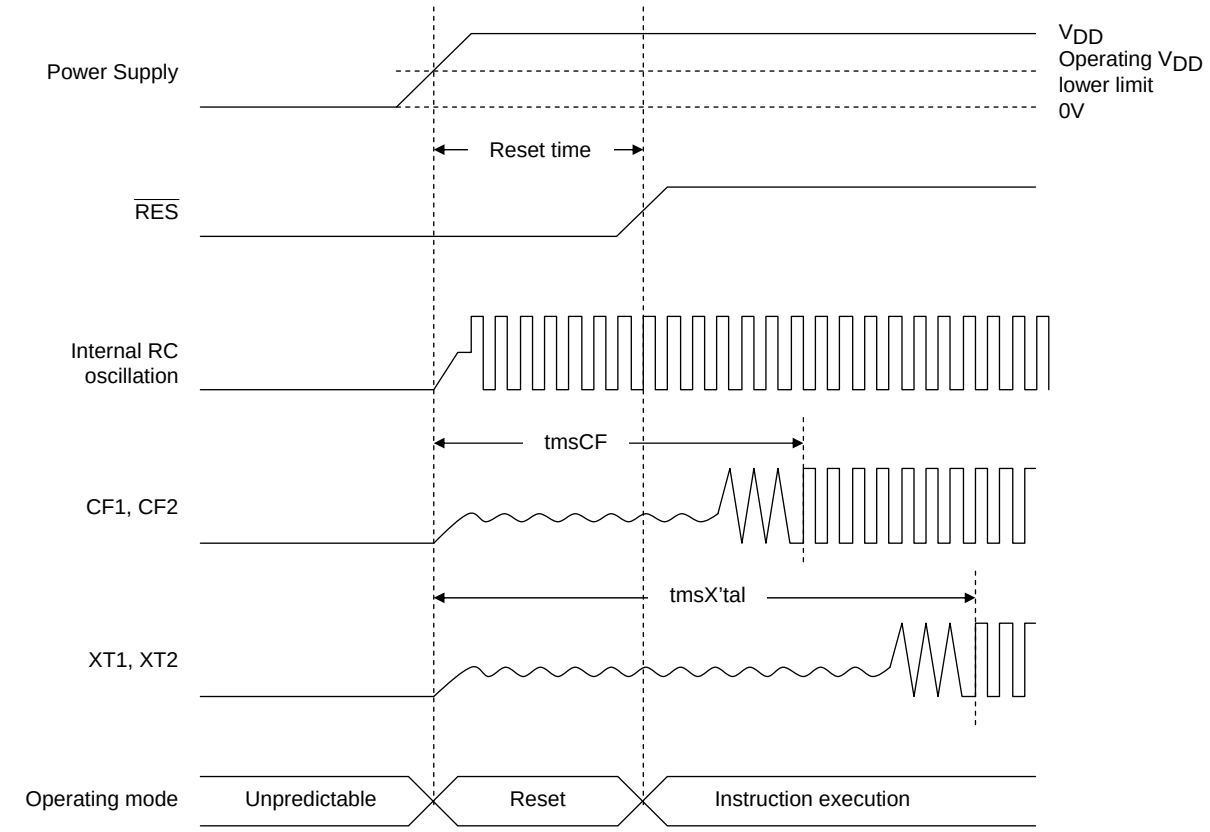
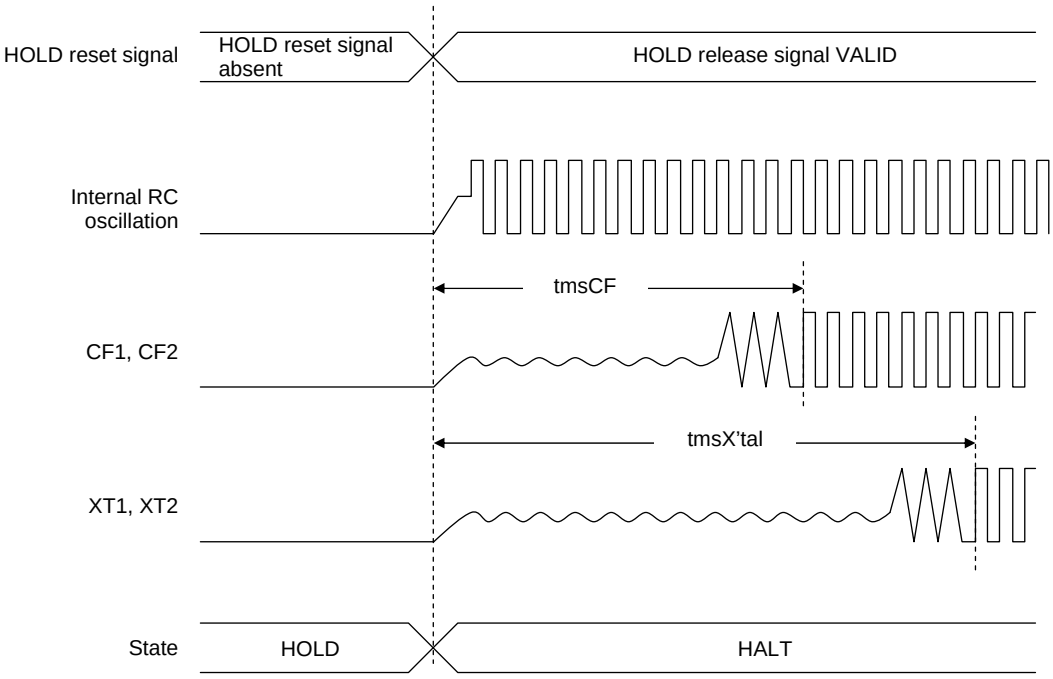


Figure 3 AC Timing Measurement Point

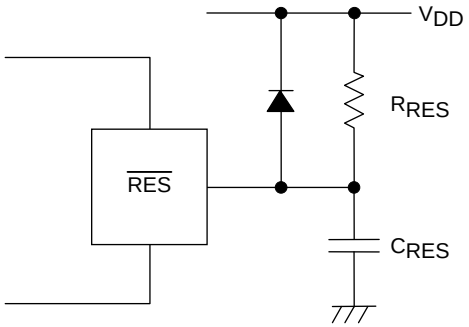


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



(Note)
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

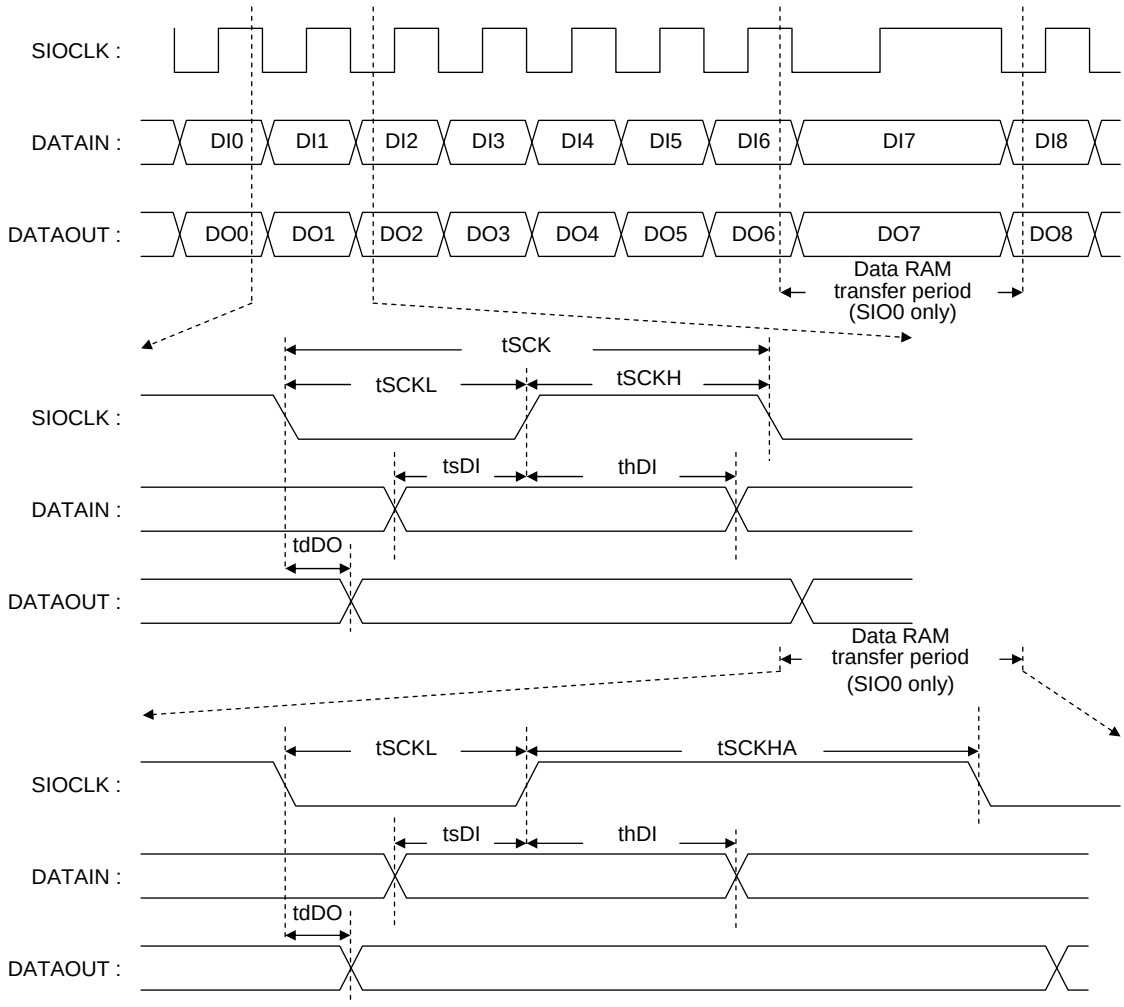


Figure 6 Serial I/O Output Waveforms

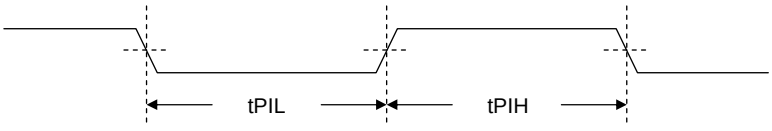


Figure 7 Pulse Input Timing Signal Waveform