Lattice Semiconductor Corporation - ORSO42G5-1BM484C Datasheet

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Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso42g5-1bm484c

ORSO42G5 and ORSO82G5 Embedded Core Detailed Description

The ORSO42G5 and ORSO82G5 have four and eight channels respectively, with a high-speed SERDES macro that performs clock data recovery, serializing and deserializing functions. There is also additional logic for SONET mode and cell mode data synchronization formatting and scrambling/descrambling. For all modes, the data paths can be characterized as the transmit path (FPGA to backplane) and receive path (backplane to FPGA); however the interface signal assignments between the FPGA logic and the core differ depending on the operating mode selected.

The three main operating modes in the ORSO42G5 and ORSO82G5 are:

- SERDES only mode
- SONET mode
- Cell mode
  - Two-link sub-mode
  - Eight-link sub-mode (ORSO82G5 only)

The SONET and cell modes each support sub-modes that can be selected by enabling or disabling certain functions through programmable register bits. Following the basic TX and RX architecture descriptions, the data formatting and logical implementations supporting each of the operational modes are described.

Top Level Description - Transmitter (TX) and Receiver (RX) Architectures

The next sections give a top level description of the transmitter and receive architectures. The high-speed transmit and receive serial data can operate at 0.6-2.7 Gbps depending on the state of the control bits from the system bus and the provided reference clock. For all of the architecture and clock distribution descriptions, however, the standard SONET STS-48 rate of 2,488.32 Mbits/s (i.e., REFCLK_[P:N] = 155.52 MHz for the full rate modes) is assumed.

Transmitter Architecture

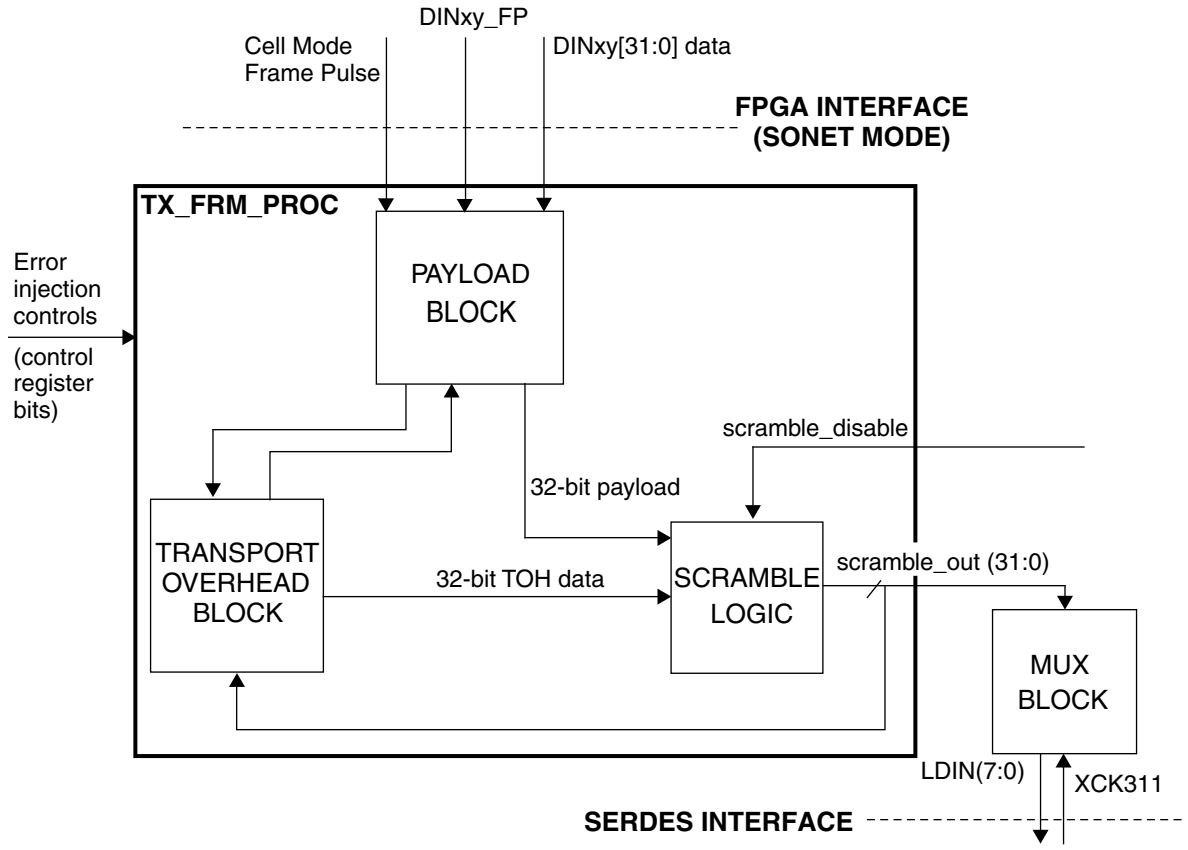
The transmitter section accepts parallel data for transmission from the FPGA logic, formats it for transmission and serializes the data. It also accepts the low-speed reference clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock. The serialized transmitted data are available at the differential CML output pins to drive either an optical transmitters, coaxial media or a circuit board backplane.

The top level transmit architecture is shown in Figure 3. The main logical blocks in the transmit path are:

- Output Port Controllers (OPCs) which contain the cell processing logic.
- SONET processing logic.
- Transmit SERDES and 32:8 MUX.

Depending on the mode of operation, the FPGA to backplane data path may include or bypass the various logical blocks.

Figure 16. TX Frame Processor (TFP) Block Diagram



Payload Sub-block

The Payload sub block is activated by the cell mode frame pulse (cell mode) or DINxx_FP from FPGA (SONET mode). A pulse on this signal indicates the start of a frame.

In SONET mode, only two types of data bytes are in each frame:

- TOH bytes
- SPE data bytes

There are N x 3 (N = 48) bytes of TOH per row and there are a total of 9 rows in a SONET frame. The rest of the bytes in each row are SPE data bytes in SONET mode.

TOH Sub-block

This block is responsible formatting the 144 (48 x 3) bytes of TOH at the beginning of each row of the transport frame. All TOH bytes may be transmitted transparently from the FPGA logic using the transparent mode. Alternately, some or all TOH bytes may be inserted by the TOH block (AUTO_SOH and AUTO_TOH mode). The TOH data is transferred across the FPGA/core interface as 32-bit words, hence 36 clock cycles (12 x 3) are needed to transfer a TOH row. TOH insertion is controlled by software register bits as shown in the Register Map tables.

frame pulse, is less than the minimum threshold set by RX_FIFO_MIN. In the memory map section OOS is referred to as SYNC2_[A2,B2]_OOS, SYNC4_OOS. OVFL is referred to as SYNC2_[A2,B2]_OVFL, SYNC4_OVFL.

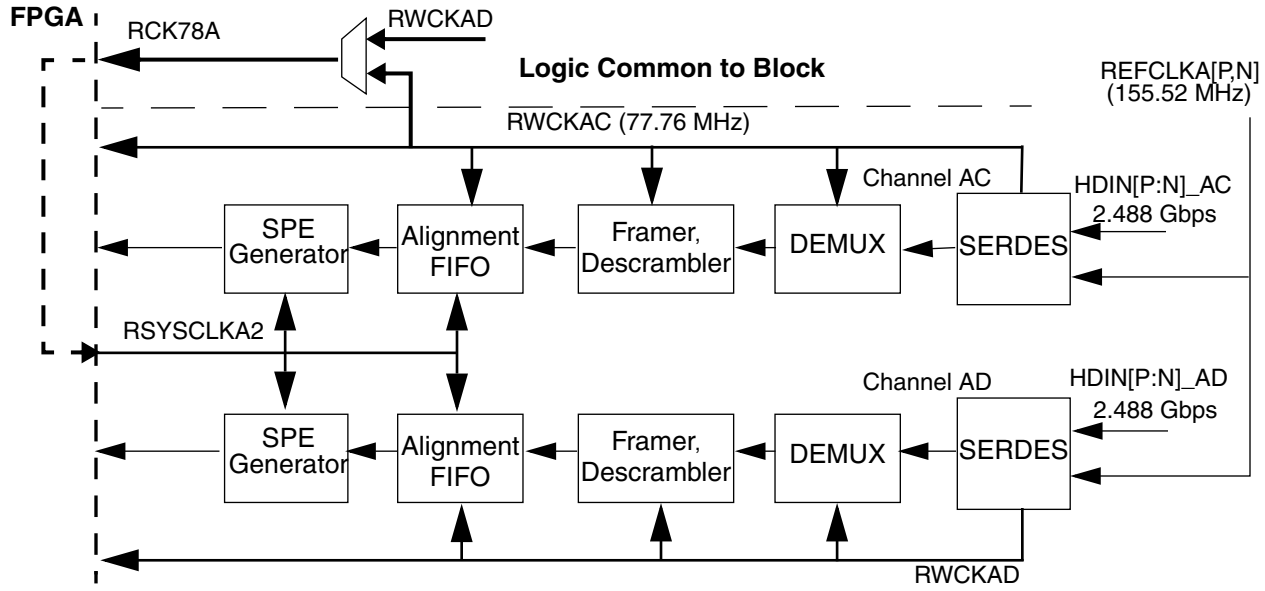
Receive Clocking for Multi-channel Alignment – ORSO42G5

There are a total of seven clocks for the receive path, from FPGA to the core. The two used in SONET mode are RSYSCLKA2 (for block A), and RSYSCLKB2 (for block B). The following diagrams show the recommended clock distribution approaches for SONET mode multi-channel alignment modes. Cell mode alignment is discussed in the section describing the Input Port Controller (IPC).)

SONET Mode Twin Alignment – ORSO42G5

Figure 22 describes the clocking scheme for twin alignment. In twin alignment, the valid channel pairs are AC,AD in block A and BC,BD in block B. The figure provides the clocking scheme for block A as an example. RSYSCLKA2 should be sourced from RCK78A, RWCKAC or RWCKAD. For the ORSO42G5, the use of RCK78A is recommended since it uses primary clock routing resources. This clocking approach provides the required 0 ppm clock frequency matching for each pair and provides flexibility in applications where the two pairs are received from asynchronous sources.

Figure 22. Receive Clocking Diagram for Twin Alignment in Block A – ORSO42G5



SONET Mode Quad Alignment – ORSO42G5

Figure 23 shows the clocking scheme for four-channel alignment. In this application, both clocks RSYSCLKA2 and RSYSCLKB2 should be sourced from a common clock. Either RCK78A or RCK78B can be used as a common clock source. The figure shows RCK78A being used as the clock source.

Figure 24. Twin Channel Alignment – ORSO82G5

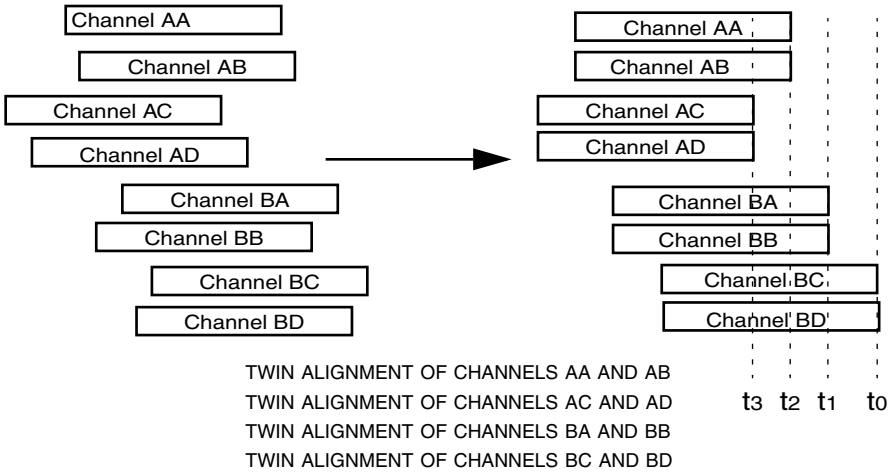


Figure 25. Alignment of SERDES Blocks A and B – ORSO82G5

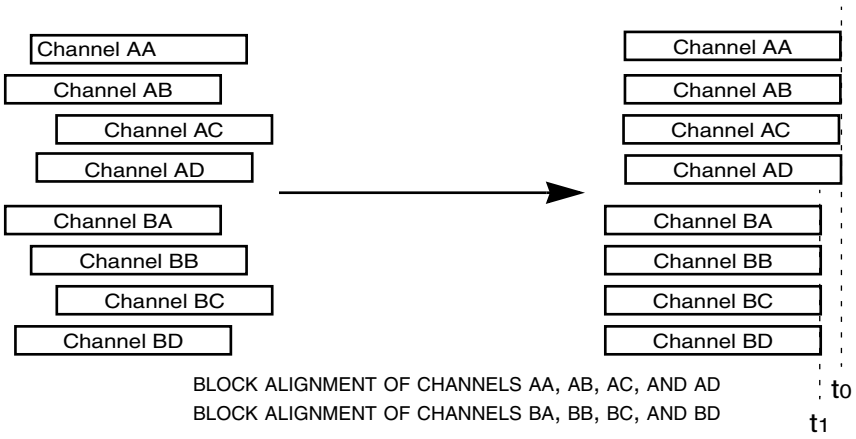
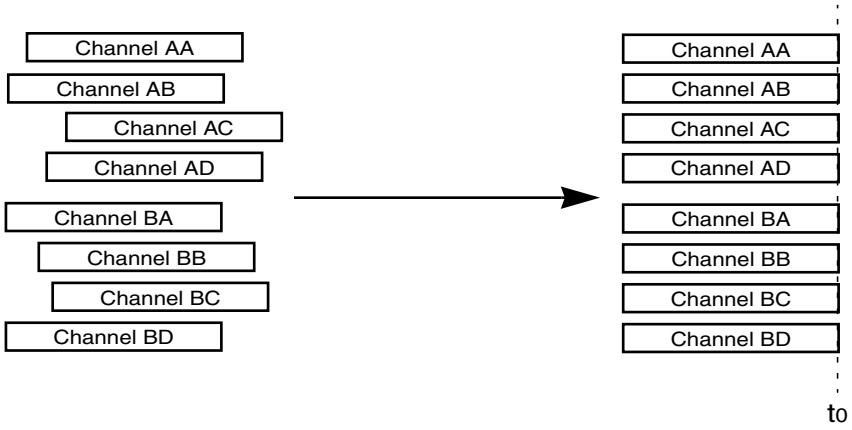


Figure 26. Alignment of all Eight SERDES Channels – ORSO82G5

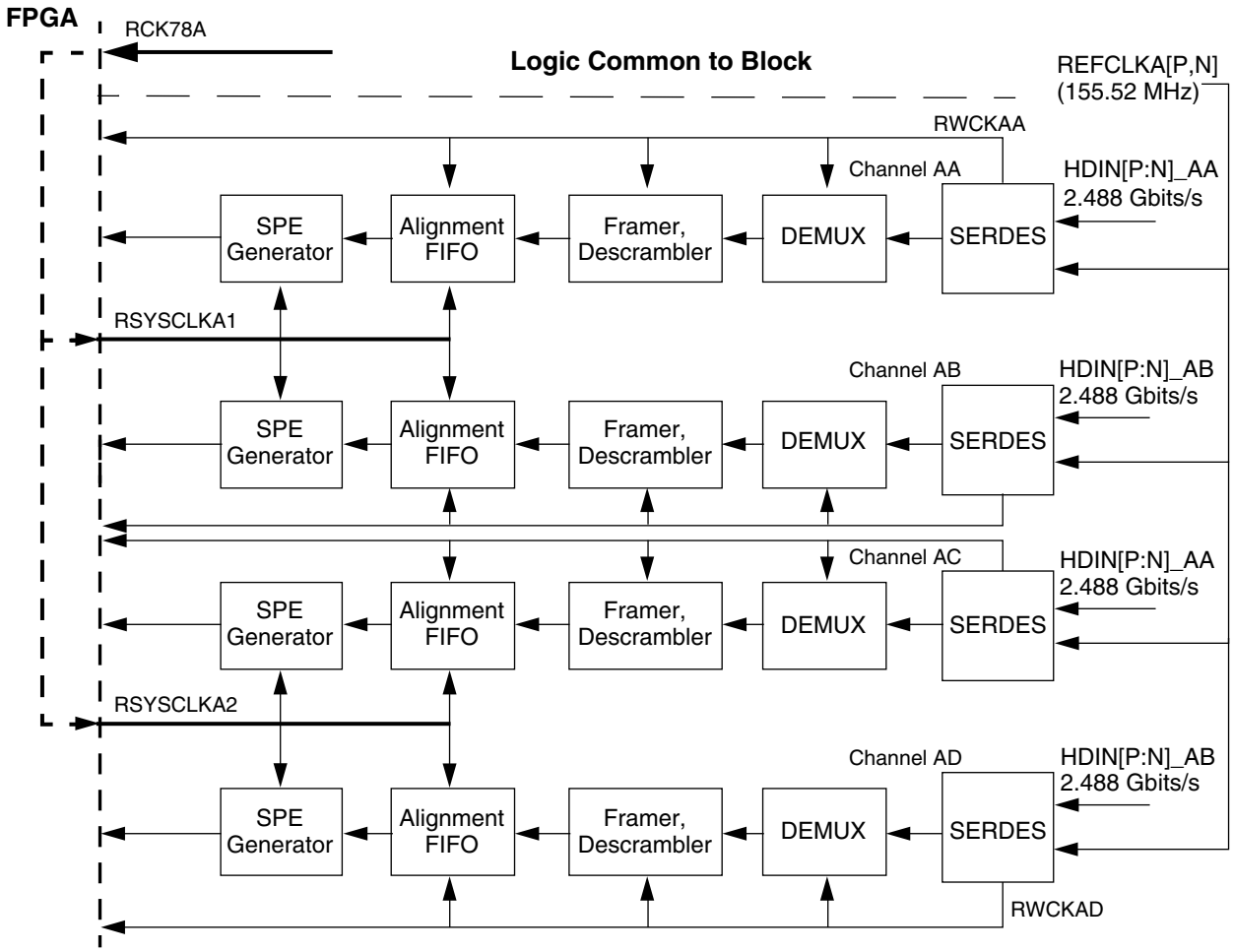


Each channel is provided with a 24 word x 33-bit FIFO. The FIFO can perform two tasks: (1) to change the clock domain from receive clock to a clock from the FPGA side, and (2) to align the receive data over 2, 4, or 8 channels. This FIFO allows a timing budget of 307 ns that can be allocated to skew between the data lanes and for transfer to the common clock. The input to the FIFO consists of 32-bit data and a frame pulse that indicates the start of a

SONET Mode Block Alignment – ORSO82G5

Figure 28 describes the clocks and recommended clocking for block alignment in the SONET mode. For block alignment, the low speed portion for each block should be sourced by a single clock. As the figure shows, for block A, RSYSCLKA1 and RSYSCLKA2 should be sourced by RCK78A. For block B, RSYSCLKB1 and RSYSCLKB2 should be sourced by RCLK78B. RCLK78A can be sourced by any channel in block A and RCLK78B can be sourced by any channel in block B.

Figure 28. Receive Clocking Diagram for Four-Channel Alignment in Block A – ORSO82G5



SONET Mode Octal Alignment – ORSO82G5

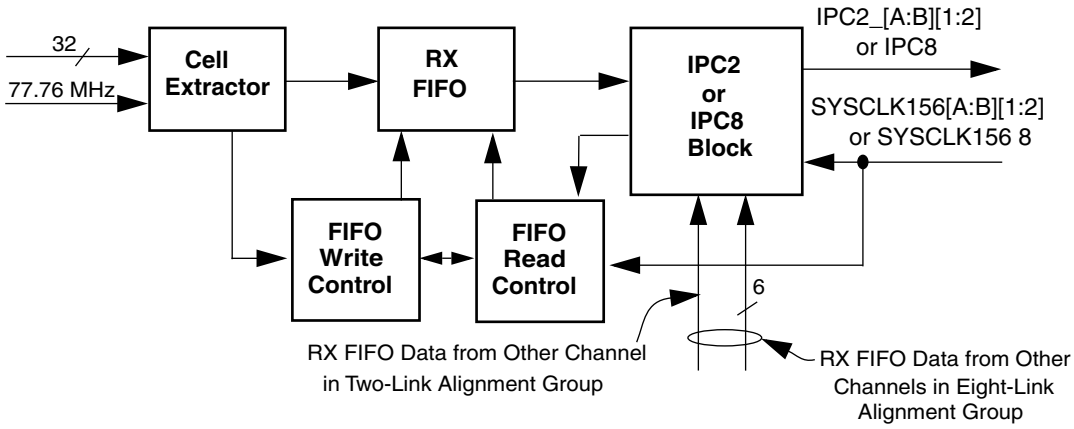
Figure 29 shows the clocking scheme for eight-channel alignment. In this application, all four clocks RSYSCLKA1, RSYSCLKA2, RSYSCLKB1 and RSYSCLKB2 should be sourced from a common clock. Either RCK78A or RCK78B can be used as a common clock source. The figure shows RCK78A being used as the clock source.

Cell Mode Receive Path

The receive logic blocks unique to the cell mode are shown in Figure 43 and are described in the next sections. Prior to reaching this logic the received data has been demultiplexed, frame aligned and descrambled by the SERDES and SONET logic and is formatted on a per channel basis as 32-bit words with an accompanying clock. The clock is a 77.76 MHz clock provided by the DEMUX block performing a divide-by-4 operation on RWCKxx.

The Data Extractor and receive FIFO (RXFIFO) process the data on a per channel basis. The receive FIFO also performs a clock domain transfer to the 156 MHz domain of the Input Port Controller (IPC2/8) blocks. The IPC2/8 blocks perform the two-link or eight-link (ORSO82G5 only) alignment functions. In two-link alignment mode, the received data are passed to the FPGA logic as 40-bit words at the 156 MHz rate. In eight-link alignment mode, the received data are passed to the FPGA logic as a single 160-bit word, again at the 156 MHz rate. Additional mode-dependent status information is also provided across the Core/FPGA interface.

Figure 43. Receive Path Logic Unique to Cell Mode



Cell Extractor

This block is used only in cell mode and does the following:

- Extracts User cells from the SPE
- Performs BIP calculation/checks to verify cell integrity
- Link Header Sequence Interrogation

Processing options include:

- Cell handling for invalid sequence (drop or pass to FPGA)
- S/W configurable ‘link removal’ due to excessive sequence errors

Data from the cell extractor block(s) is sent to the receive FIFO which aligns the data to the system clock domain and provides for deskew between the links.

Cell Extraction and BIP Calculation/Checking

The data from the descrambler are passed into the data extractor which strips the cell data from the payload of a SONET frame. The block extracts the BIP value from the data stream and also perform an internal cell BIP calculation. If the BIP value is not correct, an error flag bit will set in the status registers. The block also determines when the next Link Header is coming in the frame and what the cell sequence number contained within it should be. If the value of the cell sequence counter is not equal to the expected value, an error flag bit will set in the status registers and an error signal will be sent across the core/FPGA interface.

Link Header Detector

The Link Header detector determines when the next Link Header is coming in the frame and what the sequence number contained within it should be. If the value of the cell sequence counter is not equal to the expected value, then an error flag bit will set in the status registers and an error signal will be sent to the FPGA logic. The sequence counter will increment to the next sequence number. The sequence count value is NOT updated with the incorrect value, but is incremented each time a Link Header is received.

If excessive sequence errors are detected (three or more in a row), and the AUTO_REMOVE_[A:B] register bit is set, then the corresponding link will be treated as not valid. The RX_LINK_GOOD status bit will go low indicating the link is no longer receiving cells. If the AUTO_REMOVE_[A:B] register bit is not set, then the link is still valid when excessive sequence errors are detected. An OOF condition will also trigger the link to be removed from service if the AUTO_REMOVE_[A:B] register bit is set.

At startup or after a link has been removed from service (indicated by RX_LINK_GOOD going low), a link can be rejoined into the group. This is performed via the per block REJOIN_[A:B] register bit. When rejoining a link the RX FIFO will begin receiving cells. To cleanly rejoin a link into a group there are two methods to insure the RX FIFO begins loading correctly. The first method is to use the fast framing mode during the rejoin process. The can be done by setting the FFRM_EN_xx for the links that need to be rejoined before setting the REJOIN_[A:B] bit.

The second method is to issue a block reset to clear the FIFO once all links that have been selected to be rejoined are rejoined. This is done by first setting the REJOIN_[A:B] bit. Once the RX_LINK_GOOD status bit is high for the selected channels the GSWRST_[A:B] for the block should be set and cleared to reset the block. This method will disturb traffic on all links in the block during the GSWRST_[A:B] reset time.

Once all of the links in a group are rejoined and the traffic is again flowing the REJOIN_[A:B] bit should be cleared. If this bit is not cleared, a link may drop out using the AUTO_REMOVE mode and the channel may be rejoined incorrectly, causing errors on the entire group.

Receive FIFO

The main clock domain transfer for the data path is handled by the receive FIFO. A 16 x 161 FIFO is used in cell mode. The FIFO is implemented as a dual-port memory which will support simultaneous reads and writes. The receive FIFO block is written to at 77.76 MHz and read at 156 MHz.

The receive FIFO can allow for inter-link skew of about 800 ns (16 x 160 = 2560 bits, 400 ps per bit gives 1024 ns). The 160 LSBs in the memory are received data and the 161st bit indicates the start of a new cell. The FIFO write control logic indicates to the IPC, the start of a new frame of data. This signal will only be active for the A1 word of a frame.

Once frame synchronization has occurred and the IPC has responded with a FIFO enable signal, data will be written into the memory. Only the payload (cells) is written to the FIFO. The TOH bytes are not written into the FIFO. The cell octets immediately following the A1A2 bytes will be always written to the top of the FIFO.

Once a full cell has been written to the memory, the write control logic will send a control signal to the IPC8 or IPC2 block which will start the process of reading data from the FIFO. The IPC will read one whole cell at a time from each of the 8 FIFO blocks, if configured for the eight-link cell mode (ORSO82G5 only) or from each of 2 FIFO blocks if configured for the two-link cell mode.

A FIFO occupancy counter generates a RX_FIFO_OVRUN indication to the register interface if it detects a FIFO overflow condition. The cell mode allows for alignment of all eight-links or alignment of two-links. Thus there will be two IPC blocks for two pairs of channels per block.

Input Port Controllers

The input port controllers (IPCs) are the block responsible for “directing traffic” for the receive traffic flow. The block diagrams for the 2-link and 8-link IPCs are shown in Figure 44. They provide the following essential functions.

- Determining when cell data can be read from the FIFOs of the individual links.

- Note that RXDxx[39:32] signal assignments are the same no matter what mode the RX blocks are in.

Table 13 summarizes the signals across the Core/FPGA interface in the receive direction.

Table 13. RX Core/FPGA Interface Signals – ORSO42G5

RXDAC[39:0]	SONET mode	IPC2 A2 Mode
39	SYNC2_A2_OOS	—
38	—	IPC2_A2_CELLDROP
37	—	IPC2_A2_CELLSTART
36	DOUTAC_FP	—
35	DOUTAC_OOF	
34	DOUTAC_SPE	—
33	—	IPC2_A2_CELL_BIP_ERR
32	DOUTAC_B1_ERR	
[31:20]	DOUTAC[31:20]]	—
[19:0]	DOUTAC[19:0]	IPC2_A2[39:20]
RXDAD[39:0]	SONET Mode	IPC2 A2 Mode
39	—	—
38	—	—
37	—	CELL_BEGIN_OK_A2
36	DOUTAD_FP	—
35	DOUTAD_OOF	
34	DOUTAD_SPE	—
33	—	—
32	DOUTAD_B1_ERR	
[31:20]	DOUTAD[31:20]	—
[19:0]	DOUTAD[19:0]	IPC2_A2[19:0]
RXDBC[39:0]	SONET Mode	IPC2 B2 Mode
39	SYNC2_B2_OOS	—
38	—	IPC2_B2_CELLDROP
37	—	IPC2_B2_CELLSTART
36	DOUTBC_FP	—
35	DOUTBC_OOF	
34	DOUTBC_SPE	—
33	—	IPC2_B2_CELL_BIP_ERR
32	DOUTBC_B1_ERR	
[31:20]	DOUTBC[31:20]	—
[19:0]	DOUTBC[19:0]	IPC2_B2[39:20]
RXDBD[39:0]	SONET Mode	IPC2 B2 Mode
39	—	
38	SYNC4_B_OOS	—
37	—	CELL_BEGIN_OK_B2
36	DOUTBD_FP	—
35	DOUTBD_OOF	
34	DOUTBD_SPE	—

Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30826 - AC 30836 - AD 30926 - BC 30936 - BD	[0:5]	RSVD	00	Reserved	—
	[6]	AUTO_B1_xx		AUTO_B1_xx = 0, B1 is not inserted by the embedded core AUTO_B1_xx = 1, B1 is calculated and inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	Both
	[7]	AUTO_A1A2_xx		AUTO_A1A2_xx = 0, A1/A2 bytes are not inserted by the embedded core AUTO_A1A2_xx = 1, A1/A2 bytes inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	

Table 33. SERDES Per-Block Control Register Descriptions – ORSO82G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
SERDES Per-Block Control Register (Read/Write) xx = [AA,...,BD]					
30005 - A 30105 - B	[0]	RSVD	44	Reserved	—
	[1]	GMASK_[A:B]		Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of all channel in the SERDES block are prevented from generating an alarm (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset.	Both
	[2]	GSWRST_[A:B]		Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of all four channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset.	Both
	[3]	GPWRDNT_[A:B]		Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for all four channels are powered down. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset.	Both
	[4]	GPWRDNR_[A:B]		Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for all four channels are powered down. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset.	Both
	[5:6]	RSVD		Reserved	—
	[7]	GTESTEN_[A:B]		Global Test Enable Bit. When GTESTEN_[A:B] = 1, the transmit and receive sections of all channels in the block are place in test mode. The TESTMODE_xx bits (30006, 30106, etc.) must be set to specify the desired test on a per-channel basis. The GTESTEN_[A:B] bits override the individual TESTEN_xx settings.	Factory

Table 34. Per-Channel Control Register Descriptions – ORSO82G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30800 - AA 30810 - AB 30820 - AC 30830 - AD 30900 - BA 30910 - BB 30920 - BC 30930 - BD	[0:4]	RSVD	00	Reserved	—
	[5]	CELL_ALIGN_ERR_EN_xx		'1' = Alarm enabled for CELL_ALIGN_ERR_xx	Cell
	[6]	TX_URUN_ERR_EN_xx		'1' = Alarm enabled for TX_URUN_ERR_xx	Cell
	[7]	TX_ORUN_ERR_EN_xx		'1' = Alarm enabled for TX_ORUN_ERR_xx	Cell
30801 - AA 30811 - AB 30821 - AC 30831 - AD 30901 - BA 30911 - BB 30921 - BC 30931 - BD	[0]	RSVD	00	Reserved	—
	[1]	OOF_EN_xx		'1' = Alarm enabled for OOF_xx	Both
	[2]	EX_SEQ_ERR_EN_xx		'1' = Alarm enabled for EX_SEQ_ERR _xx	Cell
	[3]	SEQ_ERR_EN_xx		'1' = Alarm enabled for SEQ_ERR _xx	Cell
	[4]	CELL_BIP_ERR_EN_xx		'1' = Alarm enabled for CELL_BIP_ERR_xx	Cell
	[5]	B1_ERR_EN_xx		'1' = Alarm enabled for B1_ERR_xx	Both
	[6]	RX_FIFO_OVRUN_EN_xx		'1' = Alarm enabled for RX_FIFO_OVRUN_xx	Cell
	[7]	RDI_EN_xx		'1' = Alarm enabled for RDI_xx	Both
30802 - AA 30812 - AB 30822 - AC 30832 - AD 30902 - BA 30912 - BB 30922 - BC 30932 - BD	[0]	ENABLE_JUST_xx	00	ENABLE_JUST_xx =1 causes the core to interpret pointer bytes for positive or negative justification	SONET
	[1]	FMPU_STR_EN_xx		FMPU_STR_EN_xx = 1 enables a channel for alignment within a multi-channel alignment group	SONET
	[2:3]	FMPU_SYNMODE_xx		"00" - No channel alignment "01" - Twin channel alignment "10" - 4 channel alignment "11 - By-8 alignment	SONET
	[4]	DSCR_INH_xx		Descrambling Inhibit, DSCR_INH = 1 inhibits descrambling (in the Rx direction) and scrambling (in the Tx direction). When inhibiting the scrambler and descrambler the AUTO_B1_xx calculated and checked B1 value will always be incorrect.	Both
	[5]	FFRM_EN_xx		Fast Frame Enable, FFRM_EN=1 enables the fast frame mode.	Both
	[6]	AIS_ON_xx		Alarm Indication Signal (control), AIS_ON =1 forces AIS-L insertion.	Both
	[7]	AIS_ON_OOF_xx		Alarm Indication Signal on Out of Frame, AIS_ON_OOF =1 forces AIS-L insertion during OOF =1.	Both

Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A08	[0]	ALARM_STATUS_BD	00	Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BD. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[1]	ALARM_STATUS_BC		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BC. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[2]	ALARM_STATUS_BB		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BB. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[3]	ALARM_STATUS_BA		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BA. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[4]	ALARM_STATUS_AD		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AD. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[5]	ALARM_STATUS_AC		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AC. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[6]	ALARM_STATUS_AB		OR of all alarm status bits for channel AB. A 1 on this bit will set the alarm pin on the system bus interrupt cause register (on the FPGA side)	Both
	[7]	ALARM_STATUS_AA		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AA. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
30A09	[0:7]	B1_ERR_CNT	00	Error counter that increments when a section B1 error is detected on a link. The link is selected using ERRCNT_CHSEL. This counter is cleared on read.	Both
30A0A	[0:7]	CELL_BIP_ERR_CNT	00	Cell BIP Error Counter, Error counter that increments when a Cell BIP error is detected on a link. The link being monitored is selected using ERRCNT_CHSEL. This counter is cleared on read.	Cell

External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 46 specifies reference clock requirements, over the full range of operating conditions. The designer is encourage to read TN1040, *SERDES Reference Clock,* which discusses various aspects of this system element and its interconnection.

Table 46. Reference Clock Specifications (REFCLKP_[A:B] and REFCLKN_[A:B])

Parameter	Min.	Typ.	Max.	Units
Frequency Range	60	—	185	MHz
Frequency Tolerance[1]	-350	—	350	ppm
Duty Cycle (Measured at 50% Amplitude Point)	40	50	60	%
Rise Time	—	500	1000	ps
Fall Time	—	500	1000	ps
P–N Input Skew	—	—	75	ps
Differential Amplitude	500	800	2 x V_{DDIB}	mV_{p-p}
Common Mode Level	$V_{single-ended/2}$	0.75	$V_{DD15} – (V_{single-ended/2})$	V
Single-Ended Amplitude	250	400	V_{DDIB}	mV_{p-p}
Input Capacitance (at REFCLKP_[A:B])	—	—	5	pF
Input Capacitance (at REFCLKN_[A:B])	—	—	5	pF

1. This specification indicates the capability of the high speed receiver CDR PLL to acquire lock when the reference clock frequency and incoming data rate are not synchronized.

Table 47. Pin Descriptions (Continued)

Symbol	I/O	Description
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user programmable I/O, if not used for clock inputs.
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O if boundary scan is not used.[1]
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration this pin is a user-programmable I/O pin.[1]
HDC	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{LDC}}$	O	$\overline{\text{Low During Configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.[1]
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
$\overline{\text{WR}}$/MPI_RW	I	$\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{\text{WR}}$/MPI_RW is a user-programmable I/O pin.[1]
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the PowerPC bus master utilizing the least-significant bits of the PowerPC 32-bit address.
$\overline{\text{MPI\_BURST}}$	I	$\overline{\text{MPI\_BURST}}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.
$\overline{\text{MPI\_BDIP}}$	I	$\overline{\text{MPI\_BDIP}}$ is driven by the PowerPC processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	O	During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]

Table 47. Pin Descriptions (Continued)

Symbol	I/O	Description
MPI_ACK	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_CLK	I	This is the PowerPC synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the Embedded System Bus. If MPI is used this will be the AMBA bus clock.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_TEA	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_RTRY	O	This pin requests the MPC860 to relinquish the bus and retry the cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
D[0:31]	I/O	Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	O	D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.[1]
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.[1]
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.[1]
TESTCFG (ORSO82G5 only)	I	During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user programmable I/O pin.[1]

1. The FPGA States of Operation section in the ORCA Series 4 FPGAs data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

This section describes device I/O signals to/from the embedded core.

Table 48. FPSC Function Pin Descriptions

Symbol	I/O	Description
Common Signals for Both SERDES Block A and B		
PASB_RESETN	I	Active low reset for the embedded core.[1]
PASB_TRISTN	I	Active low 3-state for embedded core output buffers.[1]
PASB_PDN	I	Active low power down of all SERDES blocks and associated I/Os.[1]
PASB_TESTCLK	I	Clock input for BIST and loopback test (factory only).[1]
PBIST_TEST_ENN	I	Selection of PASB_TESTCLK input for BIST test (factory only).[1]
PLOOP_TEST_ENN	I	Digital only loopback from TX to RX (factory only).[1]
PMP_TESTCLK	I	Clock input for microprocessor in test mode (factory only).[1]
PMP_TESTCLK_ENN	I	Selection of PMP_TESTCLK in test mode (factory only).[1]
PSYS_DOBISTN	I	Input to start BIST test (factory only).[1]
PSYS_RSSIG_ALL	O	Output result of BIST test (factory only).
SERDES Block A and B Pins		
REFCLKN_A	I	CML reference clock input—SERDES block A.
REFCLKP_A	I	CML reference clock input—SERDES block A.
REFCLKN_B	I	CML reference clock input—SERDES block B.
REFCLKP_B	I	CML reference clock input—SERDES block B.
REXT_A	—	Reference resistor—SERDES block A.
REXT_B	—	Reference resistor—SERDES block B.
REXTN_A	—	Reference resistor – SERDES block. A 3.32 K W ± 1% resistor must be connected across REXT_B and REXTN_B. This resistor should handle a current of 300 µA.
REXTN_B	—	Reference resistor—SERDES block B. A 3.32 K Ω ± 1% resistor must be connected across REXT_B and REXTN_B. This register should handle a current of 300 µA
HDINN_AA	I	High-speed CML receive data input—SERDES block A, channel A (not available in ORSO42G5).
HDINP_AA	I	High-speed CML receive data input—SERDES block A, channel A (not available in ORSO42G5).
HDINN_AB	I	High-speed CML receive data input—SERDES block A, channel B (not available in ORSO42G5).
HDINP_AB	I	High-speed CML receive data input—SERDES block A, channel B (not available in ORSO42G5).
HDINN_AC	I	High-speed CML receive data input—SERDES block A, channel C.
HDINP_AC	I	High-speed CML receive data input—SERDES block A, channel C.
HDINN_AD	I	High-speed CML receive data input—SERDES block A, channel D.
HDINP_AD	I	High-speed CML receive data input—SERDES block A, channel D.
HDINN_BA	I	High-speed CML receive data input—SERDES block B, channel A.
HDINP_BA	I	High-speed CML receive data input—SERDES block B, channel A (not available in ORSO42G5).
HDINN_BB	I	High-speed CML receive data input—SERDES block B, channel B (not available in ORSO42G5).
HDINP_BB	I	High-speed CML receive data input—SERDES block B, channel B (not available in ORSO42G5).
HDINN_BC	I	High-speed CML receive data input—SERDES block B, channel C (not available in ORSO42G5).
HDINP_BC	I	High-speed CML receive data input—SERDES block B, channel C.
HDINN_BD	I	High-speed CML receive data input—SERDES block B, channel D.
HDINP_BD	I	High-speed CML receive data input—SERDES block B, channel D.
SERDES Block A and B Pins		
HDOUTN_AA	O	High-speed CML transmit data output—SERDES Block A, channel A (not available in ORSO42G5).
HDOUTP_AA	O	High-speed CML transmit data output—SERDES Block A, channel A (not available in ORSO42G5).

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
K13	-	-	VSS	VSS	-	-
B21	1 (TC)	9	IO	PT31D	-	L55C
A21	1 (TC)	9	IO	PT31C	VREF_1_09	L55T
E13	1 (TC)	-	VDDIO1	VDDIO1	-	-
D14	1 (TC)	9	IO	PT30D	-	L56C
C14	1 (TC)	9	IO	PT30C	-	L56T
K14	-	-	VSS	VSS	-	-
B20	1 (TC)	9	IO	PT29D	-	L57C
A20	1 (TC)	9	IO	PT29C	-	L57T
N7	-	-	VDD15	VDD15	-	-
B19	1 (TC)	1	IO	PT28D	-	L58C
A19	1 (TC)	1	IO	PT28C	-	L58T
L8	-	-	VSS	VSS	-	-
D13	1 (TC)	1	IO	PT27D	VREF_1_01	L59C
C13	1 (TC)	1	IO	PT27C	-	L59T
E18	1 (TC)	-	VDDIO1	VDDIO1	-	-
A18	1 (TC)	1	IO	PT27B	-	L60C
B18	1 (TC)	1	IO	PT27A	-	L60T
A17	1 (TC)	2	IO	PT26D	-	L61C
B17	1 (TC)	2	IO	PT26C	VREF_1_02	L61T
L9	-	-	VSS	VSS	-	-
D12	1 (TC)	2	IO	PT25D	-	L62C
C12	1 (TC)	2	IO	PT25C	-	L62T
E19	1 (TC)	-	VDDIO1	VDDIO1	-	-
A16	1 (TC)	3	IO	PT24D	-	L63C
B16	1 (TC)	3	IO	PT24C	VREF_1_03	L63T
A15	1 (TC)	3	IO	PT23D	-	L64C
B15	1 (TC)	3	IO	PT23C	-	L64T
F16	1 (TC)	-	VDDIO1	VDDIO1	-	-
E11	1 (TC)	3	IO	PT22D	-	-
L10	-	-	VSS	VSS	-	-
D11	1 (TC)	4	IO	PT21D	-	L65C
C11	1 (TC)	4	IO	PT21C	-	L65T
A14	1 (TC)	4	IO	PT20D	-	L66C
B14	1 (TC)	4	IO	PT20C	-	L66T
A13	1 (TC)	4	IO	PT19D	-	L67C
B13	1 (TC)	4	IO	PT19C	VREF_1_04	L67T
G14	1 (TC)	-	VDDIO1	VDDIO1	-	-
L11	-	-	VSS	VSS	-	-
N15	-	-	VDD15	VDD15	-	-
D10	1 (TC)	5	IO	PT18D	PTCK1C	L68C
C10	1 (TC)	5	IO	PT18C	PTCK1T	L68T
A12	1 (TC)	5	IO	PT17D	PTCK0C	L69C
B12	1 (TC)	5	IO	PT17C	PTCK0T	L69T

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
W18	—	—	VSS	VSS	—	—
V2	7 (CL)	5	IO	PL21D	A10/PPC_A24	L17C_A0
V3	7 (CL)	5	IO	PL21C	A9/PPC_A23	L17T_A0
W19	—	—	VSS	VSS	—	—
V4	7 (CL)	5	IO	PL21B	—	L18C_A0
V5	7 (CL)	5	IO	PL21A	—	L18T_A0
W4	7 (CL)	5	IO	PL22D	A8/PPC_A22	L19C_A0
W3	7 (CL)	5	IO	PL22C	VREF_7_05	L19T_A0
W1	7 (CL)	5	IO	PL22B	—	L20C_A0
Y1	7 (CL)	5	IO	PL22A	—	L20T_A0
Y2	7 (CL)	5	IO	PL23D	—	L21C_D0
AA1	7 (CL)	5	IO	PL23C	—	L21T_D0
Y13	—	—	VSS	VSS	—	—
Y4	7 (CL)	5	IO	PL23B	—	L22C_A0
Y3	7 (CL)	5	IO	PL23A	—	L22T_A0
Y5	7 (CL)	6	IO	PL24D	PLCK1C	L23C_A0
W5	7 (CL)	6	IO	PL24C	PLCK1T	L23T_A0
U3	7 (CL)	—	VDDIO7	VDDIO7	—	—
AB1	7 (CL)	6	IO	PL24B	—	L24C_D0
AA2	7 (CL)	6	IO	PL24A	—	L24T_D0
AB2	7 (CL)	6	IO	PL25D	VREF_7_06	L25C_D0
AC1	7 (CL)	6	IO	PL25C	A7/PPC_A21	L25T_D0
Y14	—	—	VSS	VSS	—	—
AA4	7 (CL)	6	IO	PL25B	—	—
AB4	7 (CL)	6	IO	PL26D	A6/PPC_A20	L26C_A0
AB3	7 (CL)	6	IO	PL26C	A5/PPC_A19	L26T_A0
W2	7 (CL)	—	VDDIO7	VDDIO7	—	—
AD1	7 (CL)	7	IO	PL26B	—	—
AE1	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	L27C_D0
AD2	7 (CL)	7	IO	PL27C	VREF_7_07	L27T_D0
AC3	7 (CL)	7	IO	PL27B	—	L28C_A0
AC4	7 (CL)	7	IO	PL27A	—	L28T_A0
AF1	7 (CL)	8	IO	PL28D	A4/PPC_A18	L29C_D0
AE2	7 (CL)	8	IO	PL28C	VREF_7_08	L29T_D0
AB5	7 (CL)	8	IO	PL29D	A3/PPC_A17	L30C_A0
AA5	7 (CL)	8	IO	PL29C	A2/PPC_A16	L30T_A0
Y15	—	—	VSS	VSS	—	—
AD3	7 (CL)	8	IO	PL29B	—	—
AG1	7 (CL)	8	IO	PL30D	A1/PPC_A15	L31C_D0
AF2	7 (CL)	8	IO	PL30C	A0/PPC_A14	L31T_D0
AD4	7 (CL)	8	IO	PL30B	—	L32C_D0
AE3	7 (CL)	8	IO	PL30A	—	L32T_D0
AD5	7 (CL)	8	IO	PL31D	DP0	L33C_A0
AC5	7 (CL)	8	IO	PL31C	DP1	L33T_A0

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM12	6 (BL)	9	IO	PB12B	—	L28C_A0
AP12	6 (BL)	9	IO	PB12C	VREF_6_09	L29T_A0
AP13	6 (BL)	9	IO	PB12D	D25	L29C_A0
AM13	6 (BL)	9	IO	PB13A	—	L30T_D0
AN14	6 (BL)	9	IO	PB13B	—	L30C_D0
V17	—	—	VSS	VSS	—	—
AP14	6 (BL)	10	IO	PB13C	D26	L31T_A0
AP15	6 (BL)	10	IO	PB13D	D27	L31C_A0
AK13	6 (BL)	10	IO	PB14A	—	L32T_A0
AK14	6 (BL)	10	IO	PB14B	—	L32C_A0
AM14	6 (BL)	10	IO	PB14C	VREF_6_10	L33T_A0
AL14	6 (BL)	10	IO	PB14D	D28	L33C_A0
AP17	6 (BL)	11	IO	PB15A	—	L34T_A0
AP16	6 (BL)	11	IO	PB15B	—	L34C_A0
AM15	6 (BL)	11	IO	PB15C	D29	L35T_D0
AN16	6 (BL)	11	IO	PB15D	D30	L35C_D0
AM17	6 (BL)	11	IO	PB16A	—	L36T_A0
AM16	6 (BL)	11	IO	PB16B	—	L36C_A0
AP18	6 (BL)	11	IO	PB16C	VREF_6_11	L37T_A0
AP19	6 (BL)	11	IO	PB16D	D31	L37C_A0
AL16	5 (BC)	1	IO	PB17A	—	L1T_D0
AK15	5 (BC)	1	IO	PB17B	—	L1C_D0
N22	—	—	VSS	VSS	—	—
AN18	5 (BC)	1	IO	PB17C	—	L2T_A0
AN19	5 (BC)	1	IO	PB17D	—	L2C_A0
AP20	5 (BC)	1	IO	PB18A	—	L3T_A0
AP21	5 (BC)	1	IO	PB18B	—	L3C_A0
AL17	5 (BC)	1	IO	PB18C	VREF_5_01	L4T_D0
AK16	5 (BC)	1	IO	PB18D	—	L4C_D0
P13	—	—	VSS	VSS	—	—
AM19	5 (BC)	2	IO	PB19A	—	L5T_A0
AM18	5 (BC)	2	IO	PB19B	—	L5C_A0
P14	—	—	VSS	VSS	—	—
AN20	5 (BC)	2	IO	PB19C	PBCK0T	L6T_A0
AM20	5 (BC)	2	IO	PB19D	PBCK0C	L6C_A0
AK17	5 (BC)	2	IO	PB20A	—	L7T_D0
AL18	5 (BC)	2	IO	PB20B	—	L7C_D0
AL11	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP22	5 (BC)	2	IO	PB20C	VREF_5_02	L8T_D0
AN21	5 (BC)	2	IO	PB20D	—	L8C_D0
AM22	5 (BC)	2	IO	PB21A	—	L9T_A0
AM21	5 (BC)	2	IO	PB21B	—	L9C_A0
AP23	5 (BC)	3	IO	PB21C	—	L10T_D0
AN22	5 (BC)	3	IO	PB21D	VREF_5_03	L10C_D0

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM28	5 (BC)	7	IO	PB31D	—	L26C_A0
AN30	5 (BC)	7	IO	PB32B	—	—
R14	—	—	VSS	VSS	—	—
AK25	5 (BC)	7	IO	PB32C	—	L27T_D0
AL26	5 (BC)	7	IO	PB32D	—	L27C_D0
AN17	5 (BC)	—	VDDIO5	VDDIO5	—	—
AL27	5 (BC)	8	IO	PB33C	—	L28T_A0
AL28	5 (BC)	8	IO	PB33D	VREF_5_08	L28C_A0
AN31	5 (BC)	8	IO	PB34B	—	—
R15	—	—	VSS	VSS	—	—
AK26	5 (BC)	8	IO	PB34D	—	—
AM30	5 (BC)	9	IO	PB35B	—	—
AL29	5 (BC)	9	IO	PB35D	VREF_5_09	—
AK27	5 (BC)	9	IO	PB36B	—	—
R20	—	—	VSS	VSS	—	—
AL30	5 (BC)	9	IO	PB36C	—	L29T_D0
AK29	5 (BC)	9	IO	PB36D	—	L29C_D0
AK28	—	—	VDD33	VDD33	—	—
AA16	—	—	VDD15	VDD15	—	—
AP32	—	—	IO	PSCHAR_LDIO9	—	—
AP33	—	—	IO	PSCHAR_LDIO8	—	—
AN32	—	—	IO	PSCHAR_LDIO7	—	—
AM31	—	—	IO	PSCHAR_LDIO6	—	—
AA17	—	—	VDD15	VDD15	—	—
AM32	—	—	VDD33	VDD33	—	—
AL31	—	—	IO	PSCHAR_LDIO5	—	—
AM33	—	—	IO	PSCHAR_LDIO4	—	—
AA18	—	—	VDD15	VDD15	—	—
AK30	—	—	IO	PSCHAR_LDIO3	—	—
AL32	—	—	IO	PSCHAR_LDIO2	—	—
AA19	—	—	VDD15	VDD15	—	—
AB16	—	—	VDD15	VDD15	—	—
AK31	—	—	VDD33	VDD33	—	—
AJ30	—	—	IO	PSCHAR_LDIO1	—	—
AK33	—	—	IO	PSCHAR_LDIO0	—	—
AK34	—	—	IO	PSCHAR_CKIO1	—	—
AJ31	—	—	IO	PSCHAR_CKIO0	—	—
AJ33	—	—	IO	PSCHAR_XCK	—	—
AJ34	—	—	IO	PSCHAR_WDSYNC	—	—
AH30	—	—	IO	PSCHAR_CV	—	—
AH31	—	—	IO	PSCHAR_BYTSYNC	—	—
AH32	—	—	O	ATMOUT_B (no connect)	—	—
AH33	—	—	VSS	VSS	—	—
AH34	—	—	VDDGB_B	VDDGB_B	—	—