# Lattice Semiconductor Corporation - ORSO42G5-1BM484I Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 10368 |
| Total RAM Bits | 113664 |
| Number of I/O | 204 |
| Number of Gates | 643000 |
| Voltage - Supply | 1.425V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/orso42g5-1bm484i |

12.5% of the clock period increments. An automatic input buffer delay compensation mode is available for phase delay. Each PPLL provides two outputs that can have programmable (12.5% steps) phase differences.

### Embedded Block RAM

New 512 x 18 block-port RAM blocks are embedded in the FPGA core to significantly increase the amount of memory and complement the distributed PFU memories. The EBRs include two write ports, two read ports, and two byte lane enables which provide four-port operation. Optional arbitration between the two write ports is available, as well as direct connection to the high-speed system bus.

Additional logic has been incorporated to allow significant flexibility for FIFO, constant multiply, and two-variable multiply functions. The user can configure FIFO blocks with flexible depths of 512K, 256K, and 1K including asynchronous and synchronous modes and programmable status and error flags. Multiplier capabilities allow a multiply of an 8-bit number with a 16-bit fixed coefficient or vice versa (24-bit output), or a multiply of two 8-bit numbers (16-bit output). On-the-fly coefficient modifications are available through the second read/write port.

Two 16 x 8-bit CAMs per embedded block can be implemented in single match, multiple match, and clear modes. The EBRs can also be preloaded at device configuration time.

### Configuration

The FPGAs functionality is determined by internal configuration RAM. The FPGAs internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The configuration data can reside externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low pin-count method for configuring FPGAs.

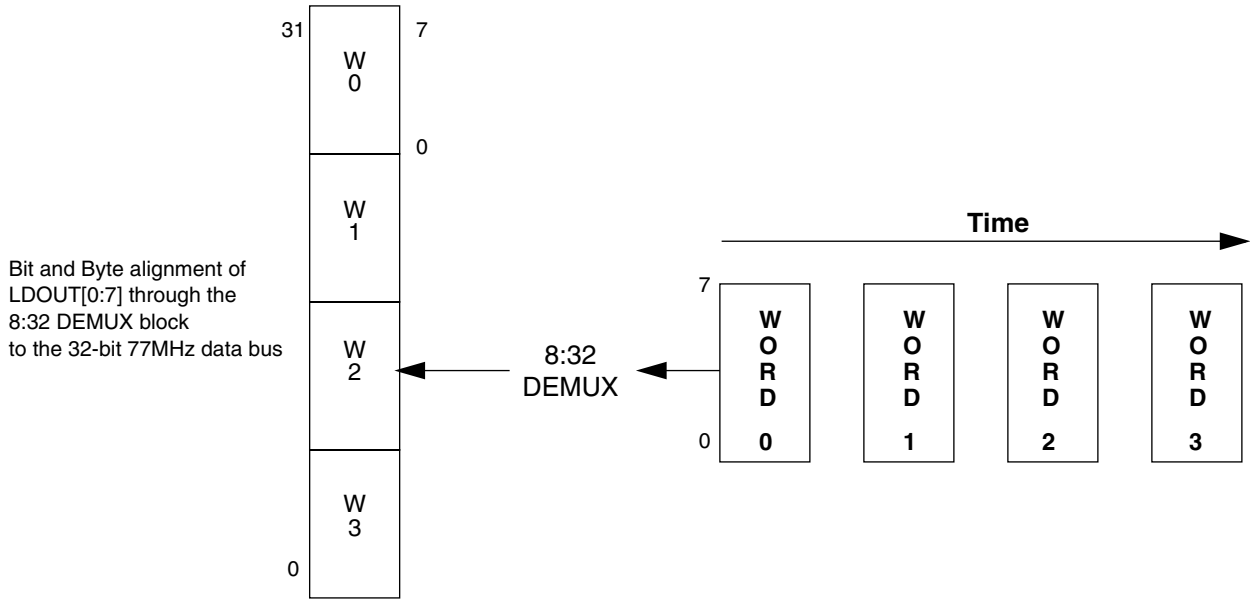
The RAM is loaded by using one of several configuration modes. Supporting the traditional master/slave serial, master/slave parallel, and asynchronous peripheral modes, Series 4 also utilizes its MicroProcessor Interface and Embedded System Bus to perform both programming and readback. Daisy chaining of multiple devices and partial reconfiguration are also permitted.

Other configuration options include the initialization of the embedded-block RAM memories and FPSC memory as well as system bus options and bit stream error checking. Programming and readback through the JTAG *(IEEE* 1149.2*)* port is also available meeting In-System Programming (ISP) standards (*IEEE* 1532 Draft).

## ORSO42G5 and ORSO82G5 Overview

The ORSO42G5 and ORSO82G5 FPSCs provide high-speed backplane transceivers combined with FPGA logic. The ORSO42G5 and ORSO82G5 devices are based on the 1.5V OR4E04 ORCA FPGA and have a 36 x 36 array of Programmable Logic Cells (PLCs). The embedded core, which contains the backplane transceivers, is attached to the right side of the device and is integrated directly into the FPGA array. A top level diagram of the basic chip configuration is shown in Figure 1.

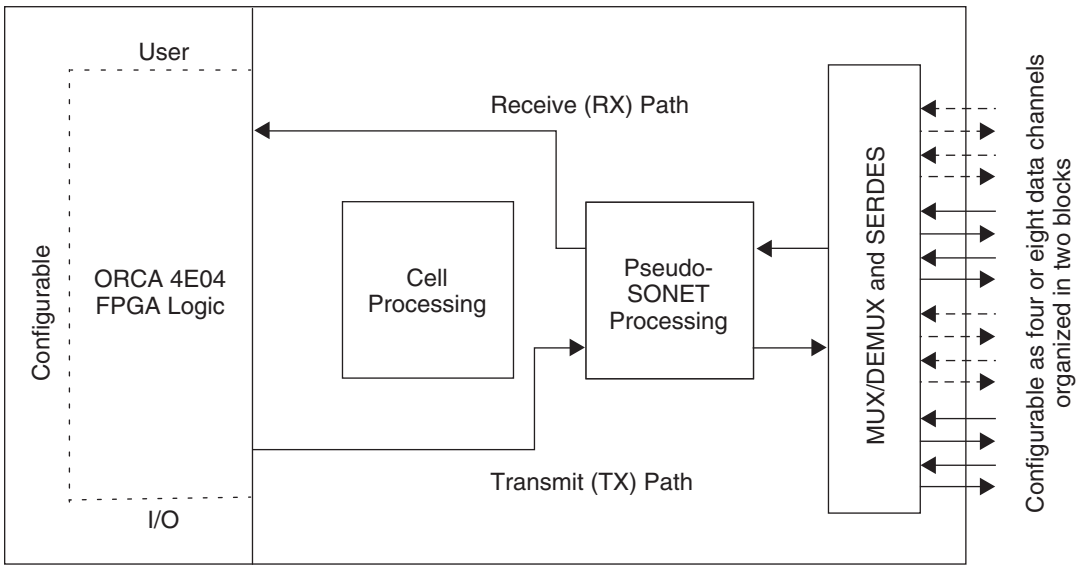
***Figure 10. Bit and Byte Alignment for DEMUX Block***




## SONET Mode Operation – Detailed Description

The following sections describe the data processing performed in the SONET logic blocks. The basic data flows in the SONET Mode are shown in Figure 11. At a top level, the descriptions are separated into processing in the transmit path (FPGA to serial link) and processing in the receive path (serial link to FPGA). In general, the descriptions in the next sections are written to describe SONET mode operation, although some of the "SONET logic blocks" are also used in cell mode operation. The various processing options are selected by setting bits in control registers and status information is written to status registers. Both types of registers can be written and/or read from the System Bus. Memory maps and descriptions for the registers are given in Table 21 through Table 36.

***Figure 11. Basic Data Flows - SONET Mode***




In the SONET mode, the transmit block receives 32-bit wide data from the FPGA (DINxx) on each of its channels along with a frame pulse (DINxx_FP) per channel and a transmit clock (TSYCLKxx). Typically this will represent a STS-48 stream on each link. The data are first passed through a TOH block which will generate all the timing pulses that are required to isolate individual overhead bytes (e.g., A1, A2, B1, D1-D3, etc.). The timing pulse gener-

***Table 5. Inserted TOH Values (All 0x) in AUTO_SOH Mode***

| | | |
|---|---|---|
| A1 = F6 | A2 = 28 | J0 |
| B1 = calculated,<br>1st. STS-1<br>B1 = 00, other STS-1s | E1 | F1 |
| D1 | D2 | D3 |
| H1 | H2 | H3 |
| B2 | K1 | K2 |
| D4 | D5 | D6 |
| D7 | D8 | D9 |
| D10 | D11 | D12 |
| S1 | M1 | E2 |

The TOH values inserted in AUTO_SOH mode are shown in Table 5. If a specific value is not listed in the table, the bytes are transmitted transparently from the FPGA logic as in the transparent mode. Optionally K2 can be inserted by the core using the FORCE_RDI_xx control register bits. A1/A2 and B1 insertion can be independently enabled.

The TOH values inserted in AUTO_TOH mode are shown in Table 6. The values are for all STS-1s in the STS-48 frame unless noted otherwise.

***Table 6. Inserted TOH Values (All 0x) in AUTO_TOH Mode***

| | | |
|---|---|---|
| A1 = F6 | A2 = 28 | J0 = STS-1 ID,<br>every 4th. STS-1<br>J0 = 00, other STS-1s |
| B1 = calculated,<br>1st. STS-1<br>B1 = 00, other STS-1s | E1 = 00 | F1 = link number,<br>1st. STS-1<br>F1 = 00, other STS-1s |
| D1 = 00 | D2 = 00 | D3 = 00 |
| H1 = 62, 1st. STS-1<br>H1 = 93 other STS-1s | H2 = 0A, 1st. STS-1<br>H2 = FF other STS-1s | H3 = 00 |
| B2 = 00 | K1 = 00 | K2 = 06 for RDI,<br>K2 = 00 otherwise,<br>1st. STS-1<br>K2 = 00, other STS-1s |
| D4 = 00 | D5 = 00 | D6 = 00 |
| D7 = 00 | D8 = 00 | D9 = 00 |
| D10 = 00 | D11 = 00 | D12 = 00 |
| S1 = 00 | M1 = 00 | E2 = 00 |

The TOH block can perform A1/A2 corruption by inverting the A1/A2 bytes and also can forces B1 errors by inverting the B1 byte. A RDI can be injected by forcing the K2 byte to “00000110”. In SONET mode, all TOH bytes can be transparently sent from the FPGA as an option. Error and RDI insertion are controlled by software register bits as shown in the Register Map tables.

**Scramble Sub-block**

The scrambler scrambles the incoming 32-bit data using the standard SONET polynomial $1 + x^6 + x^7$. The scrambler can be disabled by a software register bit.

**32:8 MUX**

The MUX block is responsible for converting 32 bits of data at 77.76 MHz to 8 bits of data at 311.04 MHz. It will contain a small elastic store for clock domain transfer between the write clock from the FPGA to the divide-by-4 clock from the SERDES output clock (XCK311). It is recommended to use the clocking scheme shown to guaran-

**SPE Generator**

The SPE generator in the ORSO42G5 and ORSO82G5 is used to indicate the payload and overhead portions of a SONET frame. It is present in the SONET data path only. The SPE generator generates row, column and STS counters based on the frame pulse received from the (24 x 33) alignment FIFO or from the descrambler if alignment FIFOs are bypassed. It also retimes the 32-bit data in order to align it with the SPE indicator. The SPE generator will also detect negative or positive pointer justification (if justification is enabled) by looking at the ID bits in the H1 and H2 bytes and adjust the SPE indicator for the STS-1 frame being justified as follows:

- During positive pointer justification, the SPE will be low during H3 byte and the SPE byte following it.
- During negative pointer justification, the SPE will be high during H3 byte.
- During no justification, the SPE will be low during H3 byte.

This block only detects the incoming pointer bytes for SPE generation. This capability can be enabled by software control. By default, the SPE generator will ignore any pointer justification. This block has no capability of any pointer processing, pointer checking or pointer mover operation and ignores “new data” indications from the SONET specification.

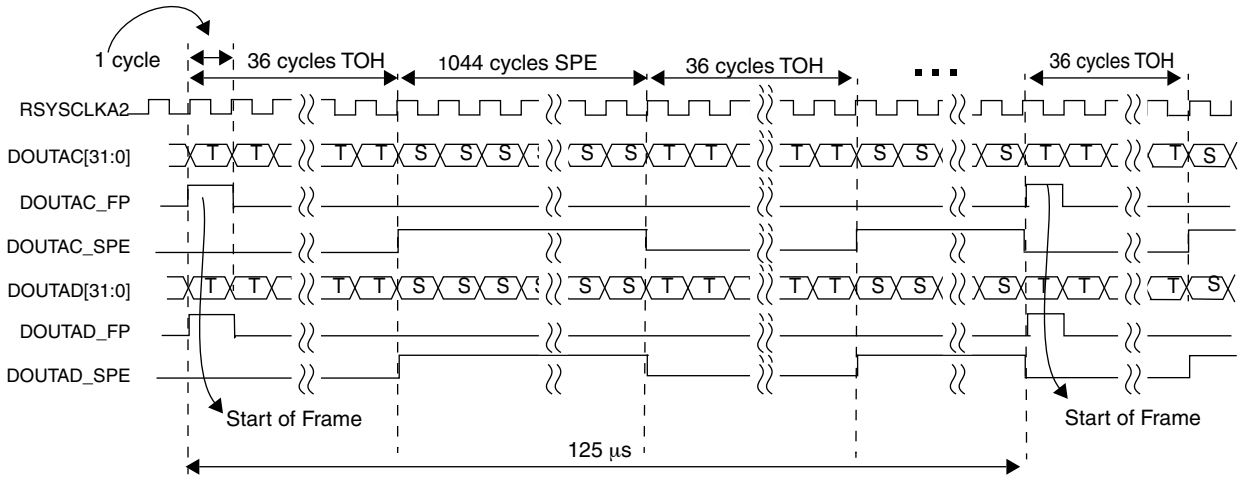
**SONET Mode Receive Timing – ORSO42G5**

This section contains timing diagrams for major interfaces of this block to the FPGA logic when SONET frames are to be transferred.

- When operating in SONET mode, the entire SONET frame is sent to the FPGA. In multi-channel alignment mode(s), data from all channels within an alignment group are aligned to the A1A2 framing bytes.
- Each SONET frame is 125μs. The frame starts with 36 clock cycles (77.76 MHz) of TOH followed by 1044 clock cycles of SPE, followed by 36 clock cycles of TOH, 1044 cycles of SPE.
- The DOUTxx_SPE signal indicates TOH or SPE in the data (low for TOH, high for SPE)
- Twin pairs are AC, AD (group A2) and BC, BD (group B2)

Figure 32 shows the SONET twin alignment mode timing for the ORSO42G5. The frame pulse and SPE indicators are show for each of the two channels (AC, AD) in twin alignment.

***Figure 30. Receive Clocking Diagram for SONET Mode Twin Alignment in Block A – ORSO42G5***




**Clocks**
RSYSCLKA2 is the read clock used for group A2
RSYSBLKB2 is the read clock used for group B2

**Data**
T Represents TOH
S Represents SPE
DOUTxx-SPE is high for SPE, low for TOH

**ORSO42G5 Configuration**

At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

- Setting bit 1 to one in registers at locations 30002, 30012, 30102 and 30112 powers down the legacy logic. (Note that the reset value for these bits is 0.)
- Setting bit 1 to zero (reset condition) in the register at locations 30802, 30812, 30902 and 30912 removes the legacy logic from any alignment group.

Register settings for SONET multi-channel alignment are shown in Table 7.

***Table 7. Multichannel Alignment Modes – ORSO42G5***

| Register Bits FMPU_SYNMODE_xx[2:3] | Mode |
|---|---|
| 00 | No multichannel alignment |
| 01 | Twin channel alignment |
| 11 | Four channel alignment |

Note: xx = [AC,AD,BC,BD]

To align two channels in SERDES A:

- FMPU_SYNMODE_AC = 01 (Register Location 30822)
- FMPU_SYNMODE_AD = 01 (Register Location 30832)

To align two channels in SERDES B:

- FMPU_SYNMODE_BC = 01 (Register Location 30922)
- FMPU_SYNMODE_BD = 01 (Register Location 30932)

To align all four channels:

- FMPU_SYNMODE_AC = 11 (Register Location 30822)
- FMPU_SYNMODE_AD = 11 (Register Location 30832)
- FMPU_SYNMODE_BC = 11 (Register Location 30922)
- FMPU_SYNMODE_BD = 11 (Register Location 30932)

To enable/disable multi-channel alignment of individual channels within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled

where xx = [AC,AD,BC,BD]

To resynchronize a multichannel alignment group set the following bits to one, and then set to zero:

- FMPU_RESYNC4 for four channels, AC, AD, BC and BD. (Register Location 30A04, bit 7)
- FMPU_RESYNCA2 for dual channels, AC and AD. (Register Location 30A04, bit 2)
- FMPU_RESYNCB2 for dual channels, BC and BD. (Register Location 30A04, bit 5)

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bits to one, and then set to zero.

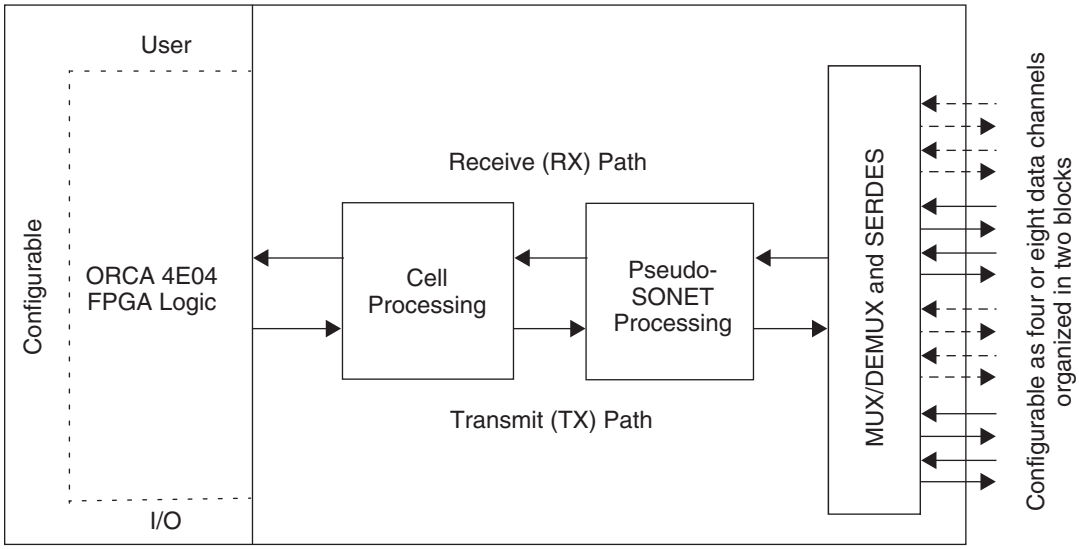
- FMPU_RESYNC1_xx (Register Locations 30824, 20834, 30924 and 30934, bit 7) where xx is one of AC, AD, BC or BD.

## Cell Mode Detailed Description

A common application for the ORSO42G5 and ORSO82G5 is to provide a bridge between a port card and a cell-based switch fabric. In cell mode, the data in the Synchronous Payload Envelope (SPE) of the SONET frames is further formatted into fixed-length cells by the ORSO42G5 and ORSO82G5. The cell contents will typically be unique to specific port card and switch devices. The ORSO42G5 and ORSO82G5 supports this application with a "cell mode" of operation

The basic data flows in cell mode are shown in Figure 35. Data to be transmitted is received from the FPGA logic (see Table 11 and Table 12 for details of the core/FPGA signal assignments in the transmit direction which differ significantly from the SERDES only and SONET modes), inserted into the SPE of the SONET frame, scrambled and transmitted from the SERDES block. In cell mode, multiple SERDES links are used to achieve desired bandwidth. A two-link mode is supported in the ORSO42G5 and both two-link and eight-link cell modes are supported. For such interfaces, data are cell-striped in a round-robin fashion across multiple links by the transmitter.

***Figure 35. Basic Data Flows - Cell Mode***




In the receive direction, the framed data are received from the SERDES block, descrambled and are passed into a cell extractor which extracts individual cells from the payload portion of the SONET frame. The cells are then passed through a FIFO that performs lane-to-lane deskew and a clock domain transfer. The clock domain transfer is handled automatically using idle cell insertion and deletion.

The cells are passed into either the eight-link Input Port Controller IPC8 block (ORSO82G5 only) or to one of the two-link IPC2 block(s), which reassemble the cells back into a single cell stream (destriping) which is sent to the FPGA logic. (See Table 13 and Table 14 for details of the core/FPGA signal assignments in the receive direction. As with the transmit path, the cell mode assignments differ significantly from those for the SERDES only and SONET modes).

SERDES and SONET processing has been described in previous sections and only features unique to the cell mode will be discussed in the following sections. The cell format will be discussed first, followed by a description of the transmit path, which will include either a two-link or an eight-link Output Port Controller (OPC) block, and a description of the receive path, including the two-link or eight-link Input Port Controller (IPC) blocks.

**Cell Formats**

Cells are arranged within a SONET (STS-48c) frame as shown in Figure 36. A SONET STS-48c frame has 4176 (87 x 48) columns of SPE and 9 rows that gives a total of 37,584 bytes. In this implementation, data in a SPE is limited to fixed size cells. Though four cell sizes are supported, only one cell size can be used at a time.

*Table 12. TX FPGA/Core Interface Signaling – ORSO82G5 (Continued)*

| | | | |
|---|---|---|---|
| [39:33] | — | — | — |
| 32 | DINAD_FP | — | — |
| [31:21] | DINAD[31:21] | — | — |
| 20 | DINAD[20] | — | OPC8_CELLVALID |
| [19:0] | DINAD[19:0] | OPC2_A2[19:0] | OPC8[99:80] |
| **TXDBA** | **SONET Mode** | **OPC2 B1 Mode** | **OPC8 Mode** |
| [39:33] | — | — | — |
| 32 | DINBA_FP | — | — |
| [31:21] | DINBA[31:21] | — | — |
| 20 | DINBA[20] | OPC2_B1_CELLVALID | — |
| [19:0] | DINBA[19;0]] | OPC2_B1[39:20] | OPC8[79:60] |
| | | | |
| **TXDBB** | **SONET Mode** | **OPC2 B1 Mode** | **OPC8 Mode** |
| [39:33] | — | — | — |
| 32 | DINBB_FP | — | — |
| [31:20] | DINBB[31:20] | — | — |
| [19:0] | DINBB[19:0] | OPC2_B1[19:0] | OPC8[59:40] |
| | | | |
| **TXDBC** | **SONET Mode** | **OPC2 B2 Mode** | **OPC8 Mode** |
| [39:33] | — | — | — |
| 32 | DINBC_FP | — | — |
| [31:21] | DINBC[31:21] | — | — |
| 20 | DINBC[20] | OPC2_B2_CELLVALID | — |
| [19:0] | DINBC[19:0] | OPC2_B2[39:20] | OPC8[39:20] |
| | | | |
| **TXDBD** | **SONET Mode** | **OPC2 B2 Mode** | **OPC8 Mode** |
| [39:33] | — | — | — |
| 32 | DINBD_FP | — | — |
| [31:20] | DINBD[31:20] | — | — |
| [19:0] | DINBD[19:0] | OPC2_B2[19:0] | OPC8[19:0] |

**Signal Description for RX Path (SERDES Core to FPGA) – ORSO42G5**

- Signals are divided across four channels with 40 signals per channel. RXDxx[39:0] is the set of 40 signals for a channel xx.
- All RX direction signals are outputs from the core.
- See Figure 47 for clock transfers across the FPGA/Core interface.
- In SONET mode, RXDxx[31:0] carries 32 bit data from the alignment FIFO of the respective channel. RXDxx[35:32] carries miscellaneous information such as OOF, BIPERR, Frame Pulse (FP), and SPE.
- In cell mode, data from each of the four 2-link IPC bundles are spread across all eight channels and are assigned to the 20 LSBs (RXDxx[19:0]) of each channel output. Data from IPC2_A1 is distributed across RXDAA[19:0] and RXDAB[19:0]. Data from IPC2_A2 is distributed across RXDAC[19:0] and RXDAD[19:0]. This symmetry is maintained for IPC2 data signals from block B.
- The IPC status signals for Cell Mode operation are contained in RXDxx[39:36] and RXDxx[33].
- The signals for SONET Mode operation are assigned to RXDxx[35:34] and RXDxx[33].

- Note that RXDxx[39:32] signal assignments are the same no matter what mode the RX blocks are in.

Table 13 summarizes the signals across the Core/FPGA interface in the receive direction.

***Table 13. RX Core/FPGA Interface Signals – ORSO42G5***

| RXDAC[39:0] | SONET mode | IPC2 A2 Mode |
|---|---|---|
| 39 | SYNC2_A2_OOS | — |
| 38 | — | IPC2_A2_CELLDROP |
| 37 | — | IPC2_A2_CELLSTART |
| 36 | DOUTAC_FP | — |
| 35 | DOUTAC_OOF | |
| 34 | DOUTAC_SPE | — |
| 33 | — | IPC2_A2_CELL_BIP_ERR |
| 32 | DOUTAC_B1_ERR | |
| [31:20] | DOUTAC[31:20]] | — |
| [19:0] | DOUTAC[19:0] | IPC2_A2[39:20] |
| | | |
| RXDAD[39:0] | SONET Mode | IPC2 A2 Mode |
| 39 | — | — |
| 38 | — | — |
| 37 | — | CELL_BEGIN_OK_A2 |
| 36 | DOUTAD_FP | — |
| 35 | DOUTAD_OOF | |
| 34 | DOUTAD_SPE | — |
| 33 | — | — |
| 32 | DOUTAD_B1_ERR | |
| [31:20] | DOUTAD[31:20] | — |
| [19:0] | DOUTAD[19:0] | IPC2_A2[19:0] |
| | | |
| RXDBC[39:0] | SONET Mode | IPC2 B2 Mode |
| 39 | SYNC2_B2_OOS | — |
| 38 | — | IPC2_B2_CELLDROP |
| 37 | — | IPC2_B2_CELLSTART |
| 36 | DOUTBC_FP | — |
| 35 | DOUTBC_OOF | |
| 34 | DOUTBC_SPE | — |
| 33 | — | IPC2_B2_CELL_BIP_ERR |
| 32 | DOUTBC_B1_ERR | |
| [31:20] | DOUTBC[31:20] | — |
| [19:0] | DOUTBC[19:0] | IPC2_B2[39:20] |
| RXDBD[39:0] | SONET Mode | IPC2 B2 Mode |
| 39 | — | |
| 38 | SYNC4_B_OOS | — |
| 37 | — | CELL_BEGIN_OK_B2 |
| 36 | DOUTBD_FP | — |
| 35 | DOUTBD_OOF | |
| 34 | DOUTBD_SPE | — |

- Toggle SOFT_RESET once all clocks have stabilized
  - 30A06 01
  - 30A06 00

**3. SONET Alignment FIFO Resynchronization – ORSO42G5**

If during operation a link goes OOF the alignment group will continue to run without the errored channel. To realign this link with the rest of group once the OOF condition is cleared the group may need to be resynchronized. This operation (for 4 channel alignment in block A) is shown below.

- Toggle the FMPU_RESYNC2_A2 register bit to reset the alignment FIFO group.
  - 30A04 04
  - 30A04 00

This sequence will stop traffic temporarily on all links in the alignment grouping.

**4. Two-Link Cell Mode Initialization – ORSO42G5**

This sample initialization uses 2-link cell mode on all links (A1, A2, B1, and B2). Auto_Bundle and Auto_Remove are both used for these links. The GSWRST_[A:B] Rejoin method is used.

- Set SERDES PLL to Lock to Data signal and Auto_TOH mode (per channel, all channels)
  - 30824 and 30834 82
- Enable Auto_Remove and Rejoin
  - 30A03 1B
- Set 2-link cell mode for groups A2 and B2
  - 30A05 0A
- Toggle SOFT_RESET
  - 30A06 01
  - 30A06 00
- Set the TX_CFG_DONE bit to indicate the transmitter is completely configured
  - 30A07 01
- Toggle GSWRST_[A:B] to clear the RX FIFOs
  - 30005 20
  - 30105 20
  - 30005 00
  - 30105 00
- Turn Off Rejoin (clear the Rejoin register bits) and enable Auto_Bundle
  - 30A03 49

## Sample Initialization Sequences – ORSO82G5

The following paragraphs show sample control register write sequences for initialization and resynchronization for the major modes of the device. Hexadecimal values will be shown for the data to be written into the control registers. For these values bit 0 will be the MSb while bit 7 is the LSb. For the per-channel control registers, only the first register address is shown. The other per-channel control registers must also be initialized for the desired mode.

**1. SERDES-Only Mode Initialization – ORSO82G5**

- Set SERDES Only mode (per channel, channel AA selected for sample initialization)
  - 30803 40
- Set SERDES PLL to Lock to Data signal (per channel, channel AA selected for sample initialization)
  - 30804 80

*Table 25. SERDES Per-Block Control Register Descriptions – ORSO42G5*

| (0x) Absolute Address | Bit | Name | Reset Value (0x) | Description | Mode |
|---|---|---|---|---|---|
| **SERDES Per-Block Control Register (Read/Write) xx = [AC, AD, BC, BD]** | | | | | |
| 30005 - A<br>30105 - B | [0] | RSVD | 44 | Reserved | — |
| | [1] | GMASK_[A:B] | | Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of all channel in the SERDES block are prevented from generating an alarm (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset. | Both |
| | [2] | GSWRST_[A:B] | | Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of all four channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset. | Both |
| | [3] | GPWRDNT_[A:B] | | Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for all four channels are powered down. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset. | Both |
| | [4] | GPWRDNR_[A:B] | | Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for all four channels are powered down. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset. | Both |
| | [5:6] | RSVD | | Reserved | — |
| | [7] | GTESTEN_[A:B] | | Global Test Enable Bit. When GTESTEN_[A:B] = 1, the transmit and receive sections of all channels in the block are place in test mode. The TESTMODE_xx bits (30026, 30126, etc.) must be set to specify the desired test on a per-channel basis. The GTESTEN_[A:B] bits override the individual TESTEN_xx settings. | Factory |

*Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)*

| (0x) Absolute Address | Bit | Name | Reset Value (0x) | Description | Mode |
|---|---|---|---|---|---|
| 30823 - AC<br>30833 - AD<br><br>30923 - BC<br>30933 - BD | [0] | BYPASS_ALGN_FIFO_xx | 00 | Bypass alignment FIFO =1 in RX path in SONET mode. DOUT_xx data is clocked off RWCKxx. | SONET |
| | [1] | SERDES_ONLY_MODE_xx | | SERDES-Only Mode. SERDES_ONLY_MODE =1 bypasses all the SONET and cell functions. Data is sent directly from the SERDES to the FPGA logic in the RX path and is passed directly from the FPGA logic to the SERDES in the TX path. | SERDES Only |
| | [2] | FORCE_B1_ERR_xx | | Force B1 Error. FORCE_B1_ERR =1 forces a Section B1 error (Bit Interleaved Parity Error) in the TX path. Valid only when the corresponding AUTO_TOH_xx bit or AUTO_B1_xx bit is set to one. | Both |
| | [3] | FORCE_BIP8_ERR_xx | | Force BIP8 Error, FORCE_BIP8_ERR =1 forces cell BIP8 error in the TX path. | Cell |
| | [4] | FORCE_A1A2_ERR_xx | | Force A1A2 Error, FORCE_A1A2_ERR =1 forces an error in A1A2 bytes (framing error) in the TX path. Valid only when the corresponding AUTO_TOH_xx bit or AUTO_A1A2_xx bit is set to one. | Both |
| | [5] | FORCE_EX_SEQ_ERR_xx | | Force Excessive Sequence Errors. FORCE_EXP_SEQ_ERR_xx = 1 forces sequence errors in the TX path by inverting the link header byte sequence number. | Cell |
| | [6] | FORCE_SEQ_ERR_xx | | Force Sequence Error, FORCE_SEQ_ERR =1 forces one sequence error in the TX path. After this bit is set, the next Link Header byte's sequence number is inverted. The Link Header after the errored Link Header byte will have the correct sequence number | Cell |
| | [7] | FORCE_RDI_xx | | Force Remote Defect Indication, FORCE_RDI =1 forces RDI errors in the TX path. The K2 byte in TOH is set to "00000110. Valid only when AUTO_TOH_xx bit is set to 1. | Cell |

*Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)*

| (0x) Absolute Address | Bit | Name | Reset Value (0x) | Description | Mode |
|---|---|---|---|---|---|
| 30824 - AC<br>30834 - AD<br><br>30924 - BC<br>30934 - BD | [0] | LCKREFN_xx | 00 | 0 = Lock receiver to reference clock (REFCLK)<br>1 = Lock receiver to HDINxx data | Both |
| | [1] | LOOPENB_xx | | LOOPENB_xx =1 Enable high-speed internal loopback from TX to RX. Disable the HDOUT buffers. | Both |
| | [2] | DISABLE_TX_xx | | Disable Transmitter, For DISABLE_TX = 1 the TX Link is disabled. The disabled link is ignored by the Output Port Controller (OPC) and internally generated idle cells are transmitted on the link.fIf the link is disabled during the transmission of a cell on the link, the entire cell is transmitted before the link is declared invalid. | Cell |
| | [3] | DISABLE_RX_xx | | Disable Receiver, DISABLE_RX = 1 disables the RX link for cell processing by the Input Port Controller (IPC). The IPC will not read cells from a link if this bit is set for that link | Cell |
| | [4] | CELL_BIP_INH_xx | | Cell BIP (Check) Inhibit, CELL_BIP_INH = 1 prevents cells from being dropped due to a Cell BIP error, in the RX path. If this bit is not set, then cells will be dropped automatically if a cell bip error is detected by the core. The CELLDROP signal across the core-FPGA interface will be active only if this bit is NOT set. | Cell |
| | [5] | CELL_SEQ_INH_xx | | Cell Sequence (Checking) Inhibit, CELL_SEQ_INH = 1 prevents cells in the RX path from being dropped due to a sequence error. If this bit is not set, then cells will be dropped automatically if a sequence error is detected internally. The CELLDROP signal across the core-FPGA interface will be active only if this bit is NOT set. | Cell |
| | [6] | AUTO_TOH_xx | | Automatic TOH Generation, AUTO_TOH_xx =1 enables the TX core to automatically generate TOH bytes. All the FORCE_* register bits are valid if this bit is set. This bit should be set to 1 in Cell Mode. It can be set to 1or 0 in SONET Mode. If this bit is not set, then user has to provide all the TOH bytes or use the AUTO_SOH mode. | SONET |
| | [7] | FMPU_RESYNC1_xx | | Single channel alignment FIFO reset. Rising edge sensitive. Write a 0 and then a 1 to enable this bit. When enabled, the read pointer in the alignment FIFO is reset to the middle of the FIFO. This bit is valid only when FMPU_SYNMODE_xx = 00 (no multi channel alignment) | SONET |
| 30825 - AC<br>30835 - AD<br><br>30925 - BC<br>30935 - BD | [0:7] | LINK_NUM_TX_xx | 00 | Transmit Link Number, This value is transmitted in the “F1” byte of the TOH. This value is used to verify that the links are connected properly and is only used in the AUTO_TOH mode. | Both |

*Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)*

| (0x) Absolute Address | Bit | Name | Reset Value (0x) | Description | Mode |
|---|---|---|---|---|---|
| 30A08 | [0] | ALARM_STATUS_BD | 00 | Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BD. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side). | Both |
| | [1] | ALARM_STATUS_BC | | Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BC. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side). | Both |
| | [2] | ALARM_STATUS_BB | | Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BB. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side). | Both |
| | [3] | ALARM_STATUS_BA | | Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BA. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side). | Both |
| | [4] | ALARM_STATUS_AD | | Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AD. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side). | Both |
| | [5] | ALARM_STATUS_AC | | Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AC. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side). | Both |
| | [6] | ALARM_STATUS_AB | | OR of all alarm status bits for channel AB. A 1 on this bit will set the alarm pin on the system bus interrupt cause register (on the FPGA side) | Both |
| | [7] | ALARM_STATUS_AA | | Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AA. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side). | Both |
| 30A09 | [0:7] | B1_ERR_CNT | 00 | Error counter that increments when a section B1 error is detected on a link. The link is selected using ERRCNT_CHSEL. This counter is cleared on read. | Both |
| 30A0A | [0:7] | CELL_BIP_ERR_CNT | 00 | Cell BIP Error Counter, Error counter that increments when a Cell BIP error is detected on a link. The link being monitored is selected using ERRCNT_CHSEL. This counter is cleared on read. | Cell |

*Table 47. Pin Descriptions (Continued)*

| Symbol | I/O | Description |
|---|---|---|
| P[TBLR]CLK[1:0][TC] | I | Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing. |
| | I/O | After configuration these pins are user programmable I/O, if not used for clock inputs. |
| TDI, TCK, TMS | I | If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration. |
| | I/O | After configuration, these pins are user-programmable I/O if boundary scan is not used.[1] |
| RDY/$\overline{\text{BUSY}}$/RCLK | O | During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode.<br>During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used. |
| | I/O | After configuration this pin is a user-programmable I/O pin.[1] |
| HDC | O | High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete. |
| | I/O | After configuration, this pin is a user-programmable I/O pin.[1] |
| $\overline{\text{LDC}}$ | O | $\overline{\text{Low During Configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete. |
| | I/O | After configuration, this pin is a user-programmable I/O pin.[1] |
| $\overline{\text{INIT}}$ | I/O | $\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration.<br>After configuration, this pin is a user-programmable I/O pin.[1] |
| $\overline{\text{CS0}}$, CS1 | I | $\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled. |
| | I/O | After configuration, if MPI is not used, these pins are user-programmable I/O pins.[1] |
| $\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$ | I | $\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides.<br>This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy. |
| $\overline{\text{WR}}$/MPI_RW | I | $\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA.<br>In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA. |
| | I/O | After configuration, if the MPI is not used, $\overline{\text{WR}}$/MPI_RW is a user-programmable I/O pin.[1] |
| PPC_A[14:31] | I | During MPI mode the PPC_A[14:31] are used as the address bus driven by the PowerPC bus master utilizing the least-significant bits of the PowerPC 32-bit address. |
| $\overline{\text{MPI\_BURST}}$ | I | $\overline{\text{MPI\_BURST}}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst. |
| $\overline{\text{MPI\_BDIP}}$ | I | $\overline{\text{MPI\_BDIP}}$ is driven by the PowerPC processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase. |
| MPI_TSZ[0:1] | I | MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word. |
| A[21:0] | O | During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes. |
| | I/O | If not used for MPI these pins are user-programmable I/O pins after configuration.[1] |

*Table 47. Pin Descriptions (Continued)*

| Symbol | I/O | Description |
|---|---|---|
| MPI_ACK | O | In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle. |
| | I/O | If not used for MPI these pins are user-programmable I/O pins after configuration.[1] |
| MPI_CLK | I | This is the PowerPC synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the Embedded System Bus. If MPI is used this will be the AMBA bus clock. |
| | I/O | If not used for MPI these pins are user-programmable I/O pins after configuration.[1] |
| MPI_TEA | O | A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction. |
| | I/O | If not used for MPI these pins are user-programmable I/O pins after configuration.[1] |
| MPI_RTRY | O | This pin requests the MPC860 to relinquish the bus and retry the cycle. |
| | I/O | If not used for MPI these pins are user-programmable I/O pins after configuration.[1] |
| D[0:31] | I/O | Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction. |
| | I | D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input. |
| | O | D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low. |
| | I/O | After configuration, if MPI is not used, the pins are user-programmable I/O pins.[1] |
| DP[0:3] | I/O | Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31].<br>After configuration, if MPI is not used, the pins are user-programmable I/O pin.[1] |
| DIN | I | During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled. |
| | I/O | After configuration, this pin is a user-programmable I/O pin.[1] |
| DOUT | O | During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK. |
| | I/O | After configuration, DOUT is a user-programmable I/O pin.[1] |
| TESTCFG (ORSO82G5 only) | I | During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration. |
| | I/O | After configuration, TESTCFG is a user programmable I/O pin.[1] |

1. The FPGA States of Operation section in the ORCA Series 4 FPGAs data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

*Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)*

| 484-PBGAM | VDDIO Bank | VREF Group | I/O | Pin Description | Additional Function | 484-PBGAM |
|---|---|---|---|---|---|---|
| C1 | 0 (TL) | 7 | IO | PL2C | PLL_CK0T/HPPLL | L1T |
| F3 | 0 (TL) | 7 | IO | PL3C | VREF_0_07 | - |
| A1 | - | - | VSS | VSS | - | - |
| D2 | 0 (TL) | 7 | IO | PL4D | D5 | L2C |
| D1 | 0 (TL) | 7 | IO | PL4C | D6 | L2T |
| E7 | 0 (TL) | - | VDDIO0 | VDDIO0 | - | - |
| E2 | 0 (TL) | 8 | IO | PL5D | HDC | L3C |
| E1 | 0 (TL) | 8 | IO | PL5C | LDC_N | L3T |
| G3 | 0 (TL) | 8 | IO | PL5A | - | - |
| G4 | 0 (TL) | 9 | IO | PL6C | D7 | - |
| F2 | 0 (TL) | 9 | IO | PL7D | VREF_0_09 | L4C |
| F1 | 0 (TL) | 9 | IO | PL7C | A17/PPC_A31 | L4T |
| G2 | 0 (TL) | 9 | IO | PL8D | CS0_N | L5C |
| G1 | 0 (TL) | 9 | IO | PL8C | CS1 | L5T |
| E8 | 0 (TL) | - | VDDIO0 | VDDIO0 | - | - |
| A2 | - | - | VSS | VSS | - | - |
| H1 | 0 (TL) | 10 | IO | PL10D | INIT_N | L6C |
| H2 | 0 (TL) | 10 | IO | PL10C | DOUT | L6T |
| E5 | - | - | VDD15 | VDD15 | - | - |
| H4 | 0 (TL) | 10 | IO | PL11D | VREF_0_10 | - |
| H3 | 0 (TL) | 10 | IO | PL11C | A16/PPC_A30 | - |
| J1 | 7 (CL) | 1 | IO | PL12D | A15/PPC_A29 | L7C |
| J2 | 7 (CL) | 1 | IO | PL12C | A14/PPC_A28 | L7T |
| J4 | 7 (CL) | 1 | IO | PL13C | D4 | - |
| G7 | - | - | VSS | VSS | - | - |
| J3 | 7 (CL) | 2 | IO | PL14D | RDY/BUSY_N/RCLK | - |
| K6 | 7 (CL) | - | VDDIO7 | VDDIO7 | - | - |
| K1 | 7 (CL) | 2 | IO | PL15D | A13/PPC_A27 | L8C |
| K2 | 7 (CL) | 2 | IO | PL15C | A12/PPC_A26 | L8T |
| K3 | 7 (CL) | 3 | IO | PL16C | - | - |
| K4 | 7 (CL) | 3 | IO | PL17D | A11/PPC_A25 | - |
| G8 | - | - | VSS | VSS | - | - |
| F8 | - | - | VDD15 | VDD15 | - | - |
| K5 | 7 (CL) | 4 | IO | PL19D | RD_N/MPI_STRB_N | - |
| L1 | 7 (CL) | 4 | IO | PL20D | PLCK0C | L9C |
| L2 | 7 (CL) | 4 | IO | PL20C | PLCK0T | L9T |
| L6 | 7 (CL) | - | VDDIO7 | VDDIO7 | - | - |
| F9 | - | - | VDD15 | VDD15 | - | - |
| G9 | - | - | VSS | VSS | - | - |
| L3 | 7 (CL) | 5 | IO | PL21D | A10/PPC_A24 | L10C |
| L4 | 7 (CL) | 5 | IO | PL21C | A9/PPC_A23 | L10T |
| L5 | 7 (CL) | 5 | IO | PL22D | A8/PPC_A22 | - |
| F10 | - | - | VDD15 | VDD15 | - | - |
| G10 | - | - | VSS | VSS | - | - |

*Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)*

| 484-PBGAM | VDDIO Bank | VREF Group | I/O | Pin Description | Additional Function | 484-PBGAM |
|---|---|---|---|---|---|---|
| G16 | - | - | VDD15 | VDD15 | - | - |
| H13 | - | - | VSS | VSS | - | - |
| AB10 | 5 (BC) | 2 | IO | PB19A | - | L37T |
| AA10 | 5 (BC) | 2 | IO | PB19B | - | L37C |
| W10 | 5 (BC) | 2 | IO | PB19C | PBCK0T | L38T |
| Y10 | 5 (BC) | 2 | IO | PB19D | PBCK0C | L38C |
| V10 | 5 (BC) | 2 | IO | PB20A | - | - |
| U13 | 5 (BC) | - | VDDIO5 | VDDIO5 | - | - |
| AB11 | 5 (BC) | 2 | IO | PB20C | VREF_5_02 | L39T |
| AA11 | 5 (BC) | 2 | IO | PB20D | - | L39C |
| U10 | 5 (BC) | 2 | IO | PB21A | - | - |
| H6 | - | - | VDD15 | VDD15 | - | - |
| Y11 | 5 (BC) | 3 | IO | PB21C | - | L40T |
| W11 | 5 (BC) | 3 | IO | PB21D | VREF_5_03 | L40C |
| U11 | 5 (BC) | 3 | IO | PB22A | - | - |
| J7 | - | - | VSS | VSS | - | - |
| AB12 | 5 (BC) | 3 | IO | PB22C | - | L41T |
| AA12 | 5 (BC) | 3 | IO | PB22D | - | L41C |
| U12 | 5 (BC) | 3 | IO | PB23A | - | - |
| Y12 | 5 (BC) | 3 | IO | PB23C | PBCK1T | L42T |
| W12 | 5 (BC) | 3 | IO | PB23D | PBCK1C | L42C |
| V11 | 5 (BC) | 3 | IO | PB24A | - | - |
| J8 | - | - | VSS | VSS | - | - |
| AB13 | 5 (BC) | 4 | IO | PB24C | - | L43T |
| AA13 | 5 (BC) | 4 | IO | PB24D | - | L43C |
| V12 | 5 (BC) | 4 | IO | PB25A | - | - |
| U14 | 5 (BC) | - | VDDIO5 | VDDIO5 | - | - |
| AB14 | 5 (BC) | 4 | IO | PB25C | - | L44T |
| AA14 | 5 (BC) | 4 | IO | PB25D | VREF_5_04 | L44C |
| J9 | - | - | VSS | VSS | - | - |
| Y13 | 5 (BC) | 5 | IO | PB26C | - | L45T |
| W13 | 5 (BC) | 5 | IO | PB26D | VREF_5_05 | L45C |
| U15 | 5 (BC) | - | VDDIO5 | VDDIO5 | - | - |
| AB15 | 5 (BC) | 5 | IO | PB27C | - | L46T |
| AA15 | 5 (BC) | 5 | IO | PB27D | - | L46C |
| AB16 | 5 (BC) | 6 | IO | PB28C | - | L47T |
| AA16 | 5 (BC) | 6 | IO | PB28D | VREF_5_06 | L47C |
| H14 | - | - | VDD15 | VDD15 | - | - |
| Y14 | 5 (BC) | 6 | IO | PB29C | - | L48T |
| W14 | 5 (BC) | 6 | IO | PB29D | - | L48C |
| J10 | - | - | VSS | VSS | - | - |
| AB17 | 5 (BC) | 7 | IO | PB30C | - | L49T |
| AA17 | 5 (BC) | 7 | IO | PB30D | - | L49C |
| U16 | 5 (BC) | - | VDDIO5 | VDDIO5 | - | - |

*Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)*

| 484-PBGAM | VDDIO Bank | VREF Group | I/O | Pin Description | Additional Function | 484-PBGAM |
|---|---|---|---|---|---|---|
| K13 | - | - | VSS | VSS | - | - |
| B21 | 1 (TC) | 9 | IO | PT31D | - | L55C |
| A21 | 1 (TC) | 9 | IO | PT31C | VREF_1_09 | L55T |
| E13 | 1 (TC) | - | VDDIO1 | VDDIO1 | - | - |
| D14 | 1 (TC) | 9 | IO | PT30D | - | L56C |
| C14 | 1 (TC) | 9 | IO | PT30C | - | L56T |
| K14 | - | - | VSS | VSS | - | - |
| B20 | 1 (TC) | 9 | IO | PT29D | - | L57C |
| A20 | 1 (TC) | 9 | IO | PT29C | - | L57T |
| N7 | - | - | VDD15 | VDD15 | - | - |
| B19 | 1 (TC) | 1 | IO | PT28D | - | L58C |
| A19 | 1 (TC) | 1 | IO | PT28C | - | L58T |
| L8 | - | - | VSS | VSS | - | - |
| D13 | 1 (TC) | 1 | IO | PT27D | VREF_1_01 | L59C |
| C13 | 1 (TC) | 1 | IO | PT27C | - | L59T |
| E18 | 1 (TC) | - | VDDIO1 | VDDIO1 | - | - |
| A18 | 1 (TC) | 1 | IO | PT27B | - | L60C |
| B18 | 1 (TC) | 1 | IO | PT27A | - | L60T |
| A17 | 1 (TC) | 2 | IO | PT26D | - | L61C |
| B17 | 1 (TC) | 2 | IO | PT26C | VREF_1_02 | L61T |
| L9 | - | - | VSS | VSS | - | - |
| D12 | 1 (TC) | 2 | IO | PT25D | - | L62C |
| C12 | 1 (TC) | 2 | IO | PT25C | - | L62T |
| E19 | 1 (TC) | - | VDDIO1 | VDDIO1 | - | - |
| A16 | 1 (TC) | 3 | IO | PT24D | - | L63C |
| B16 | 1 (TC) | 3 | IO | PT24C | VREF_1_03 | L63T |
| A15 | 1 (TC) | 3 | IO | PT23D | - | L64C |
| B15 | 1 (TC) | 3 | IO | PT23C | - | L64T |
| F16 | 1 (TC) | - | VDDIO1 | VDDIO1 | - | - |
| E11 | 1 (TC) | 3 | IO | PT22D | - | - |
| L10 | - | - | VSS | VSS | - | - |
| D11 | 1 (TC) | 4 | IO | PT21D | - | L65C |
| C11 | 1 (TC) | 4 | IO | PT21C | - | L65T |
| A14 | 1 (TC) | 4 | IO | PT20D | - | L66C |
| B14 | 1 (TC) | 4 | IO | PT20C | - | L66T |
| A13 | 1 (TC) | 4 | IO | PT19D | - | L67C |
| B13 | 1 (TC) | 4 | IO | PT19C | VREF_1_04 | L67T |
| G14 | 1 (TC) | - | VDDIO1 | VDDIO1 | - | - |
| L11 | - | - | VSS | VSS | - | - |
| N15 | - | - | VDD15 | VDD15 | - | - |
| D10 | 1 (TC) | 5 | IO | PT18D | PTCK1C | L68C |
| C10 | 1 (TC) | 5 | IO | PT18C | PTCK1T | L68T |
| A12 | 1 (TC) | 5 | IO | PT17D | PTCK0C | L69C |
| B12 | 1 (TC) | 5 | IO | PT17C | PTCK0T | L69T |

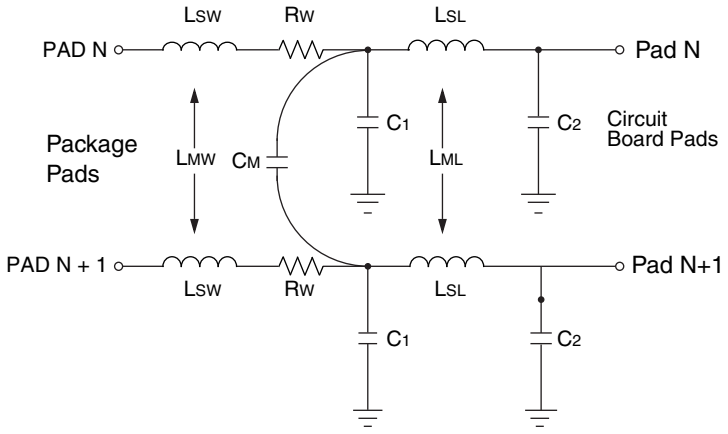
*Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)*

| 680-PBGAM | VDDIO Bank | VREF Group | I/O | Pin Description | Additional Function | 680-PBGAM |
|---|---|---|---|---|---|---|
| B29 | 1 (TC) | 8 | IO | PT33D | — | L1C_A0 |
| C29 | 1 (TC) | 8 | IO | PT33C | VREF_1_08 | L1T_A0 |
| B15 | 1 (TC) | — | VDDIO1 | VDDIO1 | — | — |
| E27 | 1 (TC) | 8 | IO | PT32D | — | L2C_A0 |
| E26 | 1 (TC) | 8 | IO | PT32C | — | L2T_A0 |
| AP34 | — | — | Vss | Vss | — | — |
| A30 | 1 (TC) | 8 | IO | PT32B | — | — |
| A29 | 1 (TC) | 9 | IO | PT31D | — | L3C_D3 |
| E25 | 1 (TC) | 9 | IO | PT31C | VREF_1_09 | L3T_D3 |
| B17 | 1 (TC) | — | VDDIO1 | VDDIO1 | — | — |
| E24 | 1 (TC) | 9 | IO | PT31A | — | — |
| B28 | 1 (TC) | 9 | IO | PT30D | — | L4C_A0 |
| C28 | 1 (TC) | 9 | IO | PT30C | — | L4T_A0 |
| B2 | — | — | Vss | Vss | — | — |
| D28 | 1 (TC) | 9 | IO | PT30A | — | — |
| C27 | 1 (TC) | 9 | IO | PT29D | — | L5C_A0 |
| D27 | 1 (TC) | 9 | IO | PT29C | — | L5T_A0 |
| E23 | 1 (TC) | 9 | IO | PT29B | — | L6C_A0 |
| E22 | 1 (TC) | 9 | IO | PT29A | — | L6T_A0 |
| D26 | 1 (TC) | 1 | IO | PT28D | — | L7C_A0 |
| D25 | 1 (TC) | 1 | IO | PT28C | — | L7T_A0 |
| B33 | — | — | Vss | Vss | — | — |
| D24 | 1 (TC) | 1 | IO | PT28B | — | L8C_A0 |
| D23 | 1 (TC) | 1 | IO | PT28A | — | L8T_A0 |
| C26 | 1 (TC) | 1 | IO | PT27D | VREF_1_01 | L9C_A0 |
| C25 | 1 (TC) | 1 | IO | PT27C | — | L9T_A0 |
| D11 | 1 (TC) | — | VDDIO1 | VDDIO1 | — | — |
| E21 | 1 (TC) | 1 | IO | PT27B | — | L10C_A0 |
| E20 | 1 (TC) | 1 | IO | PT27A | — | L10T_A0 |
| D22 | 1 (TC) | 2 | IO | PT26D | — | L11C_A0 |
| D21 | 1 (TC) | 2 | IO | PT26C | VREF_1_02 | L11T_A0 |
| E34 | — | — | Vss | Vss | — | — |
| A28 | 1 (TC) | 2 | IO | PT26B | — | — |
| B26 | 1 (TC) | 2 | IO | PT25D | — | L12C_A0 |
| B25 | 1 (TC) | 2 | IO | PT25C | — | L12T_A0 |
| D13 | 1 (TC) | — | VDDIO1 | VDDIO1 | — | — |
| B27 | 1 (TC) | 2 | IO | PT25B | — | — |
| A27 | 1 (TC) | 3 | IO | PT24D | — | L13C_A0 |
| A26 | 1 (TC) | 3 | IO | PT24C | VREF_1_03 | L13T_A0 |
| N13 | — | — | Vss | Vss | — | — |
| C24 | 1 (TC) | 3 | IO | PT24B | — | — |
| C22 | 1 (TC) | 3 | IO | PT23D | — | L14C_A0 |
| C23 | 1 (TC) | 3 | IO | PT23C | — | L14T_A0 |
| D15 | 1 (TC) | — | VDDIO1 | VDDIO1 | — | — |

***Table 54. ORCA Typical Package Parasitics***

| $L_{SW}$ | $L_{MW}$ | $R_W$ | $C_1$ | $C_2$ | $C_M$ | $L_{SL}$ | $L_{ML}$ |
|---|---|---|---|---|---|---|---|
| 3.8 | 1.3 | 250 | 1.0 | 1.0 | 0.3 | 2.8-5 | 0.5 -1 |

***Figure 53. Package Parasitics***




## Package Outline Drawings

Package Outline Drawings for the 484-ball PBGAM (fpBGA) used for the ORSO42G5 and 680-ball PBGAM (fpBGA) used for the ORSO82G5 are available at the Package Diagrams section of the Lattice Semiconductor web site at www.latticesemi.com.