Lattice Semiconductor Corporation - ORSO42G5-1BMN484I Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso42g5-1bmn484i

Embedded Function Features

- High-speed SERDES programmable serial data rates of 0.6 Gbps to 2.7 Gbps.
- Asynchronous operation per receive channel (separate PLL per channel).
- Transmit pre-emphasis (programmable) for improved receive data eye opening.
- Provides a 10 Gbps backplane interface to switch fabric using four work and, with the ORSO82G5, four protect 2.5 Gbit/s links. Also supports port cards at rates between 0.6 Gbps and 2.7 Gbps.
- Allows wide range of applications for SONET network termination, as well as generic data moving for high-speed backplane data transfer.
- No knowledge of SONET/SDH needed in generic applications. Simply supply data (75 MHz-168.75 MHz clock) and at least a single frame pulse.
- High-Speed Interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- Four- or eight-channel HSI functions provide 2.7 Gbps serial user data interface per channel for a total chip bandwidth of >10Gbps or >20 Gbps (full duplex).
- SERDES has low-power CML buffers and support for 1.5V/1.8V I/Os.
- SERDES HSI automatically recovers from loss-of-clock once its reference clock returns to normal operating state.
- Powerdown option of SERDES HSI receiver and/or transmitter on a per-channel basis.
- Ability to mix half-rate and full-rate between the channels with the same reference clock.
- Ability to configure each SERDES block independently with its own reference clock.
- STS-48 framing in SONET mode.
- Programmable enable of SONET scrambler/descrambler, A1/A2 insertion and B1 generation and checking.
- Insertion and checking of link assignment values to facilitate interconnection and debugging of backplanes.
- Optional AIS-L insertion during loss-of-frame.
- Optional RDI-L insertion to indicate remote far-end defects for maintenance capabilities.
- SPE signal marks payload bytes in SONET mode.
- Frame alignment across multiple ORSO42G5 and ORSO82G5 devices for work/protect switching at STS-768/STM-256 and above rates.
- Supports transparent mode where Transport OverHead (TOH) bytes are user-generated in the FPGA.
- Supports two modes of in-band management and configuration with TOH byte extraction/insertion by the Embedded core. A1/A2 and B1 insertion can be independently enabled.
  - AUTO_SOH where the embedded core inserts the A1/A2 framing bytes, performs the B1 calculation and inserts the B1 byte. All other bytes are passed through unchanged from the FPGA logic as in transparent mode.
  - AUTO_TOH where all of the overhead bytes are set by the embedded core. Most of the bytes are set to zero. At the receive side, all of the TOH bytes except those set to a non-zero value can be ignored.
- Optional A1/A2 corruption, B1 byte corruption, and K2 byte corruption for system debug purposes.
- Built-in boundary scan (*IEEE*® 1149.1 and 1149.2 JTAG), including the SERDES interface.
- FIFOs align incoming data across all eight channels (ORSO82G5 only), groups of four channels, or groups of two channels. Optional ability to bypass alignment FIFOs for asynchronous operation between channels is also provided. (Each channel includes its own recovered clock and frame pulse).

Dual Port RAMs

There are two independent memory blocks in the core. Each memory block has a capacity of 4K words by 36 bits. It has one read port, one write port, and four byte-write-enable (active-low) signals. The read data from the memory block is registered so that it works as a pipelined synchronous memory block. These memory blocks are completely independent of the backplane driver blocks. They are only accessible from the FPGA logic and are not connected to the system bus.

FPSC Configuration - Overview

Configuration of the ORSO42G5 and ORSO82G5 occurs in two stages: FPGA bit stream configuration and embedded core setup.

Prior to becoming operational, the FPGA goes through a sequence of states, including power-up, initialization, configuration, start-up, and operation. The FPGA logic is configured by standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet.

The options for the embedded core are set via registers that are accessed through the FPGA system bus. The system bus can be driven by an external PPC compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block, that drives the system by using the user interface and uses very little FPGA logic, is available in the *MPI/System Bus* application note (TN1017). This IP block sets up the embedded core via a state machine and allows the ORSO42G5 and ORSO82G5 to work in an independent system without an external MicroProcessor Interface.

ORSO42G5 and ORSO82G5 Embedded Core Detailed Description

The ORSO42G5 and ORSO82G5 have four and eight channels respectively, with a high-speed SERDES macro that performs clock data recovery, serializing and deserializing functions. There is also additional logic for SONET mode and cell mode data synchronization formatting and scrambling/descrambling. For all modes, the data paths can be characterized as the transmit path (FPGA to backplane) and receive path (backplane to FPGA); however the interface signal assignments between the FPGA logic and the core differ depending on the operating mode selected.

The three main operating modes in the ORSO42G5 and ORSO82G5 are:

- SERDES only mode
- SONET mode
- Cell mode
  - Two-link sub-mode
  - Eight-link sub-mode (ORSO82G5 only)

The SONET and cell modes each support sub-modes that can be selected by enabling or disabling certain functions through programmable register bits. Following the basic TX and RX architecture descriptions, the data formatting and logical implementations supporting each of the operational modes are described.

Top Level Description - Transmitter (TX) and Receiver (RX) Architectures

The next sections give a top level description of the transmitter and receive architectures. The high-speed transmit and receive serial data can operate at 0.6-2.7 Gbps depending on the state of the control bits from the system bus and the provided reference clock. For all of the architecture and clock distribution descriptions, however, the standard SONET STS-48 rate of 2,488.32 Mbits/s (i.e., REFCLK_[P:N] = 155.52 MHz for the full rate modes) is assumed.

Transmitter Architecture

The transmitter section accepts parallel data for transmission from the FPGA logic, formats it for transmission and serializes the data. It also accepts the low-speed reference clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock. The serialized transmitted data are available at the differential CML output pins to drive either an optical transmitters, coaxial media or a circuit board backplane.

The top level transmit architecture is shown in Figure 3. The main logical blocks in the transmit path are:

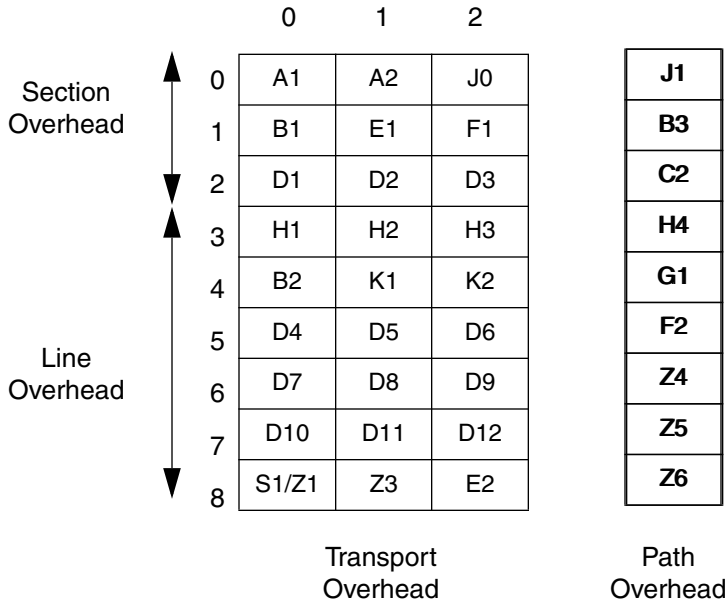
- Output Port Controllers (OPCs) which contain the cell processing logic.
- SONET processing logic.
- Transmit SERDES and 32:8 MUX.

Depending on the mode of operation, the FPGA to backplane data path may include or bypass the various logical blocks.

SONET TOH Byte Definitions

The Transport OverHead bytes of the SONET frame can be used for in-band configuration, service, and management since it is carried along the same channel as data. In the ORSO42G5 and ORSO82G5 in-band signaling can be efficiently utilized, since the total cost of overhead is only 3.3%. The overhead bytes in an STS-1 header are shown in Table 15 (The path overhead bytes are in the SPE.)

Figure 15. SONET Overhead Bytes



When used in true SONET applications, all or most TOH bytes will be generated in the FPGA logic or by an external device. Two modes are provided for this application – transparent and AUTO_SOH. In transparent mode all bytes from the FPGA logic are passed through unchanged.

In AUTO_SOH mode the embedded core inserts the A1/A2 framing bytes, performs the B1 calculation and inserts the B1 byte. A1/A2 and B1 insertion can be independently enabled. This avoids the need to do SONET scrambling in the FPGA logic. All other bytes are passed through unchanged from the FPGA logic as in transparent mode.

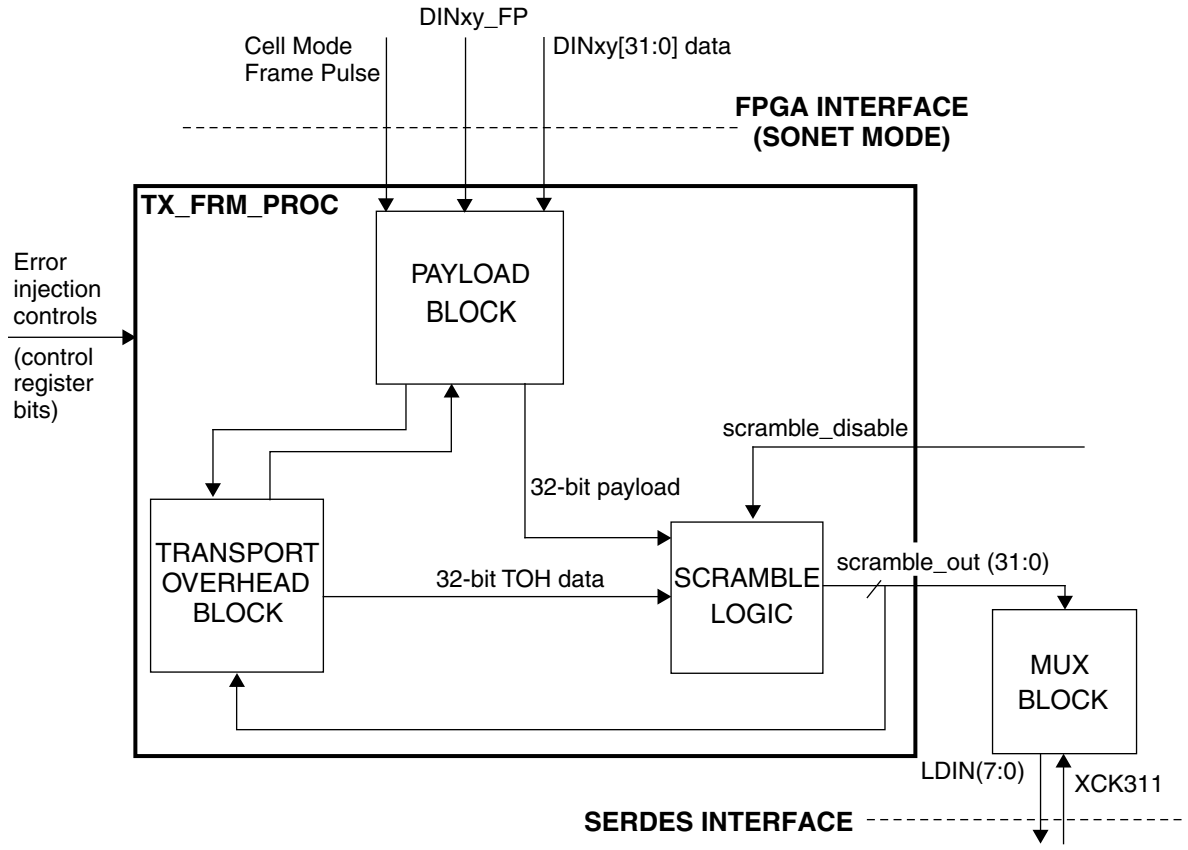
When used for applications that transfer non-SONET data, an AUTO_TOH mode is provided. In this mode, all of the overhead bytes are set by the embedded core. Most of the bytes are set to zero. At the receive side, all of the TOH bytes except those set to a non-zero value can be ignored in the AUTO_TOH mode.

The TOH bytes have the following functions in true SONET applications.

Section Overhead Bytes:

- A1, A2 – These bytes are used for framing and to mark the beginning of a SONET frame. A1 has the value 0x F6 and A2 has the value 0x28.
- J0 -Section Trace Message – This byte carries the section trace message. The message is interpreted to verify connectivity to a particular node in the network.
- B1 - Section Bit Interleaved Parity (BIP-8) byte – This byte carries the parity information which is used to check for transmission errors in a section. The computed parity value is transmitted in the next frame in the B1 position. It is defined only for the first STS-1 of a STS-N signal. The other bytes have a default value of 0x00.

Figure 16. TX Frame Processor (TFP) Block Diagram



Payload Sub-block

The Payload sub block is activated by the cell mode frame pulse (cell mode) or DINxx_FP from FPGA (SONET mode). A pulse on this signal indicates the start of a frame.

In SONET mode, only two types of data bytes are in each frame:

- TOH bytes
- SPE data bytes

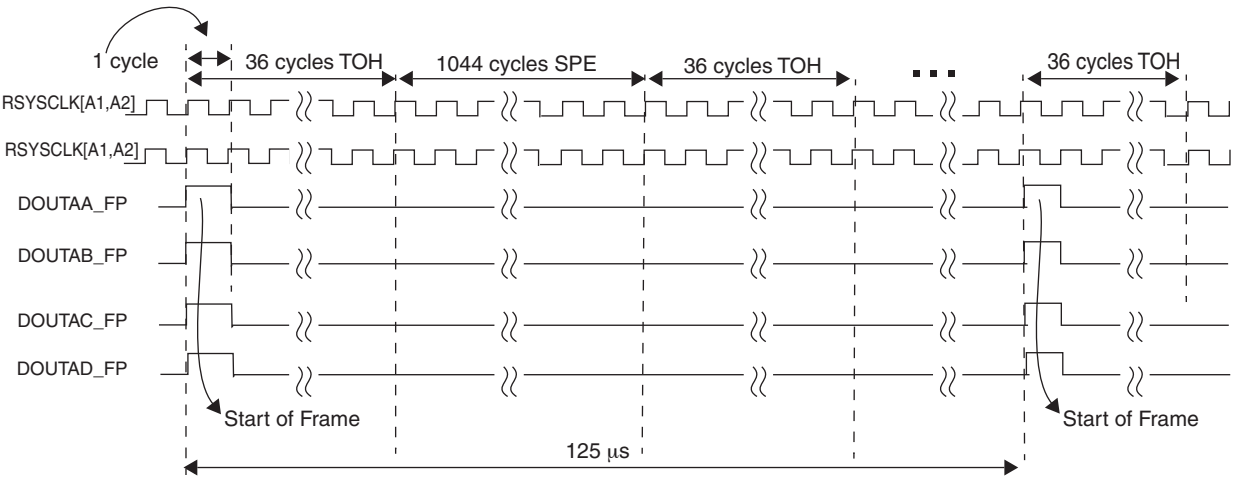
There are N x 3 (N = 48) bytes of TOH per row and there are a total of 9 rows in a SONET frame. The rest of the bytes in each row are SPE data bytes in SONET mode.

TOH Sub-block

This block is responsible formatting the 144 (48 x 3) bytes of TOH at the beginning of each row of the transport frame. All TOH bytes may be transmitted transparently from the FPGA logic using the transparent mode. Alternately, some or all TOH bytes may be inserted by the TOH block (AUTO_SOH and AUTO_TOH mode). The TOH data is transferred across the FPGA/core interface as 32-bit words, hence 36 clock cycles (12 x 3) are needed to transfer a TOH row. TOH insertion is controlled by software register bits as shown in the Register Map tables.

Figure 33 shows the SONET quad alignment mode in the ORSO82G5.

Figure 33. Receive Clocking Diagram for SONET Mode Quad Alignment – ORSO82G5

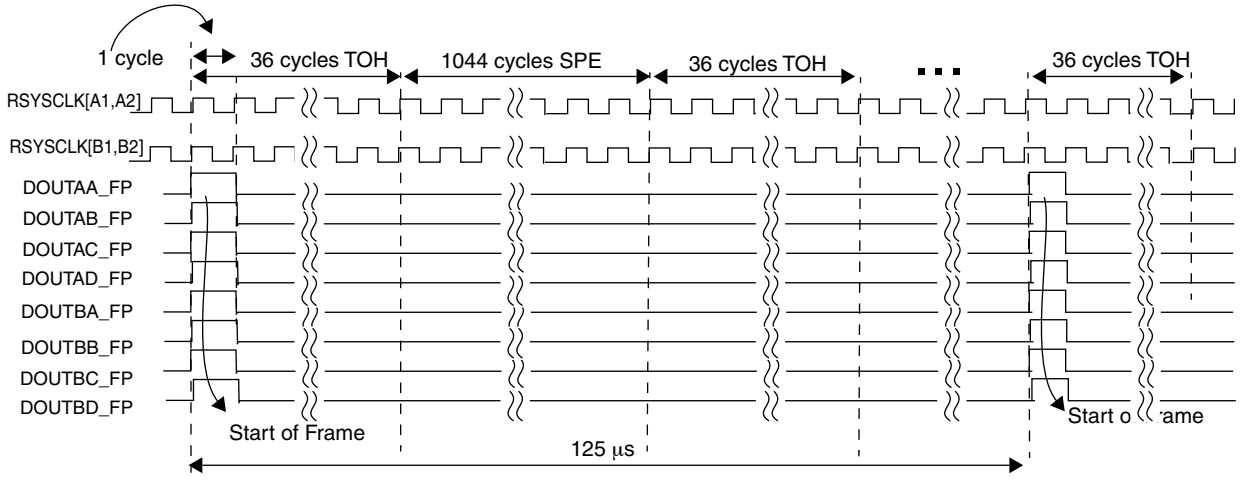


Clocks
RSYSCLKA1 and RSYSCLKA2 are sourced by RCK78A

- Only frame pulse (DOUTxx_FP) and clocks are shown for understanding of block alignment.
- Timing of data and SPE indicators are the same as shown for twin alignment.
- Block groups are Group A - AA,AB,AC,AD and Group B - BA,BB,BC,BD

Figure 34 shows the octal alignment mode in the ORSO82G5.

Figure 34. Receive SONET Mode—Octal Alignment Mode – ORSO82G5



Clocks
RSYSCLKA1, RSYSCLKA2, RSYSCLKB1, and RSYSYSCLKB2 are sourced by RCK78A

There is no way to tell where a cell starts unless one counts the cells from the beginning of the SPE. That means, there is no way to regain lost cell delineation other than wait for the next SONET frame.

Cell Mode Transmit Path

In the transmit path in cell mode, the transmit logic creates a SONET-like transport frame for the data, adds the required Transport OverHead bytes (cell mode automatically uses AUTO_TOH mode) and retimes the cell data from the FPGA interface rate of 156 MHz to the framer rate of 77.76 MHz. The data are then sent to the SONET logic blocks and SERDES. The Payload sub-block of the SONET logic operates somewhat differently than in SONET mode, however.

Output Port Controller

The ORSO42G5 has two link controllers (OPC2s). In cell mode the Output Port Controller (OPC) is the block responsible for directing traffic for the transmit traffic flow. There are four two-link controllers and one eight-link controller (OPC8) in the ORSO82G5. The user provides 160-bit data (OPC8) or 40-bit data (OPC2s) at 156 MHz, along with a cell valid strobe from the FPGA logic. No Link Header byte is sent with the cell data. The OPC provides the following functions:

- Accepts cell payload from the FPGA logic and assembles legal output cells from these.
- Inserts Bit Interleaved Parity (BIP)
- Schedules, manages and performs writes of cell data into TX FIFOs in the transmit framer blocks of all the eight-links or up to 4 pairs of two-links.
- Provides backpressure information to the FPGA to stop writes to the TXFIFO if the FIFO is not ready to accept data.

The OPC blocks, shown in Figure 39, operate as follows:

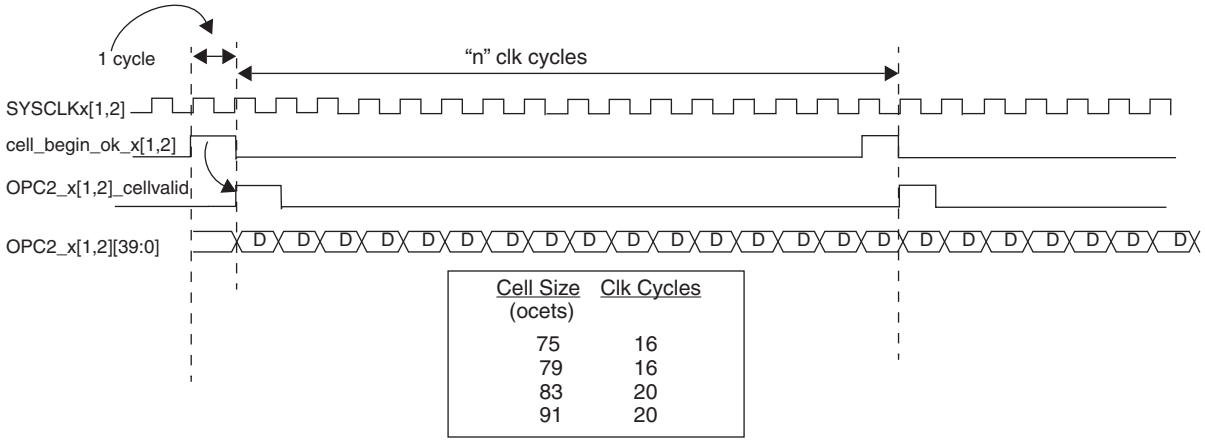
- OPC8 to stripe cells across eight links (ORSO82G5 only)
- OPC2_A1 to service links AA,AB (ORSO82G5 only)
- OPC2_A2 to service links AC,AD
- OPC2_B1 to service links BA,BB (ORSO82G5 only)
- OPC2_B2 to service links BC,BD

When operating with some links in the two-link cell mode, links not in an alignment group can optionally be operated in SONET and/or SERDES-only modes.

- If core FIFO cannot accept cells, cell_begin_ok will be low.
- If core FIFO is empty then cell_begin_ok will be asserted every 4 clock cycles until cellvalid is asserted by user to indicate valid cell data.

cellvalid: Clock-wide pulse asserted by user to indicate valid data. Asserted on the clock cycle following cell_begin_ok.

Figure 41. ORSO42G5 and ORSO82G5 Transmit FPGA Interface OPC2 Cell Mode



When operating in the eight-link cell mode, the OPC8 block passes user cells from FPGA to embedded core. Depending upon the configured CELL SIZE, cell transfers will take a variable number of SYSCLK156 cycles to be transmitted across the interface. Data are always transferred across a 160-bit bus (20 octets per clock cycle). Figure 42 shows five clock cycles for a cell transfer this corresponds to a user cell size of 91 octets. The two control signals in the figure are defined as:

sdo_bp_8: Backpressure signal from core instructing user to stop sending cell data. User should complete transmitting the current cell and can send one more cell before deasserting cellvalid.

cellvalid: Is high throughout a cell transfer to indicate valid cell data

Figure 42. ORSO82G5 Transmit FPGA Interface OPC8 Cell Mode

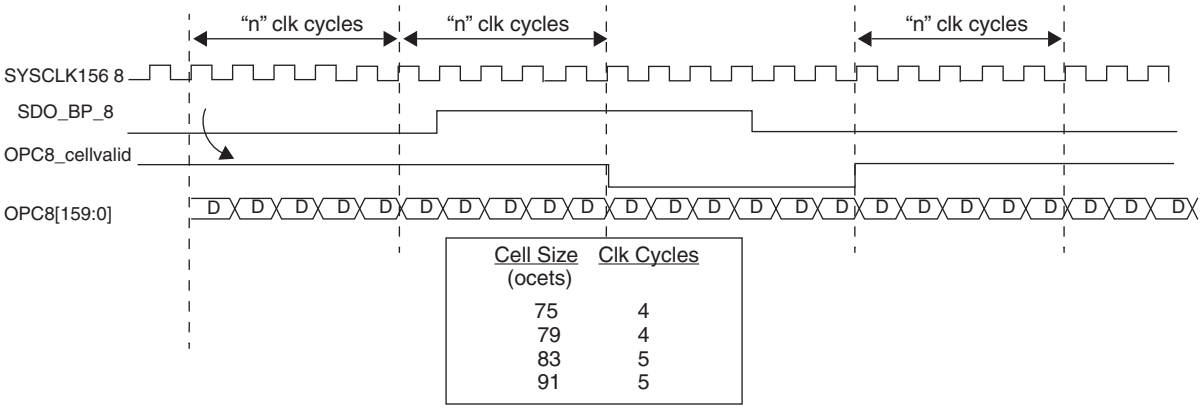


Table 13. RX Core/FPGA Interface Signals – ORSO42G5 (Continued)

33	—	
32	DOUTBD_B1_ERR	
[31:20]	DOUTBD[31:20]	—
[19:0]	DOUTBD[19:0]	IPC2_B2[19:0]

Signal Description for RX Path (SERDES Core to FPGA) – ORSO82G5

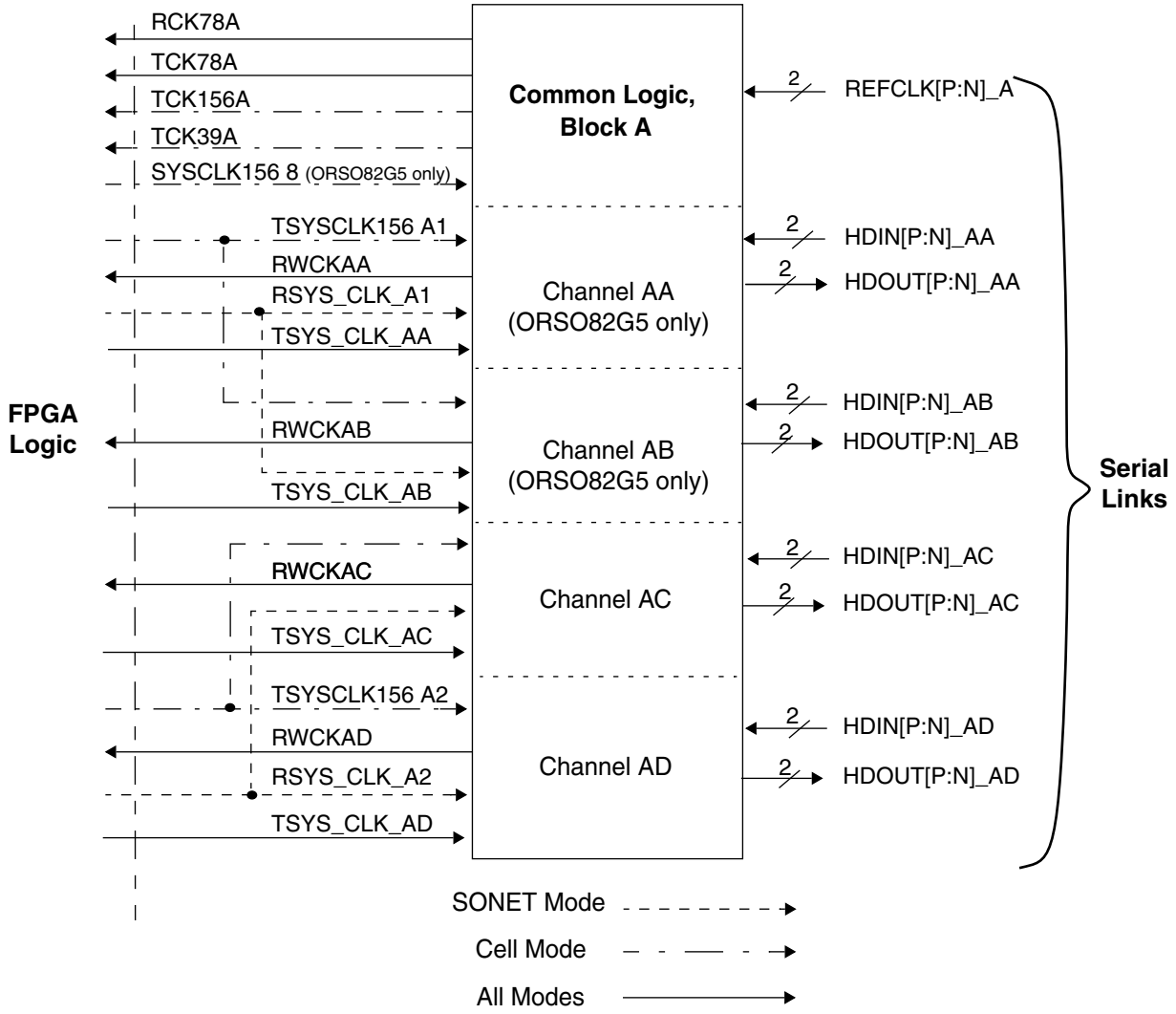
- Signals are divided across 8 channels with 40 signals per channel. RXDxx[39:0] is the set of 40 signals for a channel xx.
- All RX direction signals are outputs from the core.
- See Figure 47 for clock transfers across the FPGA/Core interface.
- In SONET mode, RXDxx[31:0] carries 32 bit data from the alignment FIFO of the respective channel. RXDxx[35:32] carries miscellaneous information such as OOF, BIPERR, Frame Pulse (FP), and SPE.
- In cell mode, data from each of the four 2-link IPC bundles are spread across all eight channels and are assigned to the 20 LSBs (RXDxx[19:0]) of each channel output. Data from IPC2_A1 is distributed across RXDAA[19:0] and RXDAB[19:0]. Data from IPC2_A2 is distributed across RXDAC[19:0] and RXDAD[19:0]. This symmetry is maintained for IPC2 data signals from block B.
- Data from the 8-link IPC block IPC8 is spread across all eight channels and assigned to the 20 LSB's (RXDxx[19:0] of each channel output.
- The IPC status signals for Cell Mode operation are contained in RXDxx[39:36] and RXDxx[33].
- The signals for SONET Mode operation are assigned to RXDxx[35:34] and RXDxx[33].
- Note that RXDxx[39:32] signal assignments are the same no matter what mode the RX blocks are in.

Table 14 summarizes the signals across the Core/FPGA interface in the receive direction.

Table 14. RX Core/FPGA Interface Signals – ORSO82G5

RXDAA[39:0]	SONET mode	IPC2 A1 Mode	IPC8 Mode
39	SYNC2_A1_OOS	—	
38	—	IPC2_A1_CELLDROP	—
37	—	IPC2_A1_CELLSTART	—
36	DOUTAA_FP	—	
35	DOUTAA_OOF		
34	DOUTAA_SPE	—	
33	—	IPC2_A1_CELL_BIP_ERR	—
32	DOUTAA_B1_ERR		
[31:20]	DOUTAA[31:20]	—	
[19:0]	DOUTAA[19:0]	IPC2_A1[39:20]	—
RXDAB[39:0]	SONET mode	IPC2 A1 Mode	IPC8 Mode
39	—	—	
38	SYNC4_A_OOS	—	
37	—	CELL_BEGIN_OK_A1	—
36	DOUTAB_FP	—	
35	DOUTAB_OOF		
34	DOUTAB_SPE	—	

Figure 47. ORSO42G5 and ORSO82G5 Clock Signals, Block A (High speed serial I/O also shown. Block B has the same signals, SYSCLK156 8 is unique to the ORSO82G5 and common to both blocks).



REFCLKP_[A:B], REFCLKN_[A:B]: These are the differential reference clocks provided to the ORSO42G5 and ORSO82G5 device as described earlier. They are used as the reference clock for both TX and RX paths. For operation of the serial links at 2.48 Gbps, the reference clocks will be at a frequency of 155.52 MHz.

RWCK[AA:BD]: These are the low-speed receive clocks from the embedded core to the FPGA across the core-FPGA interface. These are derived from the recovered low-speed complementary clocks from the SERDES blocks. RWCKAA belongs to Channel AA, RWCKAB belongs to channel AB and so on. With a reference clock input of 155.52 MHz, these clocks operate at 77.76 MHz.

RCK78[A:B]: These are muxed outputs of RWCKA[A:D] and RWCKB[B:D] respectively. With a reference clock input of 155.52 MHz, these clocks operate at 77.76 MHz.

RSYSCLK[A:B][1:2]: These clocks are inputs to the SERDES block A and B respectively from the FPGA. These are used by each channel as the read clock to read received data from the alignment FIFO within the embedded core. Clocks RSYSCLKA[1:2] are used by channels in the SERDES block A and RSYSCLKB[1:2] by channels in the SERDES block B. To guarantee that there is no overflow in the alignment FIFO, it is an absolute requirement that the write and read clocks be frequency locked within 0 ppm. Examples of how to achieve this are shown in the later section on recommended board-level clocking.

Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30826 - AC 30836 - AD 30926 - BC 30936 - BD	[0:5]	RSVD	00	Reserved	—
	[6]	AUTO_B1_xx		AUTO_B1_xx = 0, B1 is not inserted by the embedded core AUTO_B1_xx = 1, B1 is calculated and inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	Both
	[7]	AUTO_A1A2_xx		AUTO_A1A2_xx = 0, A1/A2 bytes are not inserted by the embedded core AUTO_A1A2_xx = 1, A1/A2 bytes inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	

Table 27. Per-Channel Status Register Descriptions – ORSO42G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
Channel Status Registers (Read Only) xx = [AC, AD, BC, BD]					
30828 - AC 30838 - AD 30928 - BC 30938 - BD	[0:4]	RSVD	00	Reserved	—
	[5]	CELL_ALIGN_ERR_xx		Cell Alignment Error, CELL_ALIGN_ERR = 1 indicates that the internal transmit frame processor did not detect a start of cell indicator when it was expecting a new cell. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[6]	TX_URUN_ERR_xx		Transmit Underrun Error, TX_URUN_ERR = 1 indicates an underrun error in the transmit Asynchronous FIFO. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[7]	TX_ORUN_ERR_xx		Transmit Overrun Error, TX_ORUN_ERR = 1 indicates an overrun error in the transmit Asynchronous FIFO. The TX FIFO is designed to not overflow since it sends backpressure signal to the FPGA when it cannot accept more cells. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
30829 - AC 30839 - AD 30929 - BC 30939 - BD	[0]	RSVD	00	Reserved	—
	[1]	OOF_xx		OOF_xx = 1 indicates OOF has been detected in this link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm	Both
	[2]	EX_SEQ_ERR_xx		Excessive Sequence Errors, EX_SEQ_ERR = 1 indicates that three consecutive cells containing sequence errors have been detected in this link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[3]	SEQ_ERR_xx		Sequence Error, SEQ_ERR = 1 indicates that a sequence error has been detected for a cell on this link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	]4]	CELL_BIP_ERR_xx		Cell mode BIP Error, CELL_BIP_ERR = 1 indicates that a BIP error has been detected in a cell on the link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[5]	B1_ERR_xx		Bit Interleaved Parity Error, B1_ERR = 1 indicates that a Section B1 error has been detected on the link.If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Both
	[6]	RX_FIFO_OVRUN_xx		Receive FIFO Overrun, RX_FIFO_OVRUN_xx = 1 indicates that the asynchronous RX FIFO has detected an overrun condition. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[7]	RDI_xx		Remote Defect Indication, RDI = 1 indicates that a RDI has been detected on the link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm	Both

Table 28. Common Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A03	[0]	NO_TX_RDI_EXSEQ	00	Not Transmission of RDI, If NO_TX_RDI_EXSEQ = 1, a transmit link will not send data if its corresponding receive link is not good due to excessive sequence errors. If this bit is set to 0, a transmit link will still send data even if its corresponding receive link has excessive sequence errors. This bit should always be set during simulation and in SONET mode.	Both
	[1]	AUTO_BUNDLE		Automatic (Link) Bundle, AUTO_BUNDLE = 1 allows a link within a link group to remain active even when another link within that group is defective. Cell data from all links within that group will continue to be sent to the FPGA. If this bit is set to 0, then all links within a link group must be good before cell data are read from the links by the IPC and passed to the FPGA.	Cell
	[2]	RSVD		Reserved	—
	[3]	REJOIN_A		Link Rejoin, REJOIN = 1 forces any link in a SERDES block to reassert a “RX link good” signal automatically when three consecutive sequence numbers are correct on that link.	Cell
	[4]	AUTO_REMOVE_A		Automatic (Link) Remove, AUTO_REMOVE = 1 indicates that any link in a SERDES block which sees three excessive sequence errors should deassert the “RX link good” signal which will cause the link to be inactive.	Cell
	[5]	RSVD		Reserved	
	[6]	REJOIN_B		Link Rejoin, REJOIN = 1 forces any link in a SERDES block to reassert a “RX link good” signal automatically when three consecutive sequence numbers are correct on that link.	Cell
	[7]	AUTO_REMOVE_B		AUTO_REMOVE_B = 1 indicates that any link in SERDES block B which sees three excessive sequence errors should deassert the “RX link good” signal which will cause the link to be inactive.	Cell
30A04	[0:1]	RSVD	00	Reserved	—
	[2]	FMPU_RESYNC2_B2		Control to resync channels BC and BD which have been configured for multi channel alignment in SONET mode in block B. Requires a rising edge on this bit. Write a 0 followed by a 1.	SONET
	[3:4]	RSVD		Reserve	SONET
	[5]	FMPU_RESYNC2_A2		Control to resync channels AC and AD which have been configured for multi channel alignment in SONET mode in block A. Requires a rising edge on this bit. Write a 0 followed by a 1.	SONET
	[6]	RSVD		Reserved	SONET
	[7]	FMPU_RESYNC4		Control to resync all four channels which have been configured for multi channel alignment.	SONET

Table 34. Per-Channel Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30803 - AA 30813 - AB 30823 - AC 30833 - AD 30903 - BA 30913 - BB 30923 - BC 30933 - BD	[0]	BYPASS_ALGN_FIFO_xx	00	Bypass alignment FIFO =1 in RX path in SONET mode. DOUT_xx data is clocked off RWCKxx.	SONET
	[1]	SERDES_ONLY_MODE_xx		SERDES-Only Mode. SERDES_ONLY_MODE =1 bypasses all the SONET and cell functions. Data is sent directly from the SERDES to the FPGA logic in the RX path and is passed directly from the FPGA logic to the SERDES in the TX path.	SERDES Only
	[2]	FORCE_B1_ERR_xx		Force B1 Error. FORCE_B1_ERR =1 forces a Section B1 error (Bit Interleaved Parity Error) in the TX path. Valid only when the corresponding AUTO_TOH_xx bit or AUTO_B1_xx bit is set to one.	Both
	[3]	FORCE_BIP8_ERR_xx		Force BIP8 Error, FORCE_BIP8_ERR =1 forces cell BIP8 error in the TX path.	Cell
	[4]	FORCE_A1A2_ERR_xx		Force A1A2 Error, FORCE_A1A2_ERR =1 forces an error in A1A2 bytes (framing error) in the TX path. Valid only when the corresponding AUTO_TOH_xx bit or AUTO_A1A2_xx bit is set to one.	Both
	[5]	FORCE_EX_SEQ_ERR_xx		Force Excessive Sequence Errors. FORCE_EXP_SEQ_ERR_xx = 1 forces sequence errors in the TX path by inverting the link header byte sequence number.	Cell
	[6]	FORCE_SEQ_ERR_xx		Force Sequence Error, FORCE_SEQ_ERR =1 forces one sequence error in the TX path. After this bit is set, the next Link Header byte's sequence number is inverted. The Link Header after the errored Link Header byte will have the correct sequence number	Cell
	[7]	FORCE_RDI_xx		Force Remote Defect Indication, FORCE_RDI =1 forces RDI errors in the TX path. The K2 byte in TOH is set to '00000110'. Valid only when AUTO_TOH_xx bit is set to 1.	Cell

Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A0B	[0:2]	RSVD	00	Reserved	—
	[3]	CELL_DRP_B2		Cell Drop, CELL_DRP_B2 = 1 indicates that a cell has been dropped from the link group BC and BD	Cell
	[4]	CELL_DRP_B1		Cell Drop, CELL_DRP_B1 = 1 indicates that a cell has been dropped from the link group BB and BA	Cell
	[5]	CELL_DRP_A2		Cell Drop, CELL_DRP_A2 = 1 indicates that a cell has been dropped from the link group AC and AD	Cell
	[6]	CELL_DRP_A1		Cell Drop, CELL_DRP_A1 = 1 indicates that a cell has been dropped from the link group AB and AA	Cell
	[7]	CELL_DRP_ALL8		CELL_DRP_ALL8 = 1 indicates that cells have been dropped on link group comprising of all 8 channels	Cell
30A0C	[0]	RSVD	00	Reserved	—
	[1]	SYNC4_B_OOS		SYNC4_B_OOS = 1 indicates that channels cannot be aligned within the 4 links in block B in SONET mode	SONET
	[2]	SYNC2_B2_OOS		SYNC2_B2_OOS = 1 indicates that channels cannot be aligned within the links BC and BD in SONET mode	SONET
	[3]	SYNC2_B1_OOS		SYNC2_B1_OOS = 1 indicates that channels cannot be aligned within the links BB and BA in SONET mode	SONET
	[4]	SYNC4_A_OOS		SYNC4_A_OOS = 1 indicates that channels cannot be aligned within the 4 links in block A in SONET mode	SONET
	[5]	SYNC2_A2_OOS		SYNC2_A2_OOS = 1 indicates that channels cannot be aligned within the AC and AD links in SONET mode	SONET
	[6]	SYNC2_A1_OOS		SYNC2_A1_OOS = 1 indicates that channels cannot be aligned within the AB and AD links in SONET mode	SONET
	[7]	SYNC8_OOS		SYNC8_OOS = 1 indicates that channels cannot be aligned within the 8 channels in SONET mode	SONET

High Speed Data Receiver

Table 43 specifies receiver parameters measured on devices with worst case process parameters and over the full range of operation conditions.

Table 43. External Data Input Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Data					
Stream of Nontransitions	Scrambler off	—		72	Bits
Sensitivity (differential), worst-case[1]	2.7Gbps	80		—	mVp-p
Input Levels[2]	—	V_{SS} - 0.3	—	V_{DD_ANA} + 0.3	V
Internal Buffer Resistance (Each input to VDDIB)	—	40	50	60	Ω
PLL Lock Time[3]	—	—	—	Note 2	—

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Input level min + (input peak to peak swing)/2 ≤ common mode input voltage ≤ input level max - (input peak to peak swing)/2
3. The ORT82G5 SERDES receiver performs four levels of synchronization on the incoming serial data stream, providing first bit, then byte (character), then channel (32-bit word), and finally optional multi-channel alignment as described in TN1025. The PLL Lock Time is the time required for the CDR PLL to lock to the transitions in the incoming high-speed serial data stream. If the PLL is unable to lock to the serial data stream, it instead locks to REFCLK to stabilize the voltage-controlled oscillator (VCO), and periodically switches back to the serial data stream to again attempt synchronization.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type. Table 44 shows receiver specifications with 10 MHz sinusoidal jitter injection. Other jitter tolerance measurements were measured in a separate experiment detailed in technical note TN1032, *SERDES Test Chip Jitter,* and are not reflected in these results.

Table 44. Receiver Sinusoidal Jitter Tolerance Specifications

Parameter	Conditions	Max.	Unit
Input Data			
Jitter Tolerance @ 2.7Gbps, Typical	600 mV diff eye[1]	0.75	UIP-P
Jitter Tolerance @ 2.7Gbps, Worst case	600 mV diff eye[1]	0.65	UIP-P
Jitter Tolerance @ 2.5Gbps,Typical	600 mV diff eye[1]	0.79	UIP-P
Jitter Tolerance @ 2.5Gbps, Worst case	600 mV diff eye[1]	0.67	UIP-P

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply. Jitter measured with a Wavecrest SIA-3000.

Table 47. Pin Descriptions (Continued)

Symbol	I/O	Description
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user programmable I/O, if not used for clock inputs.
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O if boundary scan is not used.[1]
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration this pin is a user-programmable I/O pin.[1]
HDC	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{LDC}}$	O	$\overline{\text{Low During Configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.[1]
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
$\overline{\text{WR}}$/MPI_RW	I	$\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{\text{WR}}$/MPI_RW is a user-programmable I/O pin.[1]
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the PowerPC bus master utilizing the least-significant bits of the PowerPC 32-bit address.
$\overline{\text{MPI\_BURST}}$	I	$\overline{\text{MPI\_BURST}}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.
$\overline{\text{MPI\_BDIP}}$	I	$\overline{\text{MPI\_BDIP}}$ is driven by the PowerPC processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	O	During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
D7	0 (TL)	—	VDDIO0	VDDIO0	—	—
C14	0 (TL)	1	IO	PT13B	—	L2C_A0
B14	0 (TL)	1	IO	PT13A	VREF_0_01	L2T_A0
A14	0 (TL)	1	IO	PT12D	M0	L3C_A0
A13	0 (TL)	1	IO	PT12C	M1	L3T_A0
AA20	—	—	Vss	Vss	—	—
E12	0 (TL)	2	IO	PT12B	MPI_CLK	L4C_A0
E13	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L4T_A0
C13	0 (TL)	2	IO	PT11D	M2	L5C_A0
C12	0 (TL)	2	IO	PT11C	M3	L5T_A0
B12	0 (TL)	2	IO	PT11B	VREF_0_02	L6C_A0
A12	0 (TL)	2	IO	PT11A	MPI_TEA_N	L6T_A0
D12	0 (TL)	3	IO	PT10D	—	L7C_D0
C11	0 (TL)	3	IO	PT10C	—	L7T_D0
B11	0 (TL)	3	IO	PT10B	—	—
A11	0 (TL)	3	IO	PT9D	VREF_0_03	L8C_A0
A10	0 (TL)	3	IO	PT9C	—	L8T_A0
AA21	—	—	Vss	Vss	—	—
B10	0 (TL)	3	IO	PT9B	—	—
E11	0 (TL)	3	IO	PT8D	D0	L9C_D0
D10	0 (TL)	3	IO	PT8C	TMS	L9T_D0
C10	0 (TL)	3	IO	PT8B	—	—
A9	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L10C_A0
B9	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L10T_A0
AA22	—	—	Vss	Vss	—	—
E10	0 (TL)	4	IO	PT7B	—	—
A8	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L11C_A0
B8	0 (TL)	4	IO	PT6C	D3	L11T_A0
D9	0 (TL)	4	IO	PT6B	VREF_0_04	L12C_D0
C8	0 (TL)	4	IO	PT6A	—	L12T_D0
E9	0 (TL)	5	IO	PT5D	D1	L13C_D0
D8	0 (TL)	5	IO	PT5C	D2	L13T_D0
AB13	—	—	Vss	Vss	—	—
A7	0 (TL)	5	IO	PT5B	—	L14C_A0
A6	0 (TL)	5	IO	PT5A	VREF_0_05	L14T_A0
C7	0 (TL)	5	IO	PT4D	TDI	L15C_D0
B6	0 (TL)	5	IO	PT4C	TCK	L15T_D0
E8	0 (TL)	5	IO	PT4B	—	L16C_A0
E7	0 (TL)	5	IO	PT4A	—	L16T_A0
A5	0 (TL)	6	IO	PT3D	—	L17C_A0
B5	0 (TL)	6	IO	PT3C	VREF_0_06	L17T_A0
AB14	—	—	Vss	Vss	—	—
C6	0 (TL)	6	IO	PT3B	—	L18C_A0
D6	0 (TL)	6	IO	PT3A	—	L18T_A0

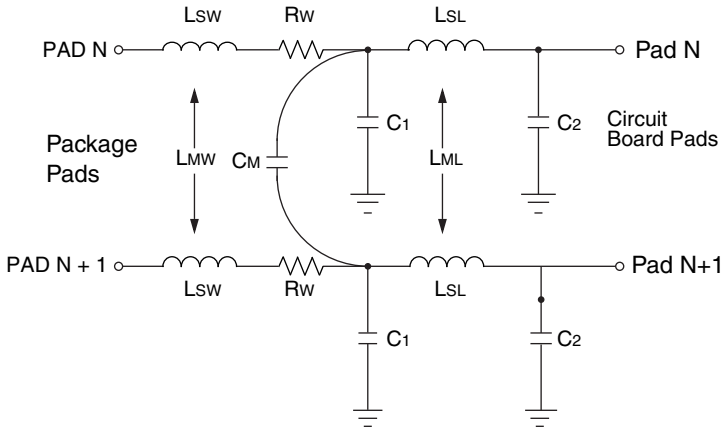
Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L19C_A0
B4	0 (TL)	6	IO	PT2C	PLL_CK1T/PPLL	L19T_A0
A4	0 (TL)	6	IO	PT2B	—	L20C_A0
A3	0 (TL)	6	IO	PT2A	—	L20T_A0
D5	—	—	O	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	—
E6	—	—	IO	PCCLK	CCLK	—
D4	—	—	IO	PDONE	DONE	—
E5	—	—	VDD33	VDD33	—	—
AB15	—	—	Vss	Vss	—	—
AL33	—	—	VDD15	VDD15	—	—
AL34	—	—	VDD15	VDD15	—	—
AM34	—	—	VDD15	VDD15	—	—
AN34	—	—	VDD15	VDD15	—	—
B34	—	—	VDD15	VDD15	—	—
C33	—	—	VDD15	VDD15	—	—
C34	—	—	VDD15	VDD15	—	—
D33	—	—	VDD15	VDD15	—	—
D34	—	—	VDD15	VDD15	—	—
E32	—	—	VDD15	VDD15	—	—
E33	—	—	VDD15	VDD15	—	—
F32	—	—	VDD15	VDD15	—	—
F34	—	—	VDD15	VDD15	—	—
N16	—	—	VDD15	VDD15	—	—
N17	—	—	VDD15	VDD15	—	—
N18	—	—	VDD15	VDD15	—	—
N19	—	—	VDD15	VDD15	—	—
P16	—	—	VDD15	VDD15	—	—
P17	—	—	VDD15	VDD15	—	—
P18	—	—	VDD15	VDD15	—	—
P19	—	—	VDD15	VDD15	—	—
R16	—	—	VDD15	VDD15	—	—
R17	—	—	VDD15	VDD15	—	—
R18	—	—	VDD15	VDD15	—	—
R19	—	—	VDD15	VDD15	—	—
T13	—	—	VDD15	VDD15	—	—
T14	—	—	VDD15	VDD15	—	—
T15	—	—	VDD15	VDD15	—	—
T20	—	—	VDD15	VDD15	—	—
T21	—	—	VDD15	VDD15	—	—
T22	—	—	VDD15	VDD15	—	—
U13	—	—	VDD15	VDD15	—	—
U14	—	—	VDD15	VDD15	—	—
U15	—	—	VDD15	VDD15	—	—
U20	—	—	VDD15	VDD15	—	—

Table 54. ORCA Typical Package Parasitics

L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
3.8	1.3	250	1.0	1.0	0.3	2.8-5	0.5 -1

Figure 53. Package Parasitics



Package Outline Drawings

Package Outline Drawings for the 484-ball PBGAM (fpBGA) used for the ORSO42G5 and 680-ball PBGAM (fpBGA) used for the ORSO82G5 are available at the Package Diagrams section of the Lattice Semiconductor web site at www.latticesemi.com.