Lattice Semiconductor Corporation - ORSO42G5-2BM484C Datasheet

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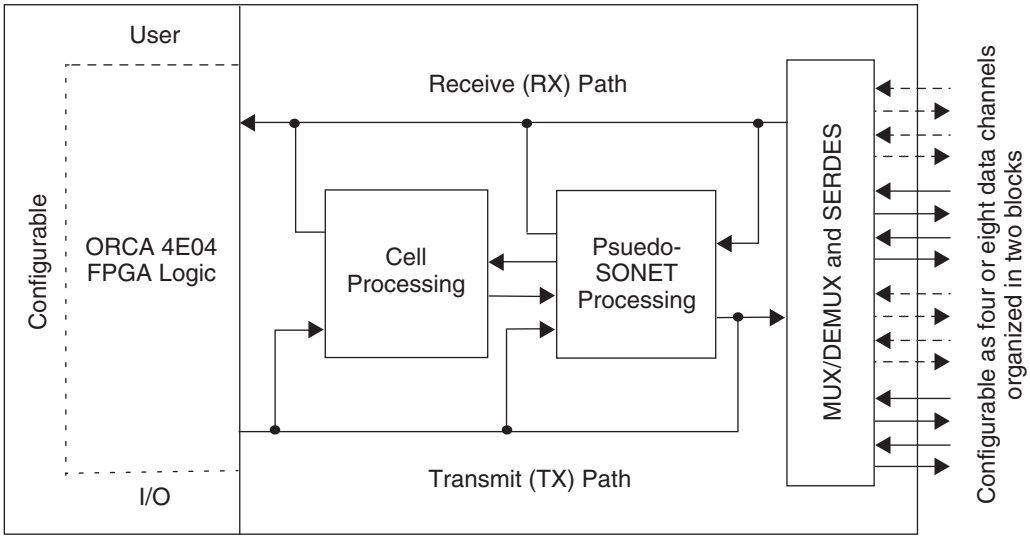
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso42g5-2bm484c

- Support for OC-48 and OC-192 (in block OC-48) formats.
- SONET framing, scrambling and SONET Mode channel alignment.
- Performance monitoring functions such as Bit Interleaved Parity (BIP-8) generation and checking and Out-Of-Frame (OOF) and Remote Defect Indication (RDI-L) detection.
- Cell Mode cell creation and extraction, idle cell insertion/deletion, destriping and striping functions.
- Additionally, there are two independent memory blocks in the core. Each embedded RAM block has a capacity of 4K words by 36 bits.

The ORSO42G5 and ORSO82G5 embedded cores contain, respectively, four-channel and eight-channel clock and data recovery macrocells and logical blocks performing functions such as SONET framing, scrambling/descrambling and cell processing. The channels each operate from 0.6 to 2.7 Gbps with per channel CDR functionality. The CDR interface enables high-speed asynchronous serial data transfer between system devices. Devices can be on the same PC-board, on separate boards connected across a backplane, or connected by cables. Figure 2 shows a top level block diagram of the backplane driver logic in the embedded core (embedded RAM not shown).

Figure 2. Top Level Block Diagram ORSO42G5 and ORSO82G5 Embedded Cores



ORSO42G5 and ORSO82G5 Main Operating Modes - Overview

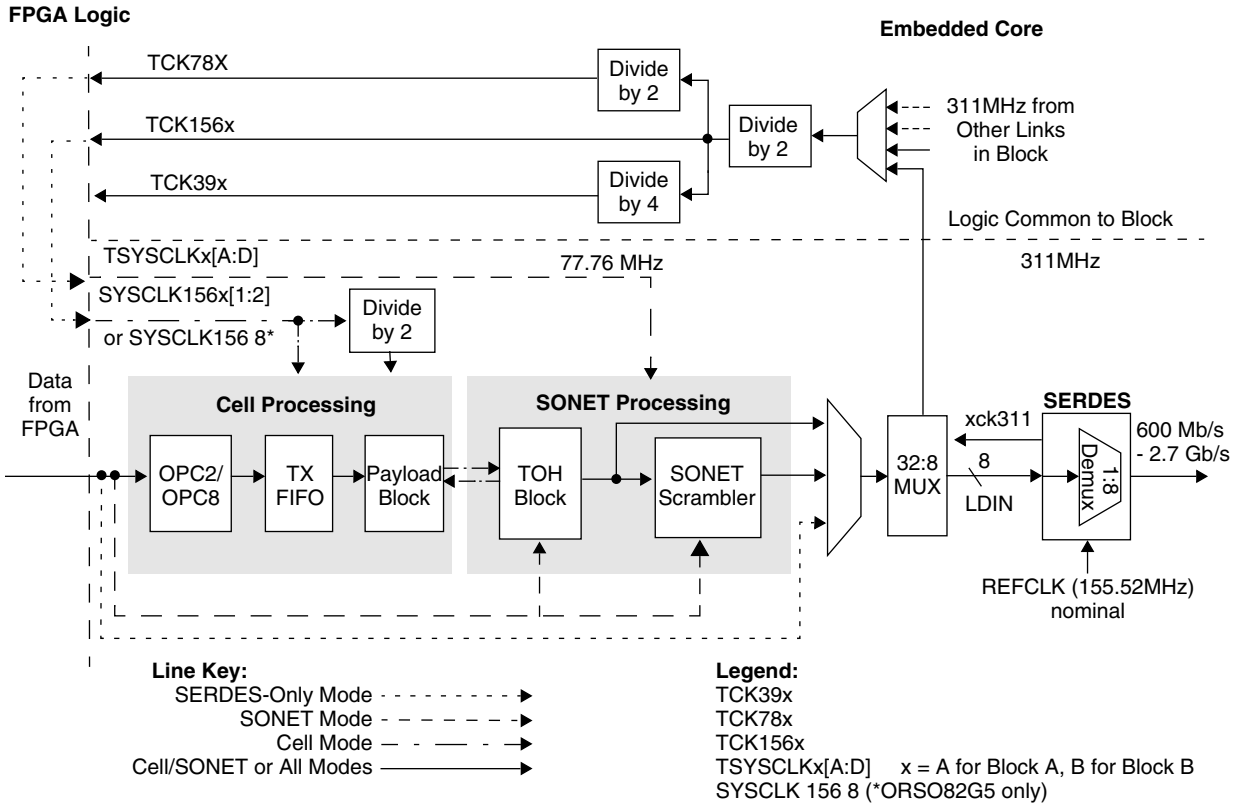
The ORSO42G5 and ORSO82G5 support four and eight 0.6 to 2.7 Gbps serial data channels respectively, which can operate independently or can be combined together (aligned) to achieve higher bit rates. The mode of operation of the core is defined by a set of control registers, which can be written through the system bus interface. The status of the core is stored in a set of status registers, which can be read through the system bus interface.

The serial data channels support OC-48 rates on each channel. The standard OC-48 rate, 2.488 Gbits, is used as the nominal data rate for the technical discussions that follow. OC-192 is also supported but is transmitted and received in block OC-48 links. The scrambled data stream conforms to the GR-255 specified polynomial sequence of $1+x^6+x^7$.

There are three main operating modes in the ORSO42G5 and ORSO82G5 as described below:

- SERDES only (bypass) mode
- SONET mode
- Cell mode
  - Two-link sub-mode
  - Eight-link sub-mode (ORSO82G5 only)

Figure 3. Top Level Overview, TX Path Logic, Single Channel



Receiver Architecture

The receiver section receives high-speed serial data at the external differential CML input pins. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. Therefore the receive clocks are asynchronous between channels. The data are then optionally framed, reformatted, aligned and passed to the FPGA logic in various parallel data formats.

The top level receiver architecture is shown in Figure 4. The main logical blocks in the receive path are:

- Receive SERDES and 8:32 DEMUX.
- SONET processing logic.
- Input Port Controllers (IPCs) which contain the cell processing logic.

Depending on the mode of operation, the FPGA to backplane data path may include or bypass the various logical blocks.

The receive PLL has two modes of operation as follows: lock to reference and lock to data with retiming. The control bit LCKREFN_xx selects the operating mode. When setup to lock to data and no data or invalid data are present on the HDINP and HDINN pins, the receive VCO will not lock to data and its frequency can drift outside of the nominal ±100 ppm range. Under this condition, the receive PLL will lock to REFCLK for a fixed time interval and then will attempt to lock to receive data. The process of attempting to lock to data, then locking to clock will repeat until valid input data exists. The default mode is lock to reference.

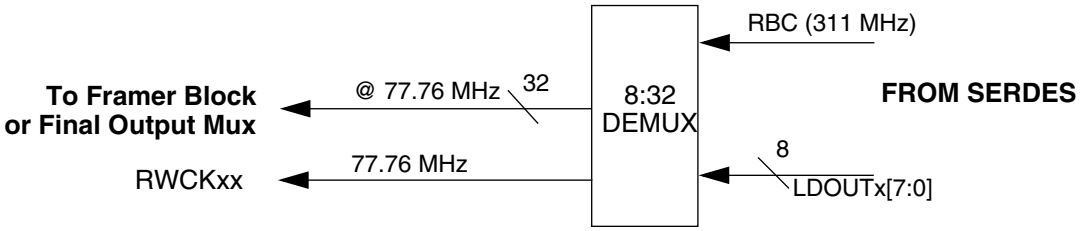
The recovered byte clock (RBC0) is only centered on the data when operating in the lock to data mode. In the lock to reference mode, RBC0 is not centered on the data and may not capture the correct byte value.

The SERDES receives MSB first and LSB last. Hence LDOUTx[7] is the bit that is received first and LDOUTx[0] is the bit that is received last.

8:32 DEMUX

The SERDES provides an eight bit data bus, and a clock, RBC0, which has a rising edge which occurs in the center of the valid data region. The DEMUX block will create one 32-bit data word from the single 8-bit bus. The DEMUX block will also provide a 77.76 MHz clock (divide-by-4 clock of RBC0) called RWCKxx to the rest of the logic blocks such as the framer, descrambler, cell extractor and FIFOs.

Figure 9. 8:32 DEMUX Block



In the DEMUX block, LDOUTx[7:0] is demultiplexed to a 32-bit data bus synchronous to the derived 77.76 MHz clock generated by dividing the 311.04 MHz clock by four. The 77.76 MHz clock is used by the remaining embedded blocks, as well as being fed to the FPGA. Receive data from the DEMUX block is unframed. Parallel data can be sent directly to the FPGA logic (SERDES only mode) or to the framer block for processing. Bit and byte alignment for the DEMUX block is shown in Figure 10.

Supported Data Formats

The ORSO42G5 and ORSO82G5 in the SONET mode support the following formats:

- Single OC-48 on each of the channels at a bit rate of 2.488 Gbps.
- OC-192 received in block OC-48 format on four channels at a combined rate of 9.952 Gbps.

The ORSO42G5 and ORSO82G5 SERDES will operate at the OC-12 rate of 622 MHz. For this rate, REFCLK is set to 77 MHz and the SERDES is used in half rate mode. However the embedded core SONET framing/processing logic is fixed at the OC-48 rate and therefore can not talk directly with standard STS-12 devices. In order to interoperate with standard STS-12 devices, the user must bypass the SONET functionality in the ORSO embedded core (SERDES-only mode) and implement all framing, TOH and scrambling/descrambling functionality in FPGA logic.

Figure 13 reveals the byte-ordering of the individual STS-48 streams. STS-192 is supported but it must be received in the block STS-48 format as shown in Figure 14. Each OC-48 stream is composed of byte-interleaved OC-1 data as described in GR-253 standard. Note that the SPE data is not touched by the core.

Figure 14. Byte Ordering of Input/Output Interface in STS-192 (Block STS-48) Mode

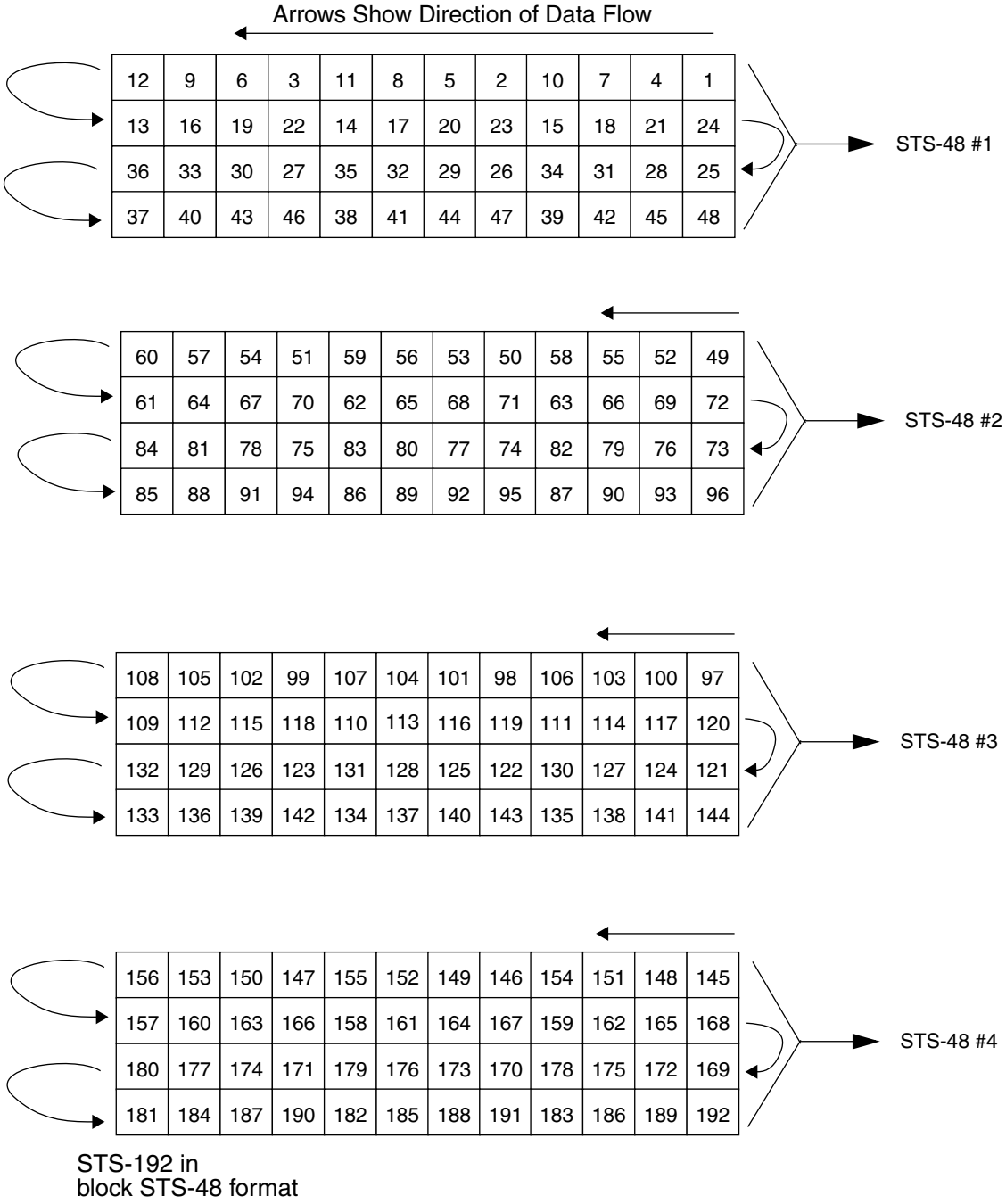
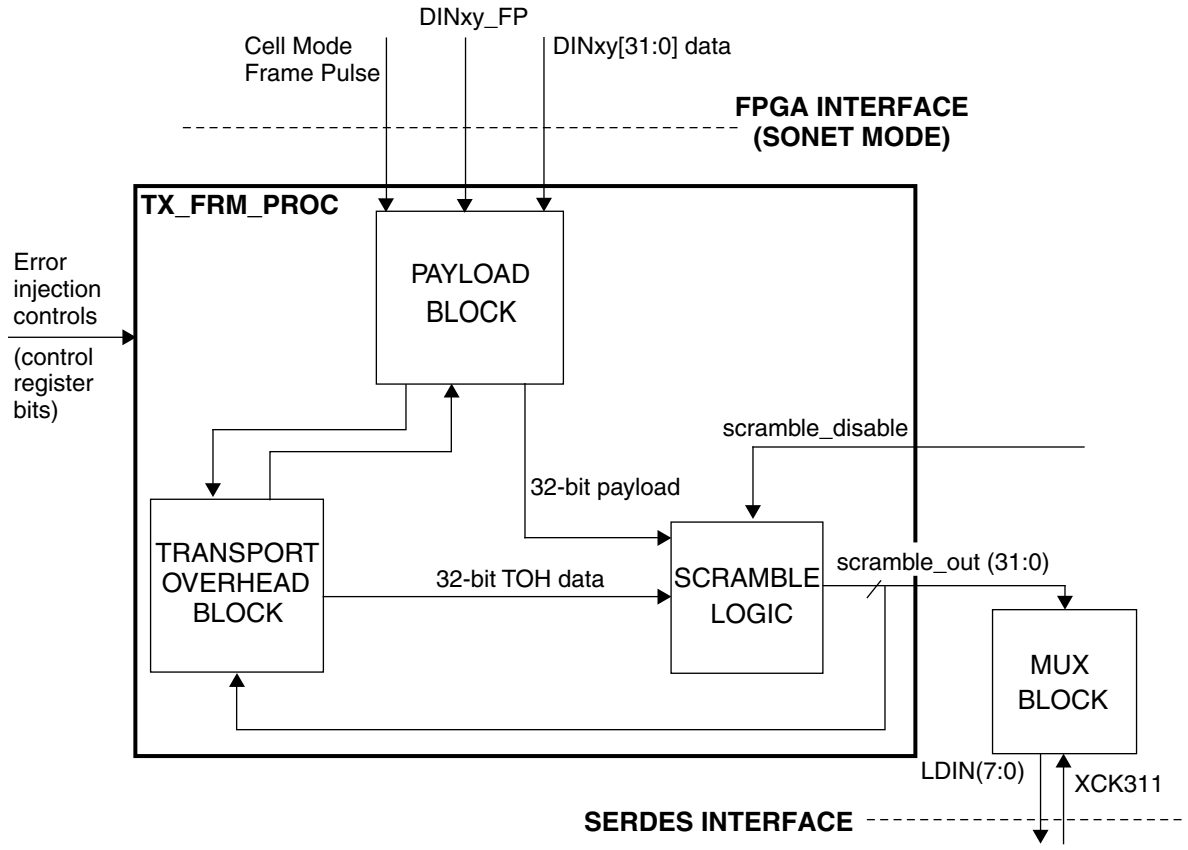


Figure 16. TX Frame Processor (TFP) Block Diagram



Payload Sub-block

The Payload sub block is activated by the cell mode frame pulse (cell mode) or DINxx_FP from FPGA (SONET mode). A pulse on this signal indicates the start of a frame.

In SONET mode, only two types of data bytes are in each frame:

- TOH bytes
- SPE data bytes

There are N x 3 (N = 48) bytes of TOH per row and there are a total of 9 rows in a SONET frame. The rest of the bytes in each row are SPE data bytes in SONET mode.

TOH Sub-block

This block is responsible formatting the 144 (48 x 3) bytes of TOH at the beginning of each row of the transport frame. All TOH bytes may be transmitted transparently from the FPGA logic using the transparent mode. Alternately, some or all TOH bytes may be inserted by the TOH block (AUTO_SOH and AUTO_TOH mode). The TOH data is transferred across the FPGA/core interface as 32-bit words, hence 36 clock cycles (12 x 3) are needed to transfer a TOH row. TOH insertion is controlled by software register bits as shown in the Register Map tables.

frame (or A1A2 framing bytes). This frame pulse is used to synchronize multiple channels within an alignment group.

If a channel is not in any alignment group, the FIFO control logic will set the FIFO-write-address to the beginning of the FIFO, and will set the FIFO-read-address to the middle of the FIFO at the first assertion of frame pulse after reset or after the resync command.

The RX_FIFO_MIN register bits can be used to control the threshold for minimum unused buffer space in the alignment FIFOs between read and write pointers before OVFL status is flagged. The synchronization algorithm consists of a down counter which starts to count down by 1 from its initial value of 18 (decimal) when a frame pulse from any channel within an alignment group has been received. The OOS alarm indicates the FIFO is out-of sync and the channel skew exceeds that which can be handled by the FIFO. Once the frame pulse for all channels within the alignment group have been received, the count is decremented by 2 until 0 is reached. Data are then read from the FIFOs and output to the SPE generator before being sent to the FPGA.

For every alignment group, there is an OVFL and OOS status register bit. The OOS bit is flagged when the down counter in the synchronization algorithm has reached a value of 0 and frame pulse from all channels within an alignment group have not been received. The OVFL bit is flagged when the read address at the time of receiving a frame pulse, is less than the minimum threshold set by RX_FIFO_MIN. In the memory map section OOS is referred to as SYNC[2,4]_[A1,A2,B1,B2]_OOS, SYNC8_OOS. OVFL is referred to as SYNC[2,4]_[A1,A2,B1,B2]_OVFL, SYNC8_OVFL.

Receive Clocking for Multi-channel Alignment – ORSO82G5

There are a total of nine clocks for the receive path, from FPGA to the core. The four used in SONET mode are RSYSCLKA1 and RSYSCLKA2 (both for block A), and RSYSCLKB1 and RSYSCLKB2 (both for block B). The following diagrams show the recommended clock distribution approaches for SONET mode multi-channel alignment modes. Cell mode alignment is discussed in the section describing the Input Port Controller (IPC).)

SONET Mode Twin Alignment

Figure 27 describes the clocking scheme for twin alignment in the ORSO82G5. In twin alignment, the valid channel pairs are AA,AB and AC,AD in block A and BA,BB and BC,BD in block B. The figure provides the clocking scheme for block A as an example. RSYSCLKA1 should be sourced from RWCKAA or RWCKAB. RSYSCLKA2 should be sourced from RWCKAC or RWCKAD. This clocking approach provides the required 0 ppm clock frequency matching for each pair and provides flexibility in applications where the two pairs in the block are received from asynchronous sources or operate at different rates.

ORSO42G5 Configuration

At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

- Setting bit 1 to one in registers at locations 30002, 30012, 30102 and 30112 powers down the legacy logic. (Note that the reset value for these bits is 0.)
- Setting bit 1 to zero (reset condition) in the register at locations 30802, 30812, 30902 and 30912 removes the legacy logic from any alignment group.

Register settings for SONET multi-channel alignment are shown in Table 7.

Table 7. Multichannel Alignment Modes – ORSO42G5

Register Bits FMPU_SYNMODE_xx[2:3]	Mode
00	No multichannel alignment
01	Twin channel alignment
11	Four channel alignment

Note: xx = [AC,AD,BC,BD]

To align two channels in SERDES A:

- FMPU_SYNMODE_AC = 01 (Register Location 30822)
- FMPU_SYNMODE_AD = 01 (Register Location 30832)

To align two channels in SERDES B:

- FMPU_SYNMODE_BC = 01 (Register Location 30922)
- FMPU_SYNMODE_BD = 01 (Register Location 30932)

To align all four channels:

- FMPU_SYNMODE_AC = 11 (Register Location 30822)
- FMPU_SYNMODE_AD = 11 (Register Location 30832)
- FMPU_SYNMODE_BC = 11 (Register Location 30922)
- FMPU_SYNMODE_BD = 11 (Register Location 30932)

To enable/disable multi-channel alignment of individual channels within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled

where xx = [AC,AD,BC,BD]

To resynchronize a multichannel alignment group set the following bits to one, and then set to zero:

- FMPU_RESYNC4 for four channels, AC, AD, BC and BD. (Register Location 30A04, bit 7)
- FMPU_RESYNCA2 for dual channels, AC and AD. (Register Location 30A04, bit 2)
- FMPU_RESYNCB2 for dual channels, BC and BD. (Register Location 30A04, bit 5)

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bits to one, and then set to zero.

- FMPU_RESYNC1_xx (Register Locations 30824, 20834, 30924 and 30934, bit 7) where xx is one of AC, AD, BC or BD.

Alignment Mode Setup Procedures – ORSO82G5
The control register bits for alignment FIFO in the ORSO42G5 and ORSO82G5 are described below.

Table 8. Multichannel Alignment Modes – ORSO82G5

Register Bits FMPU_SYNMODE_xx	Mode
00	No multichannel alignment. (default)
01	Twin channel alignment
10	Block channel alignment
11	Eight channel alignment

Note: Where xx is one of A[A:D] and B[A:D].

To align all eight channels:

- FMPU_SYNMODE_A[A:D] = 11
- FMPU_SYNMODE_B[A:D] = 11

To align twin channels in SERDES A:

- FMPU_SYNMODE_A[A:D] = 01

To align four channels in SERDES A:

- FMPU_SYNMODE_AB = 10
- FMPU_SYNMODE_AD = 10

Similar alignment can be defined for SERDES B. To enable/disable synchronization signal of individual channel within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled
  where xx is one of A[A:D] and B[A:D].

To re-synchronize a multi-channel alignment group
Set the following bit to zero, and then set it to 1 since it is a rising edge sensitive bit.

- FMPU_RESYNC8 for eight channel A[A:D] and B[A:D]
- FMPU_RESYNC4A for block channel A[A:D]
- FMPU_RESYNC2A1 for twin channel A[A:B]
- FMPU_RESYNC2A2 for twin channel A[C:D]
- FMPU_RESYNC4B for block channel B[A:D]

Re-synchronization will cause the multi-channel alignment group to perform a new synchronization procedure. This would need to occur if a link is removed from an alignment group and then paced back into service as part of the alignment group. This is not required at power up if the alignment mode is set before the channels receive the first frame pulse.

Table 28. Common Control Register Descriptions – ORSO42G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A00	[0:1]	RCKSELB	00	“10” - Channel BC source for clock RCK78B “11” - Channel BD source for clock RCK78B	Both
	[2:3]	TCKSELB		“10” - Channel BC source for clock TCK78B “11” - Channel BD source for clock TCK78B	Both
	[4:5]	RCKSELA		“10” - Channel AC source for clock RCK78A “11” - Channel AD source for clock RCK78A	Both
	[6:7]	TCKSELA		“10” - Channel AC source for clock TCK78A “11” - Channel AD source for clock TCK78A	Both
30A01	[0:2]	CELL_SIZE	00	Cell Size, Three bits to set cell size. “000” - Cell size is 75 bytes, “001” - Cell size is 79 bytes, “010” - Cell size is 83 bytes, “011” - Cell size is 91 bytes These are the only supported cell sizes.	Cell
	[3:7]	RX_FIFO_MIN		Set Minimum threshold value for alignment FIFO in SONET mode. When the read address for the FIFO is below this value at the time when write address is zero, it indicates that the FIFO is near overflow. This event will go high only once during a frame when a framing byte has been detected by the aligner. The default threshold value is “00000”.	SONET
30A02	0	TX_DISABLE_ON_RDI	00	Transmitter Disable on RDI (Detection), If TX_DISABLE_ON_RDI = 1 - No cell data is transmitted on a link in which a RDI has been detected by the corresponding link’s receiver. If this bit is set to 0, cell data will be transmitted on a link irrespective of detection of a RDI.	Cell
	[1:7]	RSVD		Reserved	—

Table 28. Common Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A03	[0]	NO_TX_RDI_EXSEQ	00	Not Transmission of RDI, If NO_TX_RDI_EXSEQ = 1, a transmit link will not send data if its corresponding receive link is not good due to excessive sequence errors. If this bit is set to 0, a transmit link will still send data even if its corresponding receive link has excessive sequence errors. This bit should always be set during simulation and in SONET mode.	Both
	[1]	AUTO_BUNDLE		Automatic (Link) Bundle, AUTO_BUNDLE = 1 allows a link within a link group to remain active even when another link within that group is defective. Cell data from all links within that group will continue to be sent to the FPGA. If this bit is set to 0, then all links within a link group must be good before cell data are read from the links by the IPC and passed to the FPGA.	Cell
	[2]	RSVD		Reserved	—
	[3]	REJOIN_A		Link Rejoin, REJOIN = 1 forces any link in a SERDES block to reassert a “RX link good” signal automatically when three consecutive sequence numbers are correct on that link.	Cell
	[4]	AUTO_REMOVE_A		Automatic (Link) Remove, AUTO_REMOVE = 1 indicates that any link in a SERDES block which sees three excessive sequence errors should deassert the “RX link good” signal which will cause the link to be inactive.	Cell
	[5]	RSVD		Reserved	
	[6]	REJOIN_B		Link Rejoin, REJOIN = 1 forces any link in a SERDES block to reassert a “RX link good” signal automatically when three consecutive sequence numbers are correct on that link.	Cell
	[7]	AUTO_REMOVE_B		AUTO_REMOVE_B = 1 indicates that any link in SERDES block B which sees three excessive sequence errors should deassert the “RX link good” signal which will cause the link to be inactive.	Cell
30A04	[0:1]	RSVD	00	Reserved	—
	[2]	FMPU_RESYNC2_B2		Control to resync channels BC and BD which have been configured for multi channel alignment in SONET mode in block B. Requires a rising edge on this bit. Write a 0 followed by a 1.	SONET
	[3:4]	RSVD		Reserve	SONET
	[5]	FMPU_RESYNC2_A2		Control to resync channels AC and AD which have been configured for multi channel alignment in SONET mode in block A. Requires a rising edge on this bit. Write a 0 followed by a 1.	SONET
	[6]	RSVD		Reserved	SONET
	[7]	FMPU_RESYNC4		Control to resync all four channels which have been configured for multi channel alignment.	SONET

Table 34. Per-Channel Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30806 - AA 30816 - AB 30826 - AC 30836 - AD 30906 - BA 30916 - BB 30926 - BC 30936 - BD	[0:5]	RSVD	00	Reserved	—
	[6]	AUTO_B1_xx		AUTO_B1_xx = 0, B1 is not inserted by the embedded core AUTO_B1_xx = 1, B1 is calculated and inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	Both
	[7]	AUTO_A1A2_xx		AUTO_A1A2_xx = 0, A1/A2 bytes are not inserted by the embedded core AUTO_A1A2_xx = 1, A1/A2 bytes inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	

Table 35. Per-Channel Status Register Descriptions – ORSO82G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
Channel Status Registers (Read Only) xx = [AA,...,BD]					
30808 - AA 30818 - AB 30828 - AC 30838 - AD 30908 - BA 30918 - BB 30928 - BC 30938 - BD	[0:4]	RSVD	00	Reserved	—
	[5]	CELL_ALIGN_ERR_xx		Cell Alignment Error, CELL_ALIGN_ERR = 1 indicates that the internal transmit frame processor did not detect a start of cell indicator when it was expecting a new cell. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[6]	TX_URUN_ERR_xx		Transmit Underrun Error, TX_URUN_ERR = 1 indicates an underrun error in the transmit Asynchronous FIFO. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[7]	TX_ORUN_ERR_xx		Transmit Overrun Error, TX_ORUN_ERR = 1 indicates an overrun error in the transmit Asynchronous FIFO. The TX FIFO is designed to not overflow since it sends backpressure signal to the FPGA when it cannot accept more cells. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell

Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A0D	[0]	RSVD	00	Reserved	—
	[1]	SYNC4_B_OVFL		SYNC8_OOS = 1 indicates that the alignment FIFO(s) in the links in block B are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[2]	SYNC2_B2_OVFL		SYNC2_B2_OVFL = 1 indicates that the alignment FIFO(s) in the links BC and BD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[3]	SYNC2_B1_OVFL		SYNC2_B1_OVFL = 1 indicates that the alignment FIFO(s) in the links BA and BB are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[4]	SYNC4_A_OVFL		SYNC4_A_OVFL = 1 indicates that the alignment FIFO(s) in the links in block A are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[5]	SYNC2_A2_OVFL		SYNC2_A2_OVFL = 1 indicates that the alignment FIFO(s) in the links AC and AD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[6]	SYNC2_A1_OVFL		SYNC2_A1_OVFL = 1 indicates that the alignment FIFO(s) in the links AA and AB are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[7]	SYNC8_OVFL		SYNC8_OVFL = 1 Indicates that the alignment FIFO(s) in eight-links are near overflow (At the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
30A0E	[0:2]	RSVD	00	Reserved	—
	[3]	BDL_ALIGN_ERR_B2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs BC and BD	Cell
	[4]	BDL_ALIGN_ERR_B1		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs BA and BB	Cell
	[5]	BDL_ALIGN_ERR_A2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs AC and AD	Cell
	[6]	BDL_ALIGN_ERR_A1		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs AA and AB	Cell
	[7]	BDL_ALIGN_ERR_ALL8		BDL_ALIGN_ERR_ALL8 = 1 -indicates that an alignment error has occurred in cell group of all eight-links	Cell

Table 47. Pin Descriptions (Continued)

Symbol	I/O	Description
MPI_ACK	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_CLK	I	This is the PowerPC synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the Embedded System Bus. If MPI is used this will be the AMBA bus clock.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_TEA	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_RTRY	O	This pin requests the MPC860 to relinquish the bus and retry the cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
D[0:31]	I/O	Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	O	D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.[1]
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.[1]
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.[1]
TESTCFG (ORSO82G5 only)	I	During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user programmable I/O pin.[1]

1. The FPGA States of Operation section in the ORCA Series 4 FPGAs data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
P17	-	-	VDD_ANA	VDD_ANA	-	-
G20	-	-	VDDIB	VDDIB_AC	-	-
P18	-	-	VDD_ANA	VDD_ANA	-	-
P19	-	-	VDD_ANA	VDD_ANA	-	-
T17	-	-	VDD_ANA	VDD_ANA	-	-
T18	-	-	VDD_ANA	VDD_ANA	-	-
R17	-	-	VSS	VSS	-	-
G21	-	-	I	REFCLKP_A	-	HSP_10
G22	-	-	I	REFCLKN_A	-	HSN_10
F21	-	-	O	REXTN_A	-	-
F22	-	-	O	REXT_A	-	-
U18	-	-	VDD_ANA	VDD_ANA	-	-
E21	-	-	VDDGB_A	VDDGB_A	-	-
E22	-	-	VSS	VSS	-	-
D21	-	-	O	PSYS_RSSIG_ALL	-	-
D22	-	-	I	PSYS_DOBISTN	-	-
D20	-	-	VDD33	VDD33	-	-
K15	-	-	VDD15	VDD15	-	-
K10	-	-	VSS	VSS	-	-
L7	-	-	VDD15	VDD15	-	-
D19	-	-	I	PBIST_TEST_ENN	-	-
D18	-	-	I	PLOOP_TEST_ENN	-	-
L15	-	-	VDD15	VDD15	-	-
E17	-	-	I	PASB_PDN	-	-
K11	-	-	VSS	VSS	-	-
D17	-	-	VDD33	VDD33	-	-
M7	-	-	VDD15	VDD15	-	-
C21	-	-	I	PASB_RESETN	-	-
C22	-	-	I	PASB_TRISTN	-	-
K12	-	-	VSS	VSS	-	-
E16	-	-	I	PASB_TESTCLK	-	-
M15	-	-	VDD15	VDD15	-	-
C17	-	-	VDD33	VDD33	-	-
D16	1 (TC)	7	IO	PT36D	-	-
C16	1 (TC)	7	IO	PT36B	-	-
F14	1 (TC)	7	IO	PT35D	-	-
F15	1 (TC)	7	IO	PT35B	-	-
E14	1 (TC)	7	IO	PT34D	VREF_1_07	-
E15	1 (TC)	8	IO	PT34B	-	-
D15	1 (TC)	8	IO	PT33D	-	L53C
C15	1 (TC)	8	IO	PT33C	VREF_1_08	L53T
E12	1 (TC)	-	VDDIO1	VDDIO1	-	-
C18	1 (TC)	8	IO	PT32D	-	L54C
C19	1 (TC)	8	IO	PT32C	-	L54T

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
M10	-	-	VSS	VSS	-	-
M11	-	-	VSS	VSS	-	-
M12	-	-	VSS	VSS	-	-
M13	-	-	VSS	VSS	-	-
M14	-	-	VSS	VSS	-	-
N8	-	-	VSS	VSS	-	-
N9	-	-	VSS	VSS	-	-
N10	-	-	VSS	VSS	-	-
N11	-	-	VSS	VSS	-	-
N12	-	-	VSS	VSS	-	-
N13	-	-	VSS	VSS	-	-
N14	-	-	VSS	VSS	-	-
P7	-	-	VSS	VSS	-	-
P8	-	-	VSS	VSS	-	-
P9	-	-	VSS	VSS	-	-
P10	-	-	VSS	VSS	-	-
P11	-	-	VSS	VSS	-	-
P12	-	-	VSS	VSS	-	-
P13	-	-	VSS	VSS	-	-
P14	-	-	VSS	VSS	-	-
R7	-	-	VSS	VSS	-	-
R8	-	-	VSS	VSS	-	-
R9	-	-	VSS	VSS	-	-
R10	-	-	VSS	VSS	-	-
R11	-	-	VSS	VSS	-	-
R12	-	-	VSS	VSS	-	-
R13	-	-	VSS	VSS	-	-
R14	-	-	VSS	VSS	-	-
AA1	-	-	VSS	VSS	-	-
AA19	-	-	VSS	VSS	-	-
AA20	-	-	VSS	VSS	-	-
AA21	-	-	VSS	VSS	-	-
AA22	-	-	VSS	VSS	-	-
AB1	-	-	VSS	VSS	-	-
AB19	-	-	VSS	VSS	-	-
AB20	-	-	VSS	VSS	-	-
AB21	-	-	VSS	VSS	-	-
AB22	-	-	VSS	VSS	-	-

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
W31	—	—	VSS	VSS	—	—
V30	—	—	VDDOB	VDDOB_BD	—	—
W33	—	—	O	HDOUTN_BD	—	—
H33	—	—	VSS	VSS	—	—
W34	—	—	O	HDOUTP_BD	—	—
V31	—	—	VDDOB	VDDOB_BD	—	—
H34	—	—	VSS	VSS	—	—
J32	—	—	VSS	VSS	—	—
U31	—	—	VDDOB	VDDOB_AD	—	—
T34	—	—	O	HDOUTP_AD	—	—
M32	—	—	VSS	VSS	—	—
T33	—	—	O	HDOUTN_AD	—	—
U30	—	—	VDDOB	VDDOB_AD	—	—
T31	—	—	VSS	VSS	—	—
R34	—	—	I	HDINP_AD	—	—
N32	—	—	VSS	VSS	—	—
R33	—	—	I	HDINN_AD	—	—
T30	—	—	VDDIB	VDDIB_AD	—	—
U32	—	—	VSS	VSS	—	—
R31	—	—	VDDOB	VDDOB_AC	—	—
P34	—	—	O	HDOUTP_AC	—	—
U33	—	—	VSS	VSS	—	—
P33	—	—	O	HDOUTN_AC	—	—
R30	—	—	VDDOB	VDDOB_AC	—	—
P31	—	—	VSS	VSS	—	—
N34	—	—	I	HDINP_AC	—	—
U34	—	—	VSS	VSS	—	—
N33	—	—	I	HDINN_AC	—	—
P30	—	—	VDDIB	VDDIB_AC	—	—
V32	—	—	VSS	VSS	—	—
M34	—	—	O	HDOUTP_AB	—	—
V33	—	—	VSS	VSS	—	—
M33	—	—	O	HDOUTN_AB	—	—
N31	—	—	VDDOB	VDDOB_AB	—	—
M31	—	—	VSS	VSS	—	—
L34	—	—	I	HDINP_AB	—	—
V34	—	—	VSS	VSS	—	—
L33	—	—	I	HDINN_AB	—	—
N30	—	—	VDDIB	VDDIB_AB	—	—
K34	—	—	O	HDOUTP_AA	—	—
K33	—	—	O	HDOUTN_AA	—	—
M30	—	—	VDDOB	VDDOB_AA	—	—
L32	—	—	VDD_ANA	VDD_ANA	—	—
L31	—	—	VSS	VSS	—	—

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
D7	0 (TL)	—	VDDIO0	VDDIO0	—	—
C14	0 (TL)	1	IO	PT13B	—	L2C_A0
B14	0 (TL)	1	IO	PT13A	VREF_0_01	L2T_A0
A14	0 (TL)	1	IO	PT12D	M0	L3C_A0
A13	0 (TL)	1	IO	PT12C	M1	L3T_A0
AA20	—	—	Vss	Vss	—	—
E12	0 (TL)	2	IO	PT12B	MPI_CLK	L4C_A0
E13	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L4T_A0
C13	0 (TL)	2	IO	PT11D	M2	L5C_A0
C12	0 (TL)	2	IO	PT11C	M3	L5T_A0
B12	0 (TL)	2	IO	PT11B	VREF_0_02	L6C_A0
A12	0 (TL)	2	IO	PT11A	MPI_TEA_N	L6T_A0
D12	0 (TL)	3	IO	PT10D	—	L7C_D0
C11	0 (TL)	3	IO	PT10C	—	L7T_D0
B11	0 (TL)	3	IO	PT10B	—	—
A11	0 (TL)	3	IO	PT9D	VREF_0_03	L8C_A0
A10	0 (TL)	3	IO	PT9C	—	L8T_A0
AA21	—	—	Vss	Vss	—	—
B10	0 (TL)	3	IO	PT9B	—	—
E11	0 (TL)	3	IO	PT8D	D0	L9C_D0
D10	0 (TL)	3	IO	PT8C	TMS	L9T_D0
C10	0 (TL)	3	IO	PT8B	—	—
A9	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L10C_A0
B9	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L10T_A0
AA22	—	—	Vss	Vss	—	—
E10	0 (TL)	4	IO	PT7B	—	—
A8	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L11C_A0
B8	0 (TL)	4	IO	PT6C	D3	L11T_A0
D9	0 (TL)	4	IO	PT6B	VREF_0_04	L12C_D0
C8	0 (TL)	4	IO	PT6A	—	L12T_D0
E9	0 (TL)	5	IO	PT5D	D1	L13C_D0
D8	0 (TL)	5	IO	PT5C	D2	L13T_D0
AB13	—	—	Vss	Vss	—	—
A7	0 (TL)	5	IO	PT5B	—	L14C_A0
A6	0 (TL)	5	IO	PT5A	VREF_0_05	L14T_A0
C7	0 (TL)	5	IO	PT4D	TDI	L15C_D0
B6	0 (TL)	5	IO	PT4C	TCK	L15T_D0
E8	0 (TL)	5	IO	PT4B	—	L16C_A0
E7	0 (TL)	5	IO	PT4A	—	L16T_A0
A5	0 (TL)	6	IO	PT3D	—	L17C_A0
B5	0 (TL)	6	IO	PT3C	VREF_0_06	L17T_A0
AB14	—	—	Vss	Vss	—	—
C6	0 (TL)	6	IO	PT3B	—	L18C_A0
D6	0 (TL)	6	IO	PT3A	—	L18T_A0

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
U21	—	—	VDD15	VDD15	—	—
U22	—	—	VDD15	VDD15	—	—
V13	—	—	VDD15	VDD15	—	—
V14	—	—	VDD15	VDD15	—	—
V15	—	—	VDD15	VDD15	—	—
V20	—	—	VDD15	VDD15	—	—
V21	—	—	VDD15	VDD15	—	—
V22	—	—	VDD15	VDD15	—	—
W13	—	—	VDD15	VDD15	—	—
W14	—	—	VDD15	VDD15	—	—
W15	—	—	VDD15	VDD15	—	—
W20	—	—	VDD15	VDD15	—	—
W21	—	—	VDD15	VDD15	—	—
W22	—	—	VDD15	VDD15	—	—
Y16	—	—	VDD15	VDD15	—	—
Y17	—	—	VDD15	VDD15	—	—
Y18	—	—	VDD15	VDD15	—	—
Y19	—	—	VDD15	VDD15	—	—
T32	—	—	NC	NC	—	—
W32	—	—	NC	NC	—	—

Note that ΘJB is expressed in units of °C/W and that this parameter and the way it is measured are still being discussed by the JEDEC committee.

FPSC Maximum Junction Temperature

Once the power dissipated by the FPSC has been determined, the maximum junction temperature of the FPSC can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Derating calculations for other temperatures than 85 °C and for other voltages can be made within the ispLEVER software environment. Using the maximum ambient temperature, T_{Amax}, and the power dissipated by the device, Q (expressed in °C), the maximum junction temperature is approximated by:

$$T_{Jmax} = T_{Amax} + (Q \cdot \Theta_{JB}) \quad (5)$$

Package Thermal Characteristics

The thermal characteristics of the 484-ball PBGAM (fpBGA with heat spreader) used for the ORT42G5, 680-ball PBGAM (fpBGA with heat spreader) and 680-ball fpBGA used for the ORT82G5 are available in the Thermal Management section of the Lattice web site at www.latticesemi.com.

Heat Sink Vendors for BGA Packages

The estimated worst-case power requirements for the ORSO42G5 and ORSO82G5 are in the 3 W to 5 W range. Consequently, for most applications an external heat sink will be required. Table 53 lists, in alphabetical order, heat sink vendors who advertise heat sinks aimed at the BGA market.

Table 53. Heat Sink Vendors

Vendor	Location	Phone
Aavid Thermal Technology	Laconia, NH	(603) 527-2152
Chip Coolers	Warwick, RI	(800) 227-0254
IERC	Burbank, CA	(818) 842-7277
R-Theta	Buffalo, NY	(800) 388-5428
Sanyo Denki	Torrance, CA	(310) 783-5400
Thermalloy	Dallas, TX	(214) 243-4321
Wakefield Engineering	Wakefield, MA	(617) 246-0874

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 54 lists eight parasitics associated with the ORCA packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 54 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.