Lattice Semiconductor Corporation - ORSO42G5-2BMN484C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso42g5-2bmn484c

device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, uplink and downlink functions, and other functions on two output signals. Large blocks of 512 x 18 block-port RAM complement the existing distributed PFU memory. The RAM blocks can be used to implement RAM, ROM, FIFO, multiplier, and CAM. Some of the other system-level functions include the MPI, PLLs, and the Embedded System Bus (ESB).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/FFs, and one additional Flip-Flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-block fashion; two sets of four LUTs and FFs that can be controlled independently. Each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected from PLC routing resources and from the outputs of the PFU. It contains eight 3-state, bidirectional buffers, and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections from the PFU outputs make fast, true, 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Programmable I/O

The Series 4 PIO addresses the demand for the flexibility to select I/Os that meet system interface requirements. I/Os can be programmed in the same manner as in previous *ORCA* devices, with the additional new features which allow the user the flexibility to select new I/O types that support High-Speed Interfaces.

Each PIO contains four programmable I/O pads and is interfaced through a common interface block to the FPGA array. The PIO is split into two pairs of I/O pads with each pair having independent clock enables, local set/reset, and global set/reset. On the input side, each PIO contains a programmable latch/Flip-Flop which enables very fast latching of data from any pad. The combination provides for very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer with a PFU.

On the output side of each PIO, an output from the PLC array can be routed to each output Flip-Flop, and logic can be associated with each I/O pad. The output logic associated with each pad allows for multiplexing of output signals and other functions of two output signals.

The output FF, in combination with output signal multiplexing, is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The output buffer signal can be inverted, and the 3-state control can be made active-high, active-low, or always enabled. In addition, this 3-state signal can be registered or nonregistered.

The Series 4 I/O logic has been enhanced to include modes for speed uplink and downlink capabilities. These modes are supported through shift register logic, which divides down incoming data rates or multiplies up outgoing data rates. This new logic block also supports high-speed DDR mode requirements where data are clocked into and out of the I/O buffers on both edges of the clock.

The new programmable I/O cell allows designers to select I/Os which meet many new communication standards permitting the device to hook up directly without any external interface translation. They support traditional FPGA standards as well as high-speed, single-ended, and differential-pair signaling. Based on a programmable, bank-oriented I/O ring architecture, designs can be implemented using 3.3V, 2.5V, 1.8V, and 1.5V referenced output levels.

ORSO42G5 and ORSO82G5 Embedded Core Detailed Description

The ORSO42G5 and ORSO82G5 have four and eight channels respectively, with a high-speed SERDES macro that performs clock data recovery, serializing and deserializing functions. There is also additional logic for SONET mode and cell mode data synchronization formatting and scrambling/descrambling. For all modes, the data paths can be characterized as the transmit path (FPGA to backplane) and receive path (backplane to FPGA); however the interface signal assignments between the FPGA logic and the core differ depending on the operating mode selected.

The three main operating modes in the ORSO42G5 and ORSO82G5 are:

- SERDES only mode
- SONET mode
- Cell mode
  - Two-link sub-mode
  - Eight-link sub-mode (ORSO82G5 only)

The SONET and cell modes each support sub-modes that can be selected by enabling or disabling certain functions through programmable register bits. Following the basic TX and RX architecture descriptions, the data formatting and logical implementations supporting each of the operational modes are described.

Top Level Description - Transmitter (TX) and Receiver (RX) Architectures

The next sections give a top level description of the transmitter and receive architectures. The high-speed transmit and receive serial data can operate at 0.6-2.7 Gbps depending on the state of the control bits from the system bus and the provided reference clock. For all of the architecture and clock distribution descriptions, however, the standard SONET STS-48 rate of 2,488.32 Mbits/s (i.e., REFCLK_[P:N] = 155.52 MHz for the full rate modes) is assumed.

Transmitter Architecture

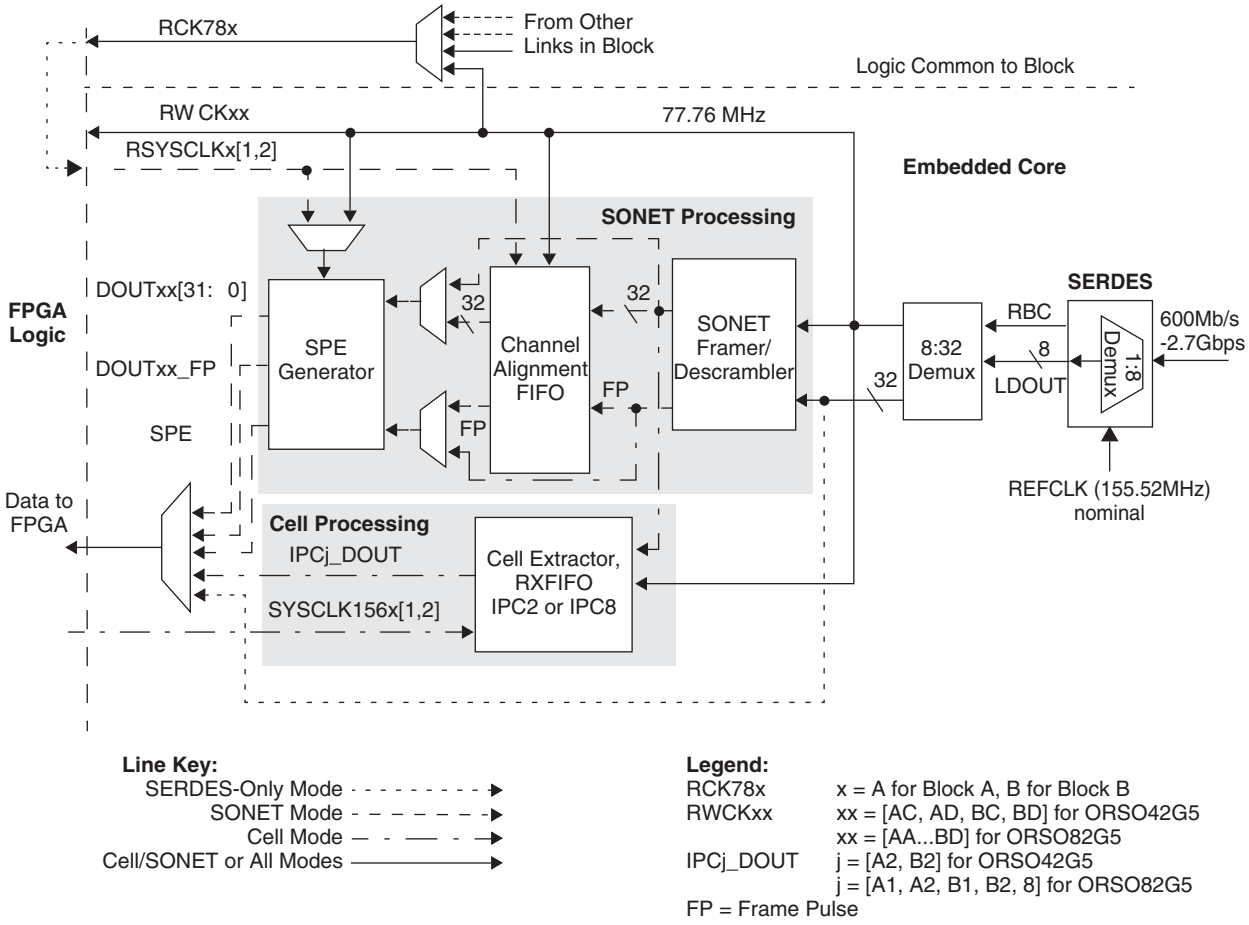
The transmitter section accepts parallel data for transmission from the FPGA logic, formats it for transmission and serializes the data. It also accepts the low-speed reference clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock. The serialized transmitted data are available at the differential CML output pins to drive either an optical transmitters, coaxial media or a circuit board backplane.

The top level transmit architecture is shown in Figure 3. The main logical blocks in the transmit path are:

- Output Port Controllers (OPCs) which contain the cell processing logic.
- SONET processing logic.
- Transmit SERDES and 32:8 MUX.

Depending on the mode of operation, the FPGA to backplane data path may include or bypass the various logical blocks.

Figure 4. Top Level Overview, RX Path Logic, Single Channel



In either the SONET or cell mode, data from the DEMUX is then passed through a framer which word aligns and frames the data. Data are then processed based on cell mode or SONET mode selection.

In the SONET mode, the descrambled data are sent to an alignment FIFO that performs lane-to-lane deskew and optionally aligns data within a multi-channel alignment group. In addition, supervisory features such as BIP error check, OOF check, RDI monitoring and AIS-L insertion during OOF are also implemented. All the supervisory features are controlled through programmable register bits.

In the cell mode, the framed data are then descrambled and passed into a cell extractor which extracts cells from the payload portion of the SONET frame. The cells are passed through a FIFO that performs lane-to-lane deskew and a clock domain transfer from 77.76 MHz to 155.52 MHz. A key feature in cell mode is the ability to use idle cell insertion and deletion for automatic rate matching between the clock domains. The cells are then passed to the IPC2 block (or, in the ORSO82G5, to the IPC8 block) which perform cell destriping before sending the cells to the FPGA logic across the Core/FPGA interface.

SERDES Transmit and Receive PLLs

The high-speed transmit and receive serial data can operate at 0.6 to 2.7 Gbps depending on the state of the control bits from the system bus. Table 2 shows the relationship between the data rates, the reference clock, and the internal transmit TCK78x clocks.

- E1 - Section order wire byte - This byte carries local orderwire information, which provides for a 64 Kbps voice channel between two Section Termination Equipment (STE) devices.
- F1 - Section user channel byte - This byte provides a 64 Kbits/s user channel which can be used in a proprietary fashion.
- D1, D2, D3 - Section Data Communications Channel (SDCC) bytes - These bytes provide a 192 Kbits/s channel for transmission of information across STEs. This information could be for control and configuration, status monitoring, alarms, network administration data etc.

Line Overhead Bytes:

- H1, H2 - STS Payload Pointers (H1 and H2) - These bytes are used to locate the start of the SPE in a SONET frame. These two bytes contain the offset value, in bytes, between the pointer bytes and the start of the SPE. These bytes are used for all the STS-1 signals contained in an STS-N signal to indicate the individual starting positions of the SPEs. They bytes also contain justification indications, concatenation indications and path alarm indication (AIS-P).
- H3 - Pointer Action Byte (H3) - This byte is used during frequency justifications. When a negative justification is performed, one extra payload byte is inserted into the SONET frame. The H3 byte is used to hold this extra byte and is hence called the pointer action byte. When justification is not being performed, this byte contains a default value of 0x00.
- B2 - Line Bit-Interleaved Parity code (BIP-8) byte - This byte carries the parity information which is used to check for transmission errors in a line. This is a even parity computed over all the bytes of the frame, except section overhead bytes, before scrambling. The computed parity value is transmitted in the next frame in the B2 position. This byte is defined for all the STS-1signals in an STS-N signal.
- K1, K2 - Automatic Protection Switching (APS channel) bytes - These bytes carry the APS information. They are used for implementing automatic protection switching and for transmitting the line Alarm Indication Signal (AIS-L) and the Remote Defect Indication (RDI-L) signal.
- D4 to D12 - Line Data Communications Channel (DCC) bytes - These bytes provide a 576 Kbps channel for transmission of information.
- S1- Synchronization Status - This byte carries the synchronization status of the network element. It is located in the first STS-1 of an STS-N. Bits 5 through 8 of this byte carry the synchronization status.
- Z1 - Growth - This byte is located in the second through Nth STS-1s of an STS-N and are allocated for future growth. An STS-1 signal does not contain a Z1 byte.
- M0 - STS-1 REI-L - This byte is defined only for STS-1 signals and is used to convey the Line Remote Error Indication (REI-L). The REI-L is the count of the number of B2 parity errors detected by an LTE and is transmitted to its peer LTE as feedback information. Bits 5 through 8 of this byte are used for this function.
- E2 - Orderwire byte - This byte carries for line orderwire information.

SONET Mode Transmit Path

The transmit block performs the following functions in SONET mode:

- A1 and A2 insertion and optional corruption
- BIP-8 parity calculation, B1 byte insertion and optional corruption. (B1 byte is inverted.)
- Performs RDI insertion (K2 byte is set to “0000 0110”).
- Scrambling of outgoing data with optional scrambler disabling.

In either STS-192 or STS-48 mode, each link operates at an STS-48 rate.

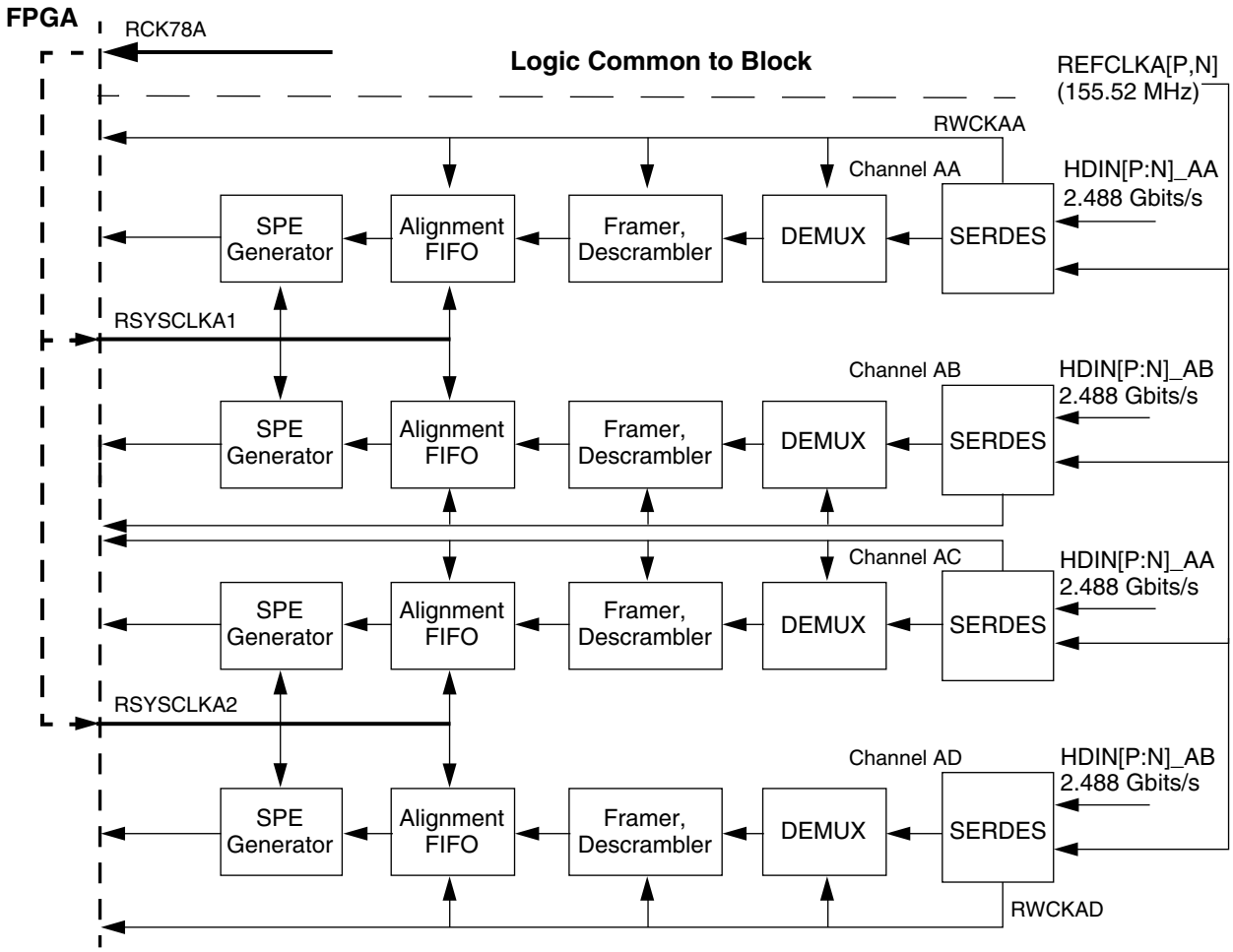
TX Frame Processor

The Tx_Frame_Processor (TFP) block is the primary data processing block in the both SONET mode and cell mode. It organizes the cell data into a SONET frame before sending it to the SERDES. The TFP is on the TSYCLKxx clock domain (77.76 MHz). In SONET mode, the 32-bit data comes from the FPGA interface. (In cell mode the data comes from the cell processing block as described in the cell mode section) The TFP block contains three major sub-blocks: payload block, TOH block and scrambler block. The interfaces for the TFP block are shown in Figure 16.

SONET Mode Block Alignment – ORSO82G5

Figure 28 describes the clocks and recommended clocking for block alignment in the SONET mode. For block alignment, the low speed portion for each block should be sourced by a single clock. As the figure shows, for block A, RSYSCLKA1 and RSYSCLKA2 should be sourced by RCK78A. For block B, RSYSCLKB1 and RSYSCLKB2 should be sourced by RCLK78B. RCLK78A can be sourced by any channel in block A and RCLK78B can be sourced by any channel in block B.

Figure 28. Receive Clocking Diagram for Four-Channel Alignment in Block A – ORSO82G5

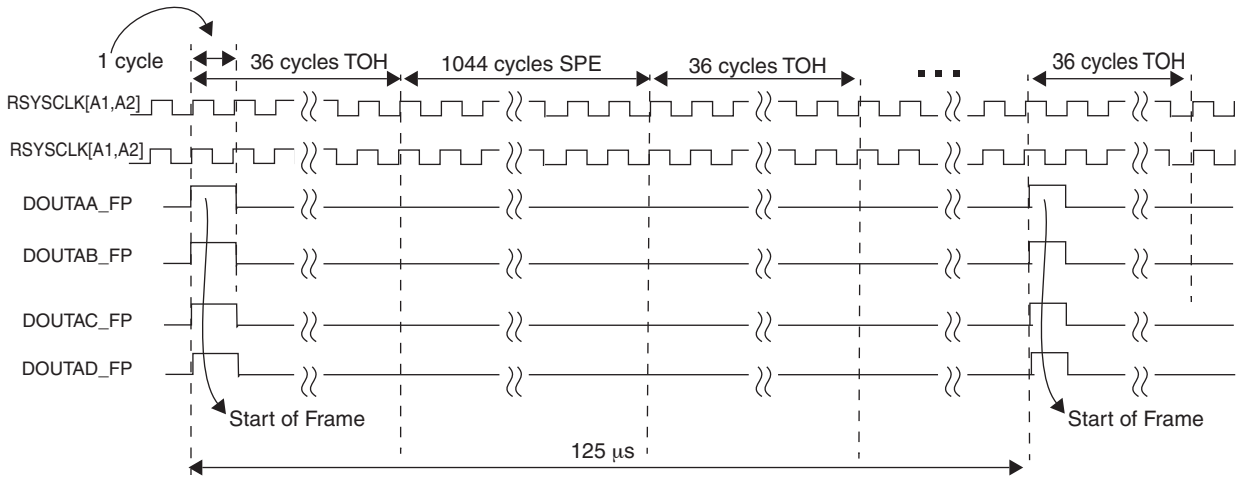


SONET Mode Octal Alignment – ORSO82G5

Figure 29 shows the clocking scheme for eight-channel alignment. In this application, all four clocks RSYSCLKA1, RSYSCLKA2, RSYSCLKB1 and RSYSCLKB2 should be sourced from a common clock. Either RCK78A or RCK78B can be used as a common clock source. The figure shows RCK78A being used as the clock source.

Figure 33 shows the SONET quad alignment mode in the ORSO82G5.

Figure 33. Receive Clocking Diagram for SONET Mode Quad Alignment – ORSO82G5

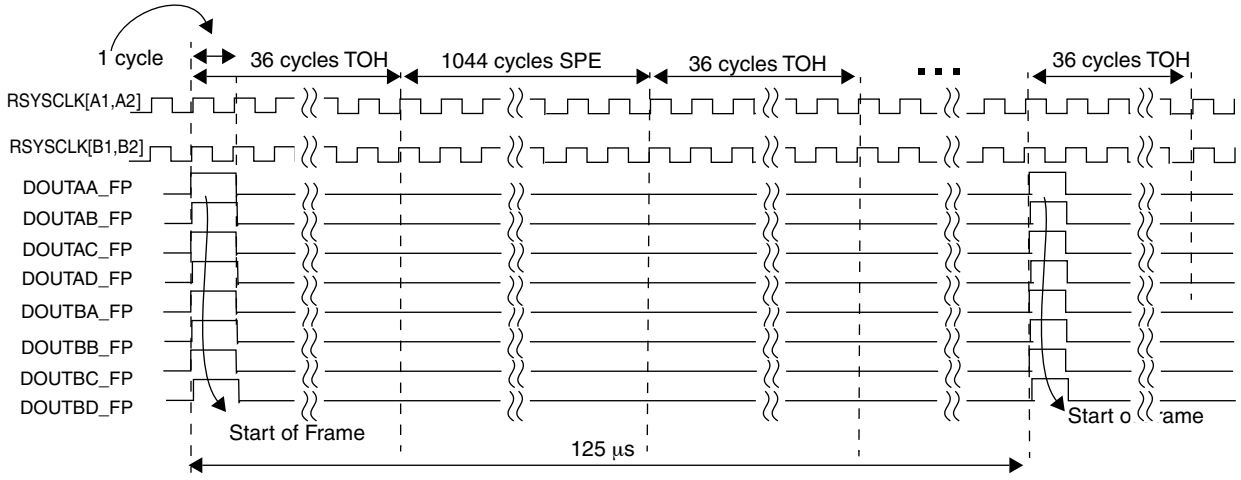


Clocks
RSYSCLKA1 and RSYSCLKA2 are sourced by RCK78A

- Only frame pulse (DOUTxx_FP) and clocks are shown for understanding of block alignment.
- Timing of data and SPE indicators are the same as shown for twin alignment.
- Block groups are Group A - AA,AB,AC,AD and Group B - BA,BB,BC,BD

Figure 34 shows the octal alignment mode in the ORSO82G5.

Figure 34. Receive SONET Mode—Octal Alignment Mode – ORSO82G5



Clocks
RSYSCLKA1, RSYSCLKA2, RSYSCLKB1, and RSYSYSCLKB2 are sourced by RCK78A

ORSO42G5 Configuration

At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

- Setting bit 1 to one in registers at locations 30002, 30012, 30102 and 30112 powers down the legacy logic. (Note that the reset value for these bits is 0.)
- Setting bit 1 to zero (reset condition) in the register at locations 30802, 30812, 30902 and 30912 removes the legacy logic from any alignment group.

Register settings for SONET multi-channel alignment are shown in Table 7.

Table 7. Multichannel Alignment Modes – ORSO42G5

Register Bits FMPU_SYNMODE_xx[2:3]	Mode
00	No multichannel alignment
01	Twin channel alignment
11	Four channel alignment

Note: xx = [AC,AD,BC,BD]

To align two channels in SERDES A:

- FMPU_SYNMODE_AC = 01 (Register Location 30822)
- FMPU_SYNMODE_AD = 01 (Register Location 30832)

To align two channels in SERDES B:

- FMPU_SYNMODE_BC = 01 (Register Location 30922)
- FMPU_SYNMODE_BD = 01 (Register Location 30932)

To align all four channels:

- FMPU_SYNMODE_AC = 11 (Register Location 30822)
- FMPU_SYNMODE_AD = 11 (Register Location 30832)
- FMPU_SYNMODE_BC = 11 (Register Location 30922)
- FMPU_SYNMODE_BD = 11 (Register Location 30932)

To enable/disable multi-channel alignment of individual channels within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled

where xx = [AC,AD,BC,BD]

To resynchronize a multichannel alignment group set the following bits to one, and then set to zero:

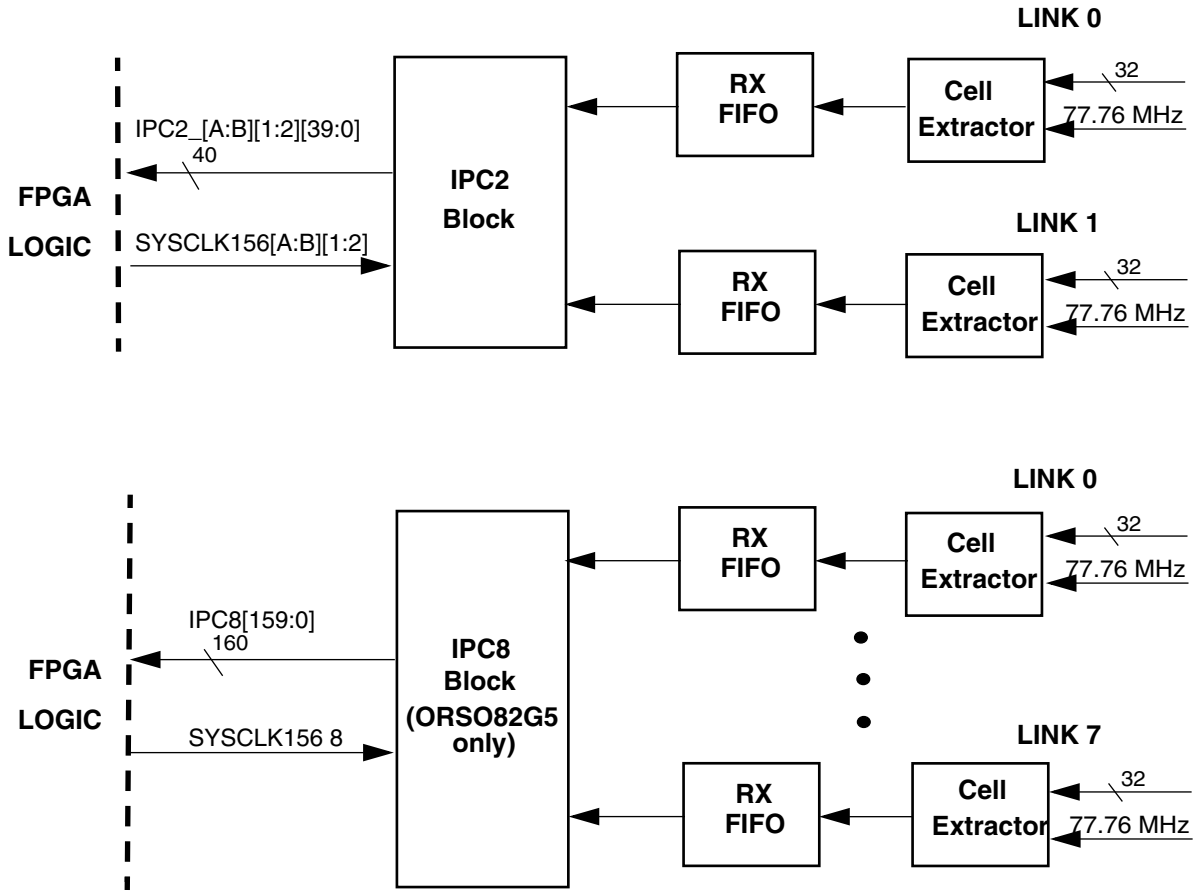
- FMPU_RESYNC4 for four channels, AC, AD, BC and BD. (Register Location 30A04, bit 7)
- FMPU_RESYNCA2 for dual channels, AC and AD. (Register Location 30A04, bit 2)
- FMPU_RESYNCB2 for dual channels, BC and BD. (Register Location 30A04, bit 5)

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bits to one, and then set to zero.

- FMPU_RESYNC1_xx (Register Locations 30824, 20834, 30924 and 30934, bit 7) where xx is one of AC, AD, BC or BD.

- Insuring group bundles are properly aligned.
- Scheduling reads from the RX FIFOs. Cells are read one at a time from the configured links.
- Parsing the cell data into payload data (along with selected header information). Cells which have errors that make them unusable (such as BIP or sequence number errors) are thrown away. This dropping of errored cells can be disabled through register bits CELL_BIP_INH_xx and CELL_SEQ_INX_xx.

Figure 44. IPC2 and IPC8 Block Diagrams



There are 5 IPC blocks in the embedded core. There is an IPC2 block for every channel pair:

- IPC2_A1 combines links from channels AA,AB (ORSO82G5 only)
- IPC2_A2 combines links from channels AC,AD
- IPC2_B1 combines links from channels BA,BB (ORSO82G5 only)
- IPC2_B2 combines links from channels BC,BD

The IPC8 block combines cells from all eight aligned links and transmits them to the FPGA logic (ORSO82G5 only).

Before an IPC can begin reading data from the Rx FIFOs and assembling cells, it must first align all FIFOs in a port bundle. This is accomplished by handshaking signals between the framer and the IPC. The framer indicates to the IPC that framing has been acquired. The framer does not start filling the FIFOs, however, until the next A1/A2 SONET signal.

- Note that RXDxx[39:32] signal assignments are the same no matter what mode the RX blocks are in.

Table 13 summarizes the signals across the Core/FPGA interface in the receive direction.

Table 13. RX Core/FPGA Interface Signals – ORSO42G5

RXDAC[39:0]	SONET mode	IPC2 A2 Mode
39	SYNC2_A2_OOS	—
38	—	IPC2_A2_CELLDROP
37	—	IPC2_A2_CELLSTART
36	DOUTAC_FP	—
35	DOUTAC_OOF	
34	DOUTAC_SPE	—
33	—	IPC2_A2_CELL_BIP_ERR
32	DOUTAC_B1_ERR	
[31:20]	DOUTAC[31:20]]	—
[19:0]	DOUTAC[19:0]	IPC2_A2[39:20]
RXDAD[39:0]	SONET Mode	IPC2 A2 Mode
39	—	—
38	—	—
37	—	CELL_BEGIN_OK_A2
36	DOUTAD_FP	—
35	DOUTAD_OOF	
34	DOUTAD_SPE	—
33	—	—
32	DOUTAD_B1_ERR	
[31:20]	DOUTAD[31:20]	—
[19:0]	DOUTAD[19:0]	IPC2_A2[19:0]
RXDBC[39:0]	SONET Mode	IPC2 B2 Mode
39	SYNC2_B2_OOS	—
38	—	IPC2_B2_CELLDROP
37	—	IPC2_B2_CELLSTART
36	DOUTBC_FP	—
35	DOUTBC_OOF	
34	DOUTBC_SPE	—
33	—	IPC2_B2_CELL_BIP_ERR
32	DOUTBC_B1_ERR	
[31:20]	DOUTBC[31:20]	—
[19:0]	DOUTBC[19:0]	IPC2_B2[39:20]
RXDBD[39:0]	SONET Mode	IPC2 B2 Mode
39	—	
38	SYNC4_B_OOS	—
37	—	CELL_BEGIN_OK_B2
36	DOUTBD_FP	—
35	DOUTBD_OOF	
34	DOUTBD_SPE	—

Table 13. RX Core/FPGA Interface Signals – ORSO42G5 (Continued)

33	—	
32	DOUTBD_B1_ERR	
[31:20]	DOUTBD[31:20]	—
[19:0]	DOUTBD[19:0]	IPC2_B2[19:0]

Signal Description for RX Path (SERDES Core to FPGA) – ORSO82G5

- Signals are divided across 8 channels with 40 signals per channel. RXDxx[39:0] is the set of 40 signals for a channel xx.
- All RX direction signals are outputs from the core.
- See Figure 47 for clock transfers across the FPGA/Core interface.
- In SONET mode, RXDxx[31:0] carries 32 bit data from the alignment FIFO of the respective channel. RXDxx[35:32] carries miscellaneous information such as OOF, BIPERR, Frame Pulse (FP), and SPE.
- In cell mode, data from each of the four 2-link IPC bundles are spread across all eight channels and are assigned to the 20 LSBs (RXDxx[19:0]) of each channel output. Data from IPC2_A1 is distributed across RXDAA[19:0] and RXDAB[19:0]. Data from IPC2_A2 is distributed across RXDAC[19:0] and RXDAD[19:0]. This symmetry is maintained for IPC2 data signals from block B.
- Data from the 8-link IPC block IPC8 is spread across all eight channels and assigned to the 20 LSB's (RXDxx[19:0] of each channel output.
- The IPC status signals for Cell Mode operation are contained in RXDxx[39:36] and RXDxx[33].
- The signals for SONET Mode operation are assigned to RXDxx[35:34] and RXDxx[33].
- Note that RXDxx[39:32] signal assignments are the same no matter what mode the RX blocks are in.

Table 14 summarizes the signals across the Core/FPGA interface in the receive direction.

Table 14. RX Core/FPGA Interface Signals – ORSO82G5

RXDAA[39:0]	SONET mode	IPC2 A1 Mode	IPC8 Mode
39	SYNC2_A1_OOS	—	
38	—	IPC2_A1_CELLDROP	—
37	—	IPC2_A1_CELLSTART	—
36	DOUTAA_FP	—	
35	DOUTAA_OOF		
34	DOUTAA_SPE	—	
33	—	IPC2_A1_CELL_BIP_ERR	—
32	DOUTAA_B1_ERR		
[31:20]	DOUTAA[31:20]	—	
[19:0]	DOUTAA[19:0]	IPC2_A1[39:20]	—
RXDAB[39:0]	SONET mode	IPC2 A1 Mode	IPC8 Mode
39	—	—	
38	SYNC4_A_OOS	—	
37	—	CELL_BEGIN_OK_A1	—
36	DOUTAB_FP	—	
35	DOUTAB_OOF		
34	DOUTAB_SPE	—	

Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30823 - AC 30833 - AD 30923 - BC 30933 - BD	[0]	BYPASS_ALGN_FIFO_xx	00	Bypass alignment FIFO =1 in RX path in SONET mode. DOUT_xx data is clocked off RWCKxx.	SONET
	[1]	SERDES_ONLY_MODE_xx		SERDES-Only Mode. SERDES_ONLY_MODE =1 bypasses all the SONET and cell functions. Data is sent directly from the SERDES to the FPGA logic in the RX path and is passed directly from the FPGA logic to the SERDES in the TX path.	SERDES Only
	[2]	FORCE_B1_ERR_xx		Force B1 Error. FORCE_B1_ERR =1 forces a Section B1 error (Bit Interleaved Parity Error) in the TX path. Valid only when the corresponding AUTO_TOH_xx bit or AUTO_B1_xx bit is set to one.	Both
	[3]	FORCE_BIP8_ERR_xx		Force BIP8 Error, FORCE_BIP8_ERR =1 forces cell BIP8 error in the TX path.	Cell
	[4]	FORCE_A1A2_ERR_xx		Force A1A2 Error, FORCE_A1A2_ERR =1 forces an error in A1A2 bytes (framing error) in the TX path. Valid only when the corresponding AUTO_TOH_xx bit or AUTO_A1A2_xx bit is set to one.	Both
	[5]	FORCE_EX_SEQ_ERR_xx		Force Excessive Sequence Errors. FORCE_EXP_SEQ_ERR_xx = 1 forces sequence errors in the TX path by inverting the link header byte sequence number.	Cell
	[6]	FORCE_SEQ_ERR_xx		Force Sequence Error, FORCE_SEQ_ERR =1 forces one sequence error in the TX path. After this bit is set, the next Link Header byte's sequence number is inverted. The Link Header after the errored Link Header byte will have the correct sequence number	Cell
	[7]	FORCE_RDI_xx		Force Remote Defect Indication, FORCE_RDI =1 forces RDI errors in the TX path. The K2 byte in TOH is set to "00000110. Valid only when AUTO_TOH_xx bit is set to 1.	Cell

Table 28. Common Control Register Descriptions – ORSO42G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A00	[0:1]	RCKSELB	00	“10” - Channel BC source for clock RCK78B “11” - Channel BD source for clock RCK78B	Both
	[2:3]	TCKSELB		“10” - Channel BC source for clock TCK78B “11” - Channel BD source for clock TCK78B	Both
	[4:5]	RCKSELA		“10” - Channel AC source for clock RCK78A “11” - Channel AD source for clock RCK78A	Both
	[6:7]	TCKSELA		“10” - Channel AC source for clock TCK78A “11” - Channel AD source for clock TCK78A	Both
30A01	[0:2]	CELL_SIZE	00	Cell Size, Three bits to set cell size. “000” - Cell size is 75 bytes, “001” - Cell size is 79 bytes, “010” - Cell size is 83 bytes, “011” - Cell size is 91 bytes These are the only supported cell sizes.	Cell
	[3:7]	RX_FIFO_MIN		Set Minimum threshold value for alignment FIFO in SONET mode. When the read address for the FIFO is below this value at the time when write address is zero, it indicates that the FIFO is near overflow. This event will go high only once during a frame when a framing byte has been detected by the aligner. The default threshold value is “00000”.	SONET
30A02	0	TX_DISABLE_ON_RDI	00	Transmitter Disable on RDI (Detection), If TX_DISABLE_ON_RDI = 1 - No cell data is transmitted on a link in which a RDI has been detected by the corresponding link’s receiver. If this bit is set to 0, cell data will be transmitted on a link irrespective of detection of a RDI.	Cell
	[1:7]	RSVD		Reserved	—

Table 35. Per-Channel Status Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
3080B - AA 3081B - AB 3082B -AC 3083B - AD 3090B - BA 3091B - BB 3092B - BC 3093B - BD	[0]	RSVD	00	Reserved	—
	[1]	STAT_OOF_xx		STAT_OOF_xx = 1 same as OOF_xx except that a 1 on this bit can NOT cause an interrupt	Both
	[2]	STAT_EX_SEQ_ERR_xx		STAT_EX_SEQ_ERR_xx = 1 same as EX_SEQ_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[3]	STAT_SEQ_ERR_xx		STAT_SEQ_ERR_xx = 1 same as SEQ_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[4]	STAT_CELL_BIP_ERR_xx		STAT_CELL_BIP_ERR_xx = 1 same as CELL_BIP_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[5]	STAT_B1_ERR_xx		STAT_B1_ERR_xx = 1 same as B1_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Both
	[6]	STAT_RX_FIFO_OVRUN_xx		STAT_RX_FIFO_OVRUN_xx = 1 same as RX_FIFO_OVRUN_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[7]	STAT_RDI_xx		STAT_RDI_xx = 1 same as RDI_xx except that a 1 on this bit can NOT cause an interrupt	Both
3080C - AA 3081C - AB 3082C - AC 3083C - AD 3090C - BA 3091C - BB 3092C - BC 3093C - BD	[0:7]	LINK_NUM_RX_xx	00	Link number received that is stored in the F1 byte position of the SONET TOH	Both
3080E - AA 3081E - AB 3082E - AC 3083E AD 3090E - BA 3091E - BB 3092E- BC 3093E - BD	[0:5]	RSVD	00	Reserved	—
	[6]	CH248_SYNC_xx		CH248_SYNC_xx = 1 indicates that A1A2 bytes have been detected by link xx for multi-channel alignment	SONET
	[7]	RX_LINK_GOOD_xx		RX_LINK_GOOD_xx = 1 indicates that frame has been acquired and the link has been stable. Goes high at an A1A2 boundary but can go low at any point in a frame due to excessive errors	Cell

High Speed Data Transmitter

Table 40 specifies serial data output buffer parameters measured on devices with typical and worst case process parameters and over the full range of operation conditions.

Table 40. Serial Output Timing and Levels (CML I/O)

Parameter	Min.	Typ.	Max.	Units
Rise Time (20% - 80%)	50	80	110	ps
Fall Time (80% - 20%)	50	80	110	ps
Common Mode	V_{DDOB} – 0.30	V_{DDOB} – 0.25	V_{DDOB} – 0.15	V
Differential Swing (Full Amplitude)[1]	750	900	1000	mV_{p-p}
Differential Swing (Half Amplitude)[1]	375	450	500	mV_{p-p}
Output Load (External)	—	86	—	Ω

1. Differential swings measured at the end of 3 inches of FR-4 and 12 inches of coax cable.

Transmitter output jitter is a critical parameter to systems with high speed data links. Table 41 and Table 42 specify the transmitter output jitter for typical and worst case devices over the full range of operating conditions.

Table 41. Channel Output Jitter (2.7 Gbps)

Parameter	Device	Min.	Typ.[1]	Max.[1]	Units
Deterministic	ORSO42G5	—	0.12	0.16	Ulp-p
	ORSO82G5	—	0.12	0.16	Ulp-p
Random[2]	ORSO42G5	—	0.05	0.18	Ulp-p
	ORSO82G5	—	0.05	0.08	Ulp-p
Total[3]	ORSO42G5	—	0.17	0.34	Ulp-p
	ORSO82G5	—	0.17	0.24	Ulp-p

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Wavecrest SIA-3000 instrument used to measure one-sigma (RMS) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10^{-12}.
3. Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10^{-12}. See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

Table 42. Channel Output Jitter (2.5 Gbps)

Parameter	Device	Min.	Typ.[1]	Max.[1]	Units
Deterministic	ORSO42G5	—	0.11	0.13	Ulp-p
	ORSO82G5	—	0.11	0.13	Ulp-p
Random[2]	ORSO42G5	—	0.05	0.14	Ulp-p
	ORSO82G5	—	0.05	0.07	Ulp-p
Total[3]	ORSO42G5	—	0.16	0.27	Ulp-p
	ORSO82G5	—	0.16	0.20	Ulp-p

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Wavecrest SIA-3000 instrument used to measure one-sigma (RMS) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10^{-12}.
3. Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10^{-12}. See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

Table 47. Pin Descriptions (Continued)

Symbol	I/O	Description
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user programmable I/O, if not used for clock inputs.
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O if boundary scan is not used.[1]
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration this pin is a user-programmable I/O pin.[1]
HDC	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{LDC}}$	O	$\overline{\text{Low During Configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.[1]
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
$\overline{\text{WR}}$/MPI_RW	I	$\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{\text{WR}}$/MPI_RW is a user-programmable I/O pin.[1]
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the PowerPC bus master utilizing the least-significant bits of the PowerPC 32-bit address.
$\overline{\text{MPI\_BURST}}$	I	$\overline{\text{MPI\_BURST}}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.
$\overline{\text{MPI\_BDIP}}$	I	$\overline{\text{MPI\_BDIP}}$ is driven by the PowerPC processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	O	During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
G16	-	-	VDD15	VDD15	-	-
H13	-	-	VSS	VSS	-	-
AB10	5 (BC)	2	IO	PB19A	-	L37T
AA10	5 (BC)	2	IO	PB19B	-	L37C
W10	5 (BC)	2	IO	PB19C	PBCK0T	L38T
Y10	5 (BC)	2	IO	PB19D	PBCK0C	L38C
V10	5 (BC)	2	IO	PB20A	-	-
U13	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB11	5 (BC)	2	IO	PB20C	VREF_5_02	L39T
AA11	5 (BC)	2	IO	PB20D	-	L39C
U10	5 (BC)	2	IO	PB21A	-	-
H6	-	-	VDD15	VDD15	-	-
Y11	5 (BC)	3	IO	PB21C	-	L40T
W11	5 (BC)	3	IO	PB21D	VREF_5_03	L40C
U11	5 (BC)	3	IO	PB22A	-	-
J7	-	-	VSS	VSS	-	-
AB12	5 (BC)	3	IO	PB22C	-	L41T
AA12	5 (BC)	3	IO	PB22D	-	L41C
U12	5 (BC)	3	IO	PB23A	-	-
Y12	5 (BC)	3	IO	PB23C	PBCK1T	L42T
W12	5 (BC)	3	IO	PB23D	PBCK1C	L42C
V11	5 (BC)	3	IO	PB24A	-	-
J8	-	-	VSS	VSS	-	-
AB13	5 (BC)	4	IO	PB24C	-	L43T
AA13	5 (BC)	4	IO	PB24D	-	L43C
V12	5 (BC)	4	IO	PB25A	-	-
U14	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB14	5 (BC)	4	IO	PB25C	-	L44T
AA14	5 (BC)	4	IO	PB25D	VREF_5_04	L44C
J9	-	-	VSS	VSS	-	-
Y13	5 (BC)	5	IO	PB26C	-	L45T
W13	5 (BC)	5	IO	PB26D	VREF_5_05	L45C
U15	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB15	5 (BC)	5	IO	PB27C	-	L46T
AA15	5 (BC)	5	IO	PB27D	-	L46C
AB16	5 (BC)	6	IO	PB28C	-	L47T
AA16	5 (BC)	6	IO	PB28D	VREF_5_06	L47C
H14	-	-	VDD15	VDD15	-	-
Y14	5 (BC)	6	IO	PB29C	-	L48T
W14	5 (BC)	6	IO	PB29D	-	L48C
J10	-	-	VSS	VSS	-	-
AB17	5 (BC)	7	IO	PB30C	-	L49T
AA17	5 (BC)	7	IO	PB30D	-	L49C
U16	5 (BC)	-	VDDIO5	VDDIO5	-	-

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM4	6 (BL)	5	IO	PB2A	DP2	L13T_D0
AL5	6 (BL)	5	IO	PB2B	—	L13C_D0
AN7	6 (BL)	—	VDDIO6	VDDIO6	—	—
AP3	6 (BL)	5	IO	PB2C	PLL_CK6T/PPLL	L14T_A0
AP4	6 (BL)	5	IO	PB2D	PLL_CK6C/PPLL	L14C_A0
AN4	6 (BL)	5	IO	PB3B	—	—
U16	—	—	VSS	VSS	—	—
AK6	6 (BL)	5	IO	PB3C	—	L15T_A0
AK7	6 (BL)	5	IO	PB3D	—	L15C_A0
AL6	6 (BL)	5	IO	PB4A	VREF_6_05	L16T_A0
AM6	6 (BL)	5	IO	PB4B	DP3	L16C_A0
AP1	6 (BL)	—	VDDIO6	VDDIO6	—	—
AN5	6 (BL)	6	IO	PB4C	—	L17T_A0
AP5	6 (BL)	6	IO	PB4D	—	L17C_A0
AK8	6 (BL)	6	IO	PB5B	—	—
U17	—	—	VSS	VSS	—	—
AP6	6 (BL)	6	IO	PB5C	VREF_6_06	L18T_D0
AP7	6 (BL)	6	IO	PB5D	D14	L18C_D0
AM7	6 (BL)	6	IO	PB6A	—	L19T_D0
AN6	6 (BL)	6	IO	PB6B	—	L19C_D0
AP2	6 (BL)	—	VDDIO6	VDDIO6	—	—
AL8	6 (BL)	7	IO	PB6C	D15	L20T_A0
AL9	6 (BL)	7	IO	PB6D	D16	L20C_A0
AK9	6 (BL)	7	IO	PB7B	—	—
U18	—	—	VSS	VSS	—	—
AN8	6 (BL)	7	IO	PB7C	D17	L21T_A0
AM8	6 (BL)	7	IO	PB7D	D18	L21C_A0
AN9	6 (BL)	7	IO	PB8A	—	L22T_D0
AP8	6 (BL)	7	IO	PB8B	—	L22C_D0
AK10	6 (BL)	7	IO	PB8C	VREF_6_07	L23T_A0
AL10	6 (BL)	7	IO	PB8D	D19	L23C_A0
AP9	6 (BL)	8	IO	PB9B	—	—
U19	—	—	VSS	VSS	—	—
AM10	6 (BL)	8	IO	PB9C	D20	L24T_A0
AM11	6 (BL)	8	IO	PB9D	D21	L24C_A0
AK11	6 (BL)	8	IO	PB10B	—	—
AN10	6 (BL)	8	IO	PB10C	VREF_6_08	L25T_A0
AP10	6 (BL)	8	IO	PB10D	D22	L25C_A0
AN11	6 (BL)	9	IO	PB11A	—	L26T_A0
AP11	6 (BL)	9	IO	PB11B	—	L26C_A0
V16	—	—	VSS	VSS	—	—
AL12	6 (BL)	9	IO	PB11C	D23	L27T_A0
AK12	6 (BL)	9	IO	PB11D	D24	L27C_A0
AN12	6 (BL)	9	IO	PB12A	—	L28T_A0

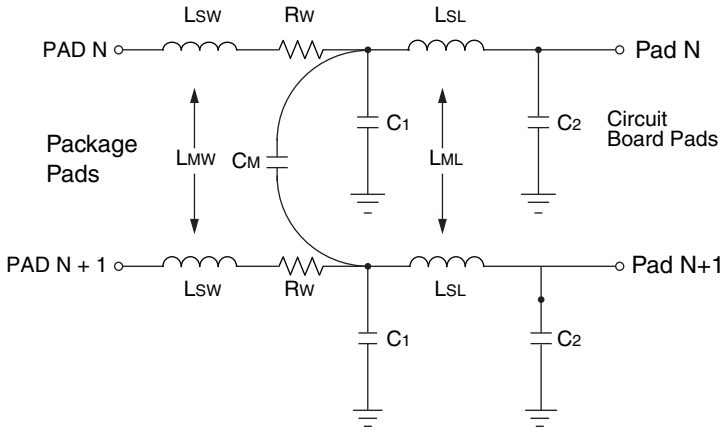
Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
B29	1 (TC)	8	IO	PT33D	—	L1C_A0
C29	1 (TC)	8	IO	PT33C	VREF_1_08	L1T_A0
B15	1 (TC)	—	VDDIO1	VDDIO1	—	—
E27	1 (TC)	8	IO	PT32D	—	L2C_A0
E26	1 (TC)	8	IO	PT32C	—	L2T_A0
AP34	—	—	Vss	Vss	—	—
A30	1 (TC)	8	IO	PT32B	—	—
A29	1 (TC)	9	IO	PT31D	—	L3C_D3
E25	1 (TC)	9	IO	PT31C	VREF_1_09	L3T_D3
B17	1 (TC)	—	VDDIO1	VDDIO1	—	—
E24	1 (TC)	9	IO	PT31A	—	—
B28	1 (TC)	9	IO	PT30D	—	L4C_A0
C28	1 (TC)	9	IO	PT30C	—	L4T_A0
B2	—	—	Vss	Vss	—	—
D28	1 (TC)	9	IO	PT30A	—	—
C27	1 (TC)	9	IO	PT29D	—	L5C_A0
D27	1 (TC)	9	IO	PT29C	—	L5T_A0
E23	1 (TC)	9	IO	PT29B	—	L6C_A0
E22	1 (TC)	9	IO	PT29A	—	L6T_A0
D26	1 (TC)	1	IO	PT28D	—	L7C_A0
D25	1 (TC)	1	IO	PT28C	—	L7T_A0
B33	—	—	Vss	Vss	—	—
D24	1 (TC)	1	IO	PT28B	—	L8C_A0
D23	1 (TC)	1	IO	PT28A	—	L8T_A0
C26	1 (TC)	1	IO	PT27D	VREF_1_01	L9C_A0
C25	1 (TC)	1	IO	PT27C	—	L9T_A0
D11	1 (TC)	—	VDDIO1	VDDIO1	—	—
E21	1 (TC)	1	IO	PT27B	—	L10C_A0
E20	1 (TC)	1	IO	PT27A	—	L10T_A0
D22	1 (TC)	2	IO	PT26D	—	L11C_A0
D21	1 (TC)	2	IO	PT26C	VREF_1_02	L11T_A0
E34	—	—	Vss	Vss	—	—
A28	1 (TC)	2	IO	PT26B	—	—
B26	1 (TC)	2	IO	PT25D	—	L12C_A0
B25	1 (TC)	2	IO	PT25C	—	L12T_A0
D13	1 (TC)	—	VDDIO1	VDDIO1	—	—
B27	1 (TC)	2	IO	PT25B	—	—
A27	1 (TC)	3	IO	PT24D	—	L13C_A0
A26	1 (TC)	3	IO	PT24C	VREF_1_03	L13T_A0
N13	—	—	Vss	Vss	—	—
C24	1 (TC)	3	IO	PT24B	—	—
C22	1 (TC)	3	IO	PT23D	—	L14C_A0
C23	1 (TC)	3	IO	PT23C	—	L14T_A0
D15	1 (TC)	—	VDDIO1	VDDIO1	—	—

Table 54. ORCA Typical Package Parasitics

L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
3.8	1.3	250	1.0	1.0	0.3	2.8-5	0.5 -1

Figure 53. Package Parasitics



Package Outline Drawings

Package Outline Drawings for the 484-ball PBGAM (fpBGA) used for the ORSO42G5 and 680-ball PBGAM (fpBGA) used for the ORSO82G5 are available at the Package Diagrams section of the Lattice Semiconductor web site at www.latticesemi.com.

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Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
July 2008	08.0	BM680 conversion to F680 per PCN#09A-08.