Lattice Semiconductor Corporation - ORSO42G5-2BMN484I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso42g5-2bmn484i

- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- Supplemental Logic and Interconnect Cell (SLIC) provides eight 3-statable buffers, up to a 10-bit decoder, and *PAL*™-like AND-OR-Invert (AOI) in each programmable logic cell.
- New 200 MHz embedded block-port RAM blocks,
  2 read ports, 2 write ports, and 2 sets of byte lane enables. Each embedded RAM block can be configured as:
  - 1—512 x 18 (block-port, two read/two write) with optional built in arbitration.
  - 1—256 x 36 (dual-port, one read/one write).
  - 1—1K x 9 (dual-port, one read/one write).
  - 2—512 x 9 (dual-port, one read/one write for each).
  - 2 RAMS with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - Supports joining of RAM blocks.
  - Two 16 x 8-bit Content Addressable Memory (CAM) support.
  - FIFO 512 x 18, 256 x 36, 1Kx 9, or dual 512 x 9.
  - Constant multiply (8 x 16 or 16 x 8).
  - Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, MicroProcessor Interface (MPI), embedded RAM blocks, and embedded standard cell blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.
- Built-in testability:
  - Full boundary scan (*IEEE* 1149.1 and Draft 1149.2 JTAG).
  - Programming and readback through boundary scan port compliant to *IEEE* Draft 1532:D1.7.
  - TS_ALL testability function to 3-state all I/O pins.
  - New temperature-sensing diode.
- Improved built-in clock management with Programmable Phase-Locked Loops (PPLLs) provide optimum clock modification and conditioning for phase, frequency, and duty cycle from 15 MHz up to 420 MHz. Multiplication of the input frequency up to 64x and division of the input frequency down to 1/64x possible.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also enables compliance with many setup/hold and clock to out I/O specifications and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.
- PCI local bus compliant for FPGA I/Os.

Programmable Logic System Features

- Improved *PowerPC*® 860 and *PowerPC* II high-speed synchronous MicroProcessor Interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard cell blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space provided.
- New embedded system bus facilitates communication among the MicroProcessor Interface, configuration logic, Embedded Block RAM, FPGA logic, and embedded standard cell blocks.
- Variable size bused readback of configuration data with the built-in MicroProcessor Interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew.
- New local clock routing structures allow creation of localized clock trees.
- Two new edge clock routing structures allow up to six high-speed clocks on each edge of the device for improved

ispLEVER Development System

The ispLEVER development system is used to process a design from a netlist to a configured FPGA. This system is used to map a design onto the *ORCA* architecture, and then place and route it using ispLEVER development system timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

FPSC Design Kit

Development is facilitated by an FPSC design kit which, together with ispLEVER and third-party synthesis and simulation engines, provides all software and documentation required to design and verify an FPSC implementation. Included in the kit are the FPSC configuration manager and/or complied *Verilog* simulation model, *HSPICE* and/or IBIS models for I/O buffers, and complete online documentation. The kit's software couples with ispLEVER, providing a seamless FPSC design environment.

ORSO82G5/42G5 FPGA Logic Overview

The following sections provide a brief overview of the main architectural features of the ORSO82G5/42G5 FPGA logic. For more detailed information, refer to the ORCA Series 4 FPGA Data Sheet which can be found on the Lattice web site at www.latticesemi.com. The ORCA Series 4 FPGA Data Sheet provides detailed information required for designing with the ORSO82G5/42G5 device. Topics covered in the ORCA Series 4 Data Sheet include:

- FPGA Logic Architecture
- FPGA Routing Resources
- FPGA Clock Routing Resources
- FPGA Programmable Input/Output Cells (PICs)
- FPGA Embedded Block RAM (EBR)
- Microprocessor Interface (MPI)
- Phase-Locked Loops (PLLs)
- Electrical Characteristics
- FPGA Timing Characteristics
- Power-up
- Configuration

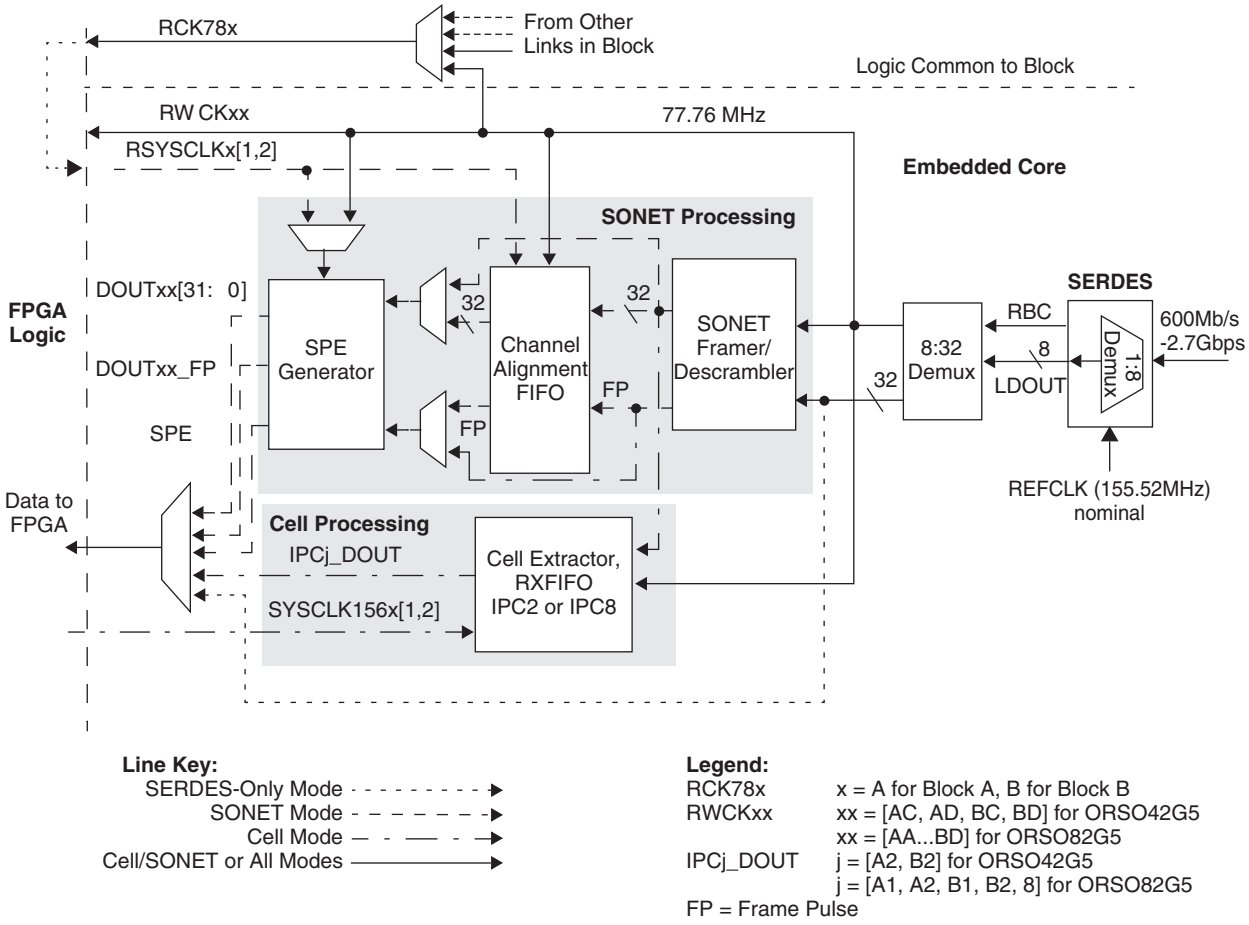
ORCA Series 4 FPGA Logic Overview

The *ORCA* Series 4 architecture is a new generation of SRAM-based programmable devices from Lattice. It includes enhancements and innovations geared toward today's high-speed systems on a single chip. Designed with networking applications in mind, the Series 4 family incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* Series 4 devices contain many new patented enhancements and are offered in a variety of packages and speed grades.

The hierarchical architecture of the logic, clocks, routing, RAM, and system-level blocks create a seamless merge of FPGA and ASIC designs. Modular hardware and software technologies enable system-on-chip integration with true plug-and-play design implementation.

The architecture consists of four basic elements: Programmable Logic Cells (PLCs), programmable I/O cells (PIOs), Embedded Block RAMs (EBRs), and system-level features. These elements are interconnected with a rich routing fabric of both global and local wires. An array of PLCs are surrounded by common interface blocks which provide an abundant interface to the adjacent PLCs or system blocks. Routing congestion around these critical blocks is eliminated by the use of the same routing fabric implemented within the programmable logic core. Each PLC contains a PFU, SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PIOs provide

Figure 4. Top Level Overview, RX Path Logic, Single Channel



In either the SONET or cell mode, data from the DEMUX is then passed through a framer which word aligns and frames the data. Data are then processed based on cell mode or SONET mode selection.

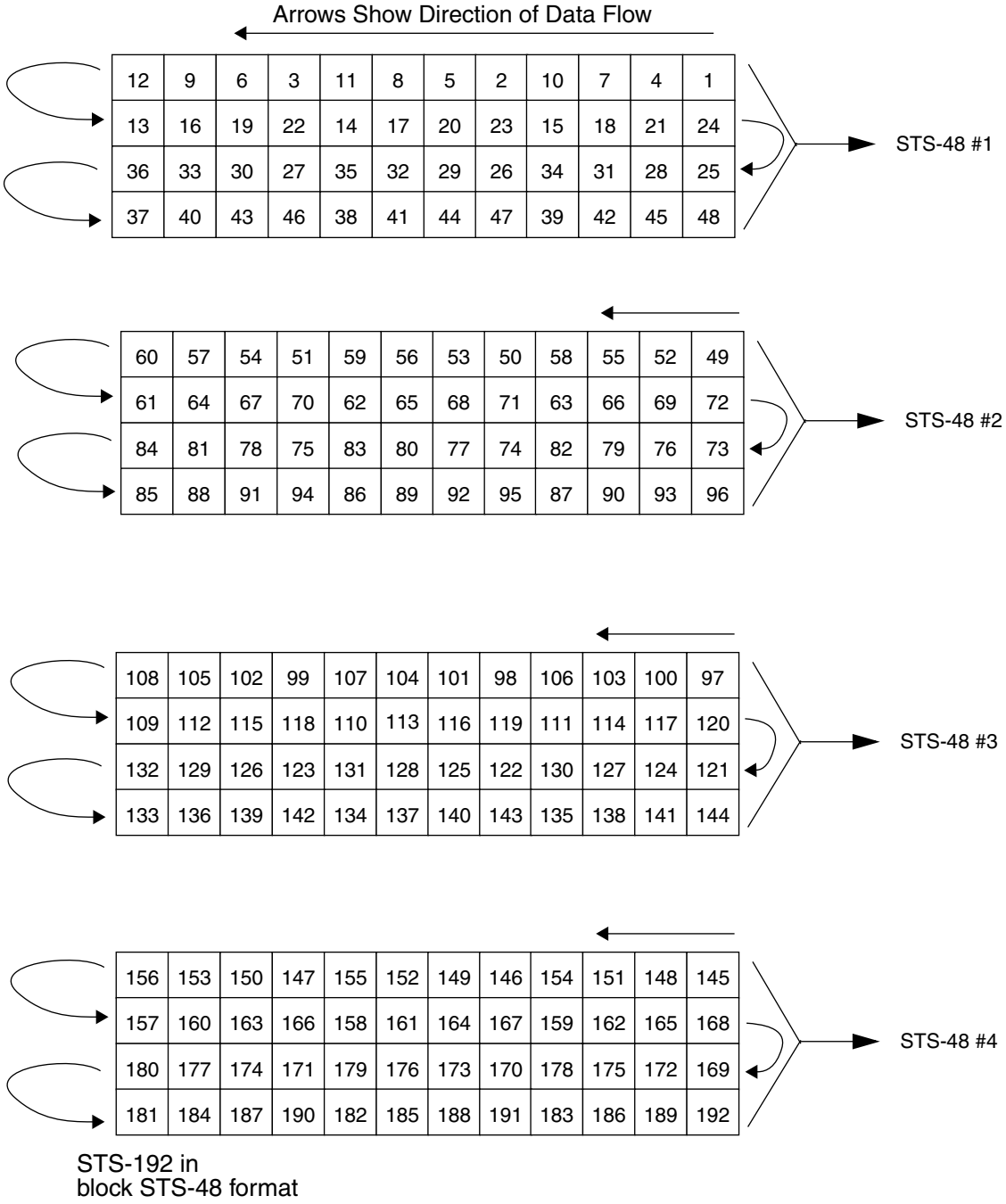
In the SONET mode, the descrambled data are sent to an alignment FIFO that performs lane-to-lane deskew and optionally aligns data within a multi-channel alignment group. In addition, supervisory features such as BIP error check, OOF check, RDI monitoring and AIS-L insertion during OOF are also implemented. All the supervisory features are controlled through programmable register bits.

In the cell mode, the framed data are then descrambled and passed into a cell extractor which extracts cells from the payload portion of the SONET frame. The cells are passed through a FIFO that performs lane-to-lane deskew and a clock domain transfer from 77.76 MHz to 155.52 MHz. A key feature in cell mode is the ability to use idle cell insertion and deletion for automatic rate matching between the clock domains. The cells are then passed to the IPC2 block (or, in the ORSO82G5, to the IPC8 block) which perform cell destriping before sending the cells to the FPGA logic across the Core/FPGA interface.

SERDES Transmit and Receive PLLs

The high-speed transmit and receive serial data can operate at 0.6 to 2.7 Gbps depending on the state of the control bits from the system bus. Table 2 shows the relationship between the data rates, the reference clock, and the internal transmit TCK78x clocks.

Figure 14. Byte Ordering of Input/Output Interface in STS-192 (Block STS-48) Mode



ORSO42G5 Configuration

At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

- Setting bit 1 to one in registers at locations 30002, 30012, 30102 and 30112 powers down the legacy logic. (Note that the reset value for these bits is 0.)
- Setting bit 1 to zero (reset condition) in the register at locations 30802, 30812, 30902 and 30912 removes the legacy logic from any alignment group.

Register settings for SONET multi-channel alignment are shown in Table 7.

Table 7. Multichannel Alignment Modes – ORSO42G5

Register Bits FMPU_SYNMODE_xx[2:3]	Mode
00	No multichannel alignment
01	Twin channel alignment
11	Four channel alignment

Note: xx = [AC,AD,BC,BD]

To align two channels in SERDES A:

- FMPU_SYNMODE_AC = 01 (Register Location 30822)
- FMPU_SYNMODE_AD = 01 (Register Location 30832)

To align two channels in SERDES B:

- FMPU_SYNMODE_BC = 01 (Register Location 30922)
- FMPU_SYNMODE_BD = 01 (Register Location 30932)

To align all four channels:

- FMPU_SYNMODE_AC = 11 (Register Location 30822)
- FMPU_SYNMODE_AD = 11 (Register Location 30832)
- FMPU_SYNMODE_BC = 11 (Register Location 30922)
- FMPU_SYNMODE_BD = 11 (Register Location 30932)

To enable/disable multi-channel alignment of individual channels within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled

where xx = [AC,AD,BC,BD]

To resynchronize a multichannel alignment group set the following bits to one, and then set to zero:

- FMPU_RESYNC4 for four channels, AC, AD, BC and BD. (Register Location 30A04, bit 7)
- FMPU_RESYNCA2 for dual channels, AC and AD. (Register Location 30A04, bit 2)
- FMPU_RESYNCB2 for dual channels, BC and BD. (Register Location 30A04, bit 5)

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bits to one, and then set to zero.

- FMPU_RESYNC1_xx (Register Locations 30824, 20834, 30924 and 30934, bit 7) where xx is one of AC, AD, BC or BD.

Link Header Detector

The Link Header detector determines when the next Link Header is coming in the frame and what the sequence number contained within it should be. If the value of the cell sequence counter is not equal to the expected value, then an error flag bit will set in the status registers and an error signal will be sent to the FPGA logic. The sequence counter will increment to the next sequence number. The sequence count value is NOT updated with the incorrect value, but is incremented each time a Link Header is received.

If excessive sequence errors are detected (three or more in a row), and the AUTO_REMOVE_[A:B] register bit is set, then the corresponding link will be treated as not valid. The RX_LINK_GOOD status bit will go low indicating the link is no longer receiving cells. If the AUTO_REMOVE_[A:B] register bit is not set, then the link is still valid when excessive sequence errors are detected. An OOF condition will also trigger the link to be removed from service if the AUTO_REMOVE_[A:B] register bit is set.

At startup or after a link has been removed from service (indicated by RX_LINK_GOOD going low), a link can be rejoined into the group. This is performed via the per block REJOIN_[A:B] register bit. When rejoining a link the RX FIFO will begin receiving cells. To cleanly rejoin a link into a group there are two methods to insure the RX FIFO begins loading correctly. The first method is to use the fast framing mode during the rejoin process. The can be done by setting the FFRM_EN_xx for the links that need to be rejoined before setting the REJOIN_[A:B] bit.

The second method is to issue a block reset to clear the FIFO once all links that have been selected to be rejoined are rejoined. This is done by first setting the REJOIN_[A:B] bit. Once the RX_LINK_GOOD status bit is high for the selected channels the GSWRST_[A:B] for the block should be set and cleared to reset the block. This method will disturb traffic on all links in the block during the GSWRST_[A:B] reset time.

Once all of the links in a group are rejoined and the traffic is again flowing the REJOIN_[A:B] bit should be cleared. If this bit is not cleared, a link may drop out using the AUTO_REMOVE mode and the channel may be rejoined incorrectly, causing errors on the entire group.

Receive FIFO

The main clock domain transfer for the data path is handled by the receive FIFO. A 16 x 161 FIFO is used in cell mode. The FIFO is implemented as a dual-port memory which will support simultaneous reads and writes. The receive FIFO block is written to at 77.76 MHz and read at 156 MHz.

The receive FIFO can allow for inter-link skew of about 800 ns (16 x 160 = 2560 bits, 400 ps per bit gives 1024 ns). The 160 LSBs in the memory are received data and the 161st bit indicates the start of a new cell. The FIFO write control logic indicates to the IPC, the start of a new frame of data. This signal will only be active for the A1 word of a frame.

Once frame synchronization has occurred and the IPC has responded with a FIFO enable signal, data will be written into the memory. Only the payload (cells) is written to the FIFO. The TOH bytes are not written into the FIFO. The cell octets immediately following the A1A2 bytes will be always written to the top of the FIFO.

Once a full cell has been written to the memory, the write control logic will send a control signal to the IPC8 or IPC2 block which will start the process of reading data from the FIFO. The IPC will read one whole cell at a time from each of the 8 FIFO blocks, if configured for the eight-link cell mode (ORSO82G5 only) or from each of 2 FIFO blocks if configured for the two-link cell mode.

A FIFO occupancy counter generates a RX_FIFO_OVRUN indication to the register interface if it detects a FIFO overflow condition. The cell mode allows for alignment of all eight-links or alignment of two-links. Thus there will be two IPC blocks for two pairs of channels per block.

Input Port Controllers

The input port controllers (IPCs) are the block responsible for “directing traffic” for the receive traffic flow. The block diagrams for the 2-link and 8-link IPCs are shown in Figure 44. They provide the following essential functions.

- Determining when cell data can be read from the FIFOs of the individual links.

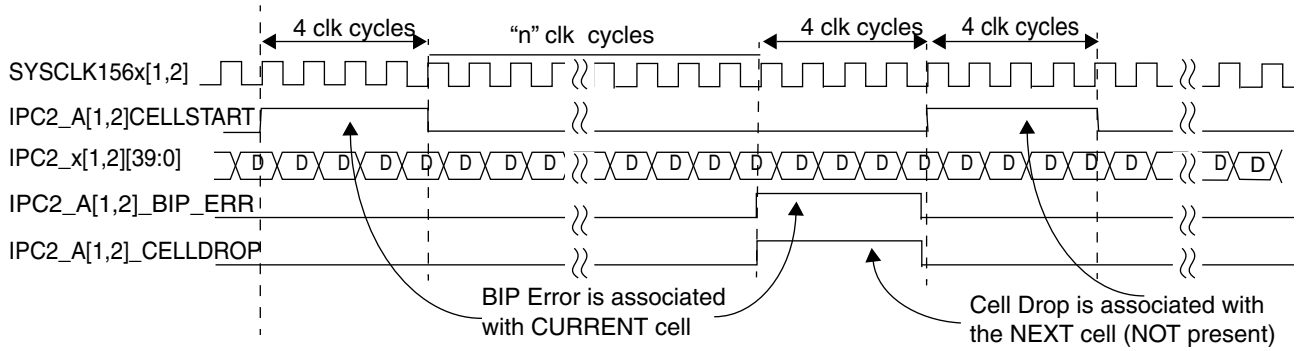
The behavior of the IPC is dependent on the AUTO_BUNDLE register bit. If AUTO_BUNDLE is set, the group will continue to operate even if a link (or several links) of the group is not valid (RX_LINK_GOOD is low). If AUTO_BUNDLE is not set the entire group must be valid (RX_LINK_GOOD is high) for the group to receive cells through the IPC.

The IPC must determine when FIFO reads may begin. Before reading data from a FIFO can begin, the FIFO must have a full cell available to be read. This is condition is indicated by a signal from each FIFO which is monitored by the IPC. The IPC then makes sure that the cells in a given port are received in the order that they are transmitted.

IPC Receive Cell Mode Timing Core/FPGA

This section contains timing diagrams for major interfaces of this block to the FPGA logic when cells are to be transferred. Figure 45 shows the cell twin-link mode timing. The number of clock cycles to transfer the cell data depends on the payload size selected. Error indications for CELL BIP errors and CELL DROP are also shown.

Figure 45. IPC2 Data Flow



CELL BIP ERROR
If a Cell BIP Error occurs,
the CELL_BIP_ERR signal reflects the occurrence, as shown in the Figure.
For 2-Link CELL MODE,
the CELL_BIP_ERR signal is asserted during the last 4 clock cycles of the receive cell.

CELL BIP ERROR
If a cell error occurs within the ASB and;
1. CELL_BIP_INH=0 ...Do not drop BIP errored cells (s/w selectable)
2. A BIP error occurs

The drop indicator will PRECEED the user cell that contains the BIP error. All data will be passed w/o modification.

When operating in CELL MODE, the IPC2 Block passes user cells as well as control and status signals to the user. Depending upon the configured CELL SIZE, cell transfers will take a variable number of SYSCLK156 cycles to be received across the interface. Data are always transferred across a 40-bit bus (5 octets per clock cycle). Figure 45 shows 16 clock cycles for a cell transfer. This corresponds to a User Cell size of 79 octets.

Figure 46 shows cell octal alignment mode timing for the ORSO82G5. When operating in CELL MODE, the IPC8 Block aligns all 8 channels of receive data on a FRAME basis. The IPC8 also passes user cells as well as control and status signals to the user. Depending upon the configured CELL SIZE, cell transfers will take a variable number of SYSCLK156 cycles to be received across the interface. Data are always transferred across an 160-bit bus (20 octets per clock cycle). Figure 46 shows 4 clock cycles for a cell transfer. This corresponds to a User Cell size of 79 octets.

TCK156[A:B]: This is a muxed output from the core to the FPGA across the core-FPGA interface of one of the 4 transmit SERDES clocks per block. There is one clock output per SERDES block. It is derived from REFCLK_[A:B] and runs at the reference clock frequency.This clock is available from the core in all modes and used by the core in cell mode.

TCK78[A:B]: This is a muxed output from the core to the FPGA across the core-FPGA interface of one of the 4 transmit SERDES clocks per block. There is one clock output per SERDES block. It is derived from REFCLK_[A:B] and runs at half the reference clock frequency. This clock is available from the core in all modes and used by the core in SONET and SERDES-only mode.

TCK39[A:B]: This is a muxed output from the core to the FPGA across the core-FPGA interface of one of the 4 transmit SERDES clocks per block. There is one clock output per SERDES block. It is derived from REFCLK_[A:B] and runs at a quarter of the reference clock frequency. This clock is available from the core in all modes.

TSYSCLK[AA,…BD]: These clocks are inputs to the SERDES block A and B respectively from the FPGA. These are used by each channel to control the timing of the Transmit Data Path in the SONET and SERDES-only modes. (They are not used in cell mode.) To guarantee correct transmit operation theses clocks must be frequency locked within 0 ppm to TCK78[A:B].

SYSCLK156 [A:B][1:2] and SYSCLK156 8: These clocks are inputs to the SERDES block A and B from the FPGA. and are used by the cell processing blocks within the embedded core. Clocks SYSCLK156 A[1:2] are used by channels in the SERDES block A and SYSCLK156 B[1:2] by channels in the SERDES block B for two-link cell mode operation. SYSCLK156 8 is used by both blocks for eight-link cell mode in the ORSO82G5.

Sample Initialization Sequences – ORSO42G5

The following paragraphs show sample control register write sequences for initialization and resynchronization for the major modes of the device. Hexadecimal values will be shown for the data to be written into the control registers. For these values bit 0 will be the MSb while bit 7 is the LSb. For the per-channel control registers, only the first register address is shown. The other per-channel control registers must also be initialized for the desired mode.

1. SERDES-Only Mode Initialization – ORSO42G5

- Set SERDES Only mode (per channel, channel AA selected for sample initialization)
  - 30823 and 30833 40
- Set SERDES PLL to Lock to Data signal (per channel, channel AA selected for sample initialization)
  - 30824 and 30834 80
- Toggle SOFT_RESET once all clocks have stabilized
  - 30A06 01
  - 30A06 00
- Provide a rising edge on the DINxx_START signal

2. SONET Mode Initialization – ORSO42G5

This sample initialization uses the alignment FIFO for two channel alignment and Auto_SOH mode

- Set Dual Channel Alignment (per channel, channels AC and AD)
  - 30822 and 30833 10
- Set SERDES PLL to Lock to Data signal (per channel, channels AC and AD)
  - 30824 and 30834 80
- Set Auto_SOH Mode (per channel, channels AC and AD)
  - 30826 and 30836 03

Table 24. SERDES Per Channel Configuration Registers (Read/Write) – ORSO42G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
SERDES Per Channel Transmit and Receive Channel Configuration Registers (Read/Write) xx = [AC, AD, BC, BD]					
30024 - AC 30034 - AD 30124 - BC 30134 - BD	[0]	RSVD	40	Reserved	—
	[1]	MASK_xx		Transmit and Receive Alarm Mask Bit, Channel xx. When MASK_xx = 1, the transmit and receive alarms of a channel are prevented from generating an alarm (i.e., they are masked or disabled). The MASK_xx bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK_xx = 1 on device reset.	Both
	[2]	SWRST_xx		Transmit and Receive Software Reset Bit, Channel xx. When SWRST_xx = 1, this bit provides the same function as the hardware reset, except that all configuration register settings are unaltered. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. SWRST = 0 on device reset.	Both
	[3:6]	RSVD		Reserved	—
	[7]	TESTEN_xx		Transmit and receive Test Enable Bit, Channel xx. When TESTEN_xx = 1, the transmit and receive sections of channel xx are place in test mode. The TESTMODE_xx bits (30006, 30106, etc.) must be set to specify the desired test. The GTESTEN_[A:B] bits override the individual TESTEN_xx settings.	Both
30026-AC 30036-AD 30126-BC 30136-BD	[0]	TESTMODE_xx	00	SERDES Test Mode Select, channel xx. TESTMODE_xx = 0 selects Near End Loopback (CML TX to CML RX internally) TESTMODE_xx = 1 selects Far End Loopback (CML RX to CML TX internally)	Factory Test
	[1:7]	RSVD		Reserved, Set to zero (default).	—

Table 33. SERDES Per-Block Control Register Descriptions – ORSO82G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
SERDES Per-Block Control Register (Read/Write) xx = [AA,...,BD]					
30005 - A 30105 - B	[0]	RSVD	44	Reserved	—
	[1]	GMASK_[A:B]		Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of all channel in the SERDES block are prevented from generating an alarm (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset.	Both
	[2]	GSWRST_[A:B]		Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of all four channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset.	Both
	[3]	GPWRDNT_[A:B]		Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for all four channels are powered down. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset.	Both
	[4]	GPWRDNR_[A:B]		Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for all four channels are powered down. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset.	Both
	[5:6]	RSVD		Reserved	—
	[7]	GTESTEN_[A:B]		Global Test Enable Bit. When GTESTEN_[A:B] = 1, the transmit and receive sections of all channels in the block are place in test mode. The TESTMODE_xx bits (30006, 30106, etc.) must be set to specify the desired test on a per-channel basis. The GTESTEN_[A:B] bits override the individual TESTEN_xx settings.	Factory

Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A05	[0:2]	ERRCNT_CH	00	Error Count Channel Select, Control bits to select which channel's Section B1 error and Cell BIP error counts are recorded by the BIP_ERR_CNT and CELL_BIP_ERR_CNT registers. "000" - Channel AA, "001" - Channel AB, "010" - Channel AC, "011" - Channel AD, "100" - Channel BA, "101" - Channel BB, "110" - Channel BC, "111" - Channel BD	Both
	[3]	CELL_MODE_A1		Cell Mode Enable, CELL_MODE_A1 = 1 enables cell mode for the channel group AA and AB.	Cell
	[4]	CELL_MODE_A2		Cell Mode Enable, CELL_MODE_A2 = 1 enables cell mode for the channel group AC and AD.	Cell
	[5]	CELL_MODE_B1		Cell Mode Enable, CELL_MODE_B1 = 1 enables cell mode for the channel group BA and BB.	Cell
	[6]	CELL_MODE_B2		Cell Mode Enable, CELL_MODE_B2 = 1 enables cell mode for the channel group BC and BD.	Cell
	[7]	CELL_MODE_ALL		Cell Mode Enable, CELL_MODE_ALL = 1 enables cell mode for 8-link cell mode. CELL_MODE_[A1,A2,B1,B2] bits are not valid.	Cell
30A06	[0:4]	RSVD	00	Reserved	—
	[5:6]	RESET_PHASE		Reset Phase, Two bits to select delay phase for delaying the soft reset bit SOFT_RESET with respect to the synchronizing clock. Four delay phases can be selected through the values "00", "01", "10" and "11".	Both
	[7]	SOFT_RESET		Soft Reset, SOFT_RESET=1 resets the embedded core flip flops except for the software registers. This bit does not affect the state of the registers inside the SERDES blocks.	Both
30A07	[0:6]	RSVD	00	Reserved	—
	[7]	TX_CFG_DONE		Transmitter Configuration Done, Edge sensitive bit to indicate that all TX configuration bits are set. After all register bits have been set for Transmit direction, write a 0 and then a 1 to this bit.	Cell

Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A0D	[0]	RSVD	00	Reserved	—
	[1]	SYNC4_B_OVFL		SYNC8_OOS = 1 indicates that the alignment FIFO(s) in the links in block B are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[2]	SYNC2_B2_OVFL		SYNC2_B2_OVFL = 1 indicates that the alignment FIFO(s) in the links BC and BD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[3]	SYNC2_B1_OVFL		SYNC2_B1_OVFL = 1 indicates that the alignment FIFO(s) in the links BA and BB are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[4]	SYNC4_A_OVFL		SYNC4_A_OVFL = 1 indicates that the alignment FIFO(s) in the links in block A are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[5]	SYNC2_A2_OVFL		SYNC2_A2_OVFL = 1 indicates that the alignment FIFO(s) in the links AC and AD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[6]	SYNC2_A1_OVFL		SYNC2_A1_OVFL = 1 indicates that the alignment FIFO(s) in the links AA and AB are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[7]	SYNC8_OVFL		SYNC8_OVFL = 1 Indicates that the alignment FIFO(s) in eight-links are near overflow (At the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
30A0E	[0:2]	RSVD	00	Reserved	—
	[3]	BDL_ALIGN_ERR_B2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs BC and BD	Cell
	[4]	BDL_ALIGN_ERR_B1		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs BA and BB	Cell
	[5]	BDL_ALIGN_ERR_A2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs AC and AD	Cell
	[6]	BDL_ALIGN_ERR_A1		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs AA and AB	Cell
	[7]	BDL_ALIGN_ERR_ALL8		BDL_ALIGN_ERR_ALL8 = 1 -indicates that an alignment error has occurred in cell group of all eight-links	Cell

High Speed Data Receiver

Table 43 specifies receiver parameters measured on devices with worst case process parameters and over the full range of operation conditions.

Table 43. External Data Input Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Data					
Stream of Nontransitions	Scrambler off	—		72	Bits
Sensitivity (differential), worst-case[1]	2.7Gbps	80		—	mVp-p
Input Levels[2]	—	V_{SS} - 0.3	—	V_{DD_ANA} + 0.3	V
Internal Buffer Resistance (Each input to VDDIB)	—	40	50	60	Ω
PLL Lock Time[3]	—	—	—	Note 2	—

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Input level min + (input peak to peak swing)/2 ≤ common mode input voltage ≤ input level max - (input peak to peak swing)/2
3. The ORT82G5 SERDES receiver performs four levels of synchronization on the incoming serial data stream, providing first bit, then byte (character), then channel (32-bit word), and finally optional multi-channel alignment as described in TN1025. The PLL Lock Time is the time required for the CDR PLL to lock to the transitions in the incoming high-speed serial data stream. If the PLL is unable to lock to the serial data stream, it instead locks to REFCLK to stabilize the voltage-controlled oscillator (VCO), and periodically switches back to the serial data stream to again attempt synchronization.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type. Table 44 shows receiver specifications with 10 MHz sinusoidal jitter injection. Other jitter tolerance measurements were measured in a separate experiment detailed in technical note TN1032, *SERDES Test Chip Jitter,* and are not reflected in these results.

Table 44. Receiver Sinusoidal Jitter Tolerance Specifications

Parameter	Conditions	Max.	Unit
Input Data			
Jitter Tolerance @ 2.7Gbps, Typical	600 mV diff eye[1]	0.75	UIP-P
Jitter Tolerance @ 2.7Gbps, Worst case	600 mV diff eye[1]	0.65	UIP-P
Jitter Tolerance @ 2.5Gbps,Typical	600 mV diff eye[1]	0.79	UIP-P
Jitter Tolerance @ 2.5Gbps, Worst case	600 mV diff eye[1]	0.67	UIP-P

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply. Jitter measured with a Wavecrest SIA-3000.

Table 47. Pin Descriptions (Continued)

Symbol	I/O	Description
MPI_ACK	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_CLK	I	This is the PowerPC synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the Embedded System Bus. If MPI is used this will be the AMBA bus clock.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_TEA	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_RTRY	O	This pin requests the MPC860 to relinquish the bus and retry the cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
D[0:31]	I/O	Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	O	D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.[1]
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.[1]
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.[1]
TESTCFG (ORSO82G5 only)	I	During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user programmable I/O pin.[1]

1. The FPGA States of Operation section in the ORCA Series 4 FPGAs data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

This section describes device I/O signals to/from the embedded core.

Table 48. FPSC Function Pin Descriptions

Symbol	I/O	Description
Common Signals for Both SERDES Block A and B		
PASB_RESETN	I	Active low reset for the embedded core.[1]
PASB_TRISTN	I	Active low 3-state for embedded core output buffers.[1]
PASB_PDN	I	Active low power down of all SERDES blocks and associated I/Os.[1]
PASB_TESTCLK	I	Clock input for BIST and loopback test (factory only).[1]
PBIST_TEST_ENN	I	Selection of PASB_TESTCLK input for BIST test (factory only).[1]
PLOOP_TEST_ENN	I	Digital only loopback from TX to RX (factory only).[1]
PMP_TESTCLK	I	Clock input for microprocessor in test mode (factory only).[1]
PMP_TESTCLK_ENN	I	Selection of PMP_TESTCLK in test mode (factory only).[1]
PSYS_DOBISTN	I	Input to start BIST test (factory only).[1]
PSYS_RSSIG_ALL	O	Output result of BIST test (factory only).
SERDES Block A and B Pins		
REFCLKN_A	I	CML reference clock input—SERDES block A.
REFCLKP_A	I	CML reference clock input—SERDES block A.
REFCLKN_B	I	CML reference clock input—SERDES block B.
REFCLKP_B	I	CML reference clock input—SERDES block B.
REXT_A	—	Reference resistor—SERDES block A.
REXT_B	—	Reference resistor—SERDES block B.
REXTN_A	—	Reference resistor – SERDES block. A 3.32 K W ± 1% resistor must be connected across REXT_B and REXTN_B. This resistor should handle a current of 300 µA.
REXTN_B	—	Reference resistor—SERDES block B. A 3.32 K Ω ± 1% resistor must be connected across REXT_B and REXTN_B. This register should handle a current of 300 µA
HDINN_AA	I	High-speed CML receive data input—SERDES block A, channel A (not available in ORSO42G5).
HDINP_AA	I	High-speed CML receive data input—SERDES block A, channel A (not available in ORSO42G5).
HDINN_AB	I	High-speed CML receive data input—SERDES block A, channel B (not available in ORSO42G5).
HDINP_AB	I	High-speed CML receive data input—SERDES block A, channel B (not available in ORSO42G5).
HDINN_AC	I	High-speed CML receive data input—SERDES block A, channel C.
HDINP_AC	I	High-speed CML receive data input—SERDES block A, channel C.
HDINN_AD	I	High-speed CML receive data input—SERDES block A, channel D.
HDINP_AD	I	High-speed CML receive data input—SERDES block A, channel D.
HDINN_BA	I	High-speed CML receive data input—SERDES block B, channel A.
HDINP_BA	I	High-speed CML receive data input—SERDES block B, channel A (not available in ORSO42G5).
HDINN_BB	I	High-speed CML receive data input—SERDES block B, channel B (not available in ORSO42G5).
HDINP_BB	I	High-speed CML receive data input—SERDES block B, channel B (not available in ORSO42G5).
HDINN_BC	I	High-speed CML receive data input—SERDES block B, channel C (not available in ORSO42G5).
HDINP_BC	I	High-speed CML receive data input—SERDES block B, channel C.
HDINN_BD	I	High-speed CML receive data input—SERDES block B, channel D.
HDINP_BD	I	High-speed CML receive data input—SERDES block B, channel D.
SERDES Block A and B Pins		
HDOUTN_AA	O	High-speed CML transmit data output—SERDES Block A, channel A (not available in ORSO42G5).
HDOUTP_AA	O	High-speed CML transmit data output—SERDES Block A, channel A (not available in ORSO42G5).

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
G16	-	-	VDD15	VDD15	-	-
H13	-	-	VSS	VSS	-	-
AB10	5 (BC)	2	IO	PB19A	-	L37T
AA10	5 (BC)	2	IO	PB19B	-	L37C
W10	5 (BC)	2	IO	PB19C	PBCK0T	L38T
Y10	5 (BC)	2	IO	PB19D	PBCK0C	L38C
V10	5 (BC)	2	IO	PB20A	-	-
U13	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB11	5 (BC)	2	IO	PB20C	VREF_5_02	L39T
AA11	5 (BC)	2	IO	PB20D	-	L39C
U10	5 (BC)	2	IO	PB21A	-	-
H6	-	-	VDD15	VDD15	-	-
Y11	5 (BC)	3	IO	PB21C	-	L40T
W11	5 (BC)	3	IO	PB21D	VREF_5_03	L40C
U11	5 (BC)	3	IO	PB22A	-	-
J7	-	-	VSS	VSS	-	-
AB12	5 (BC)	3	IO	PB22C	-	L41T
AA12	5 (BC)	3	IO	PB22D	-	L41C
U12	5 (BC)	3	IO	PB23A	-	-
Y12	5 (BC)	3	IO	PB23C	PBCK1T	L42T
W12	5 (BC)	3	IO	PB23D	PBCK1C	L42C
V11	5 (BC)	3	IO	PB24A	-	-
J8	-	-	VSS	VSS	-	-
AB13	5 (BC)	4	IO	PB24C	-	L43T
AA13	5 (BC)	4	IO	PB24D	-	L43C
V12	5 (BC)	4	IO	PB25A	-	-
U14	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB14	5 (BC)	4	IO	PB25C	-	L44T
AA14	5 (BC)	4	IO	PB25D	VREF_5_04	L44C
J9	-	-	VSS	VSS	-	-
Y13	5 (BC)	5	IO	PB26C	-	L45T
W13	5 (BC)	5	IO	PB26D	VREF_5_05	L45C
U15	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB15	5 (BC)	5	IO	PB27C	-	L46T
AA15	5 (BC)	5	IO	PB27D	-	L46C
AB16	5 (BC)	6	IO	PB28C	-	L47T
AA16	5 (BC)	6	IO	PB28D	VREF_5_06	L47C
H14	-	-	VDD15	VDD15	-	-
Y14	5 (BC)	6	IO	PB29C	-	L48T
W14	5 (BC)	6	IO	PB29D	-	L48C
J10	-	-	VSS	VSS	-	-
AB17	5 (BC)	7	IO	PB30C	-	L49T
AA17	5 (BC)	7	IO	PB30D	-	L49C
U16	5 (BC)	-	VDDIO5	VDDIO5	-	-

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AA15	—	—	VSS	VSS	—	—
L4	0 (TL)	10	IO	PL11B	—	—
N5	7 (CL)	1	IO	PL12D	A15/PPC_A29	L1C_D0
M4	7 (CL)	1	IO	PL12C	A14/PPC_A28	L1T_D0
AA3	7 (CL)	—	VDDIO7	VDDIO7	—	—
L3	7 (CL)	1	IO	PL12B	—	L2C_D0
K2	7 (CL)	1	IO	PL12A	—	L2T_D0
H1	7 (CL)	1	IO	PL13D	VREF_7_01	L3C_A0
J1	7 (CL)	1	IO	PL13C	D4	L3T_A0
V18	—	—	VSS	VSS	—	—
N4	7 (CL)	2	IO	PL13B	—	L4C_D0
P5	7 (CL)	2	IO	PL13A	—	L4T_D0
M3	7 (CL)	2	IO	PL14D	RDY/BUSY_N/RCLK	L5C_D0
L2	7 (CL)	2	IO	PL14C	VREF_7_02	L5T_D0
AC2	7 (CL)	—	VDDIO7	VDDIO7	—	—
K1	7 (CL)	2	IO	PL14B	—	L6C_A0
L1	7 (CL)	2	IO	PL14A	—	L6T_A0
P4	7 (CL)	2	IO	PL15D	A13/PPC_A27	L7C_A0
P3	7 (CL)	2	IO	PL15C	A12/PPC_A26	L7T_A0
V19	—	—	VSS	VSS	—	—
M2	7 (CL)	2	IO	PL15B	—	L8C_A0
M1	7 (CL)	2	IO	PL15A	—	L8T_A0
N2	7 (CL)	3	IO	PL16D	—	L9C_A0
N1	7 (CL)	3	IO	PL16C	—	L9T_A0
N3	7 (CL)	—	VDDIO7	VDDIO7	—	—
R4	7 (CL)	3	IO	PL16B	—	—
P2	7 (CL)	3	IO	PL17D	A11/PPC_A25	L10C_D0
R3	7 (CL)	3	IO	PL17C	VREF_7_03	L10T_D0
W16	—	—	VSS	VSS	—	—
R5	7 (CL)	3	IO	PL17B	—	—
P1	7 (CL)	3	IO	PL18D	—	L11C_A0
R1	7 (CL)	3	IO	PL18C	—	L11T_A0
T5	7 (CL)	3	IO	PL18B	—	L12C_A0
T4	7 (CL)	3	IO	PL18A	—	L12T_A0
T3	7 (CL)	4	IO	PL19D	RD_N/MPI_STRB_N	L13C_A0
T2	7 (CL)	4	IO	PL19C	VREF_7_04	L13T_A0
W17	—	—	VSS	VSS	—	—
U1	7 (CL)	4	IO	PL19B	—	L14C_A0
T1	7 (CL)	4	IO	PL19A	—	L14T_A0
U4	7 (CL)	4	IO	PL20D	PLCK0C	L15C_A0
U5	7 (CL)	4	IO	PL20C	PLCK0T	L15T_A0
R2	7 (CL)	—	VDDIO7	VDDIO7	—	—
U2	7 (CL)	4	IO	PL20B	—	L16C_D0
V1	7 (CL)	4	IO	PL20A	—	L16T_D0

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
B24	1 (TC)	3	IO	PT23B	—	—
D20	1 (TC)	3	IO	PT22D	—	L15C_A0
D19	1 (TC)	3	IO	PT22C	—	L15T_A0
N14	—	—	Vss	Vss	—	—
E19	1 (TC)	3	IO	PT22B	—	L16C_A0
E18	1 (TC)	3	IO	PT22A	—	L16T_A0
C21	1 (TC)	4	IO	PT21D	—	L17C_A0
C20	1 (TC)	4	IO	PT21C	—	L17T_A0
A25	1 (TC)	4	IO	PT21B	—	L18C_A0
A24	1 (TC)	4	IO	PT21A	—	L18T_A0
B23	1 (TC)	4	IO	PT20D	—	L19C_A0
A23	1 (TC)	4	IO	PT20C	—	L19T_A0
N15	—	—	Vss	Vss	—	—
E17	1 (TC)	4	IO	PT20B	—	L20C_A0
E16	1 (TC)	4	IO	PT20A	—	L20T_A0
B22	1 (TC)	4	IO	PT19D	—	L21C_A0
B21	1 (TC)	4	IO	PT19C	VREF_1_04	L21T_A0
C18	1 (TC)	4	IO	PT19B	—	L22C_A0
C19	1 (TC)	4	IO	PT19A	—	L22T_A0
N20	—	—	Vss	Vss	—	—
A22	1 (TC)	5	IO	PT18D	PTCK1C	L23C_A0
A21	1 (TC)	5	IO	PT18C	PTCK1T	L23T_A0
N21	—	—	Vss	Vss	—	—
D17	1 (TC)	5	IO	PT18B	—	L24C_A0
D18	1 (TC)	5	IO	PT18A	—	L24T_A0
B20	1 (TC)	5	IO	PT17D	PTCK0C	L25C_A0
B19	1 (TC)	5	IO	PT17C	PTCK0T	L25T_A0
A20	1 (TC)	5	IO	PT17B	—	L26C_A0
A19	1 (TC)	5	IO	PT17A	—	L26T_A0
A18	1 (TC)	5	IO	PT16D	VREF_1_05	L27C_A0
B18	1 (TC)	5	IO	PT16C	—	L27T_A0
Y21	—	—	Vss	Vss	—	—
C17	1 (TC)	5	IO	PT16B	—	L28C_D0
D16	1 (TC)	5	IO	PT16A	—	L28T_D0
A17	1 (TC)	6	IO	PT15D	—	L29C_D0
B16	1 (TC)	6	IO	PT15C	—	L29T_D0
E15	1 (TC)	6	IO	PT15B	—	L30C_A0
E14	1 (TC)	6	IO	PT15A	—	L30T_A0
A16	1 (TC)	6	IO	PT14D	—	L31C_A0
A15	1 (TC)	6	IO	PT14C	VREF_1_06	L31T_A0
Y22	—	—	Vss	Vss	—	—
D14	1 (TC)	6	IO	PT14B	—	—
C16	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L1C_A0
C15	0 (TL)	1	IO	PT13C	MPI_ACK_N	L1T_A0

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L19C_A0
B4	0 (TL)	6	IO	PT2C	PLL_CK1T/PPLL	L19T_A0
A4	0 (TL)	6	IO	PT2B	—	L20C_A0
A3	0 (TL)	6	IO	PT2A	—	L20T_A0
D5	—	—	O	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	—
E6	—	—	IO	PCCLK	CCLK	—
D4	—	—	IO	PDONE	DONE	—
E5	—	—	VDD33	VDD33	—	—
AB15	—	—	Vss	Vss	—	—
AL33	—	—	VDD15	VDD15	—	—
AL34	—	—	VDD15	VDD15	—	—
AM34	—	—	VDD15	VDD15	—	—
AN34	—	—	VDD15	VDD15	—	—
B34	—	—	VDD15	VDD15	—	—
C33	—	—	VDD15	VDD15	—	—
C34	—	—	VDD15	VDD15	—	—
D33	—	—	VDD15	VDD15	—	—
D34	—	—	VDD15	VDD15	—	—
E32	—	—	VDD15	VDD15	—	—
E33	—	—	VDD15	VDD15	—	—
F32	—	—	VDD15	VDD15	—	—
F34	—	—	VDD15	VDD15	—	—
N16	—	—	VDD15	VDD15	—	—
N17	—	—	VDD15	VDD15	—	—
N18	—	—	VDD15	VDD15	—	—
N19	—	—	VDD15	VDD15	—	—
P16	—	—	VDD15	VDD15	—	—
P17	—	—	VDD15	VDD15	—	—
P18	—	—	VDD15	VDD15	—	—
P19	—	—	VDD15	VDD15	—	—
R16	—	—	VDD15	VDD15	—	—
R17	—	—	VDD15	VDD15	—	—
R18	—	—	VDD15	VDD15	—	—
R19	—	—	VDD15	VDD15	—	—
T13	—	—	VDD15	VDD15	—	—
T14	—	—	VDD15	VDD15	—	—
T15	—	—	VDD15	VDD15	—	—
T20	—	—	VDD15	VDD15	—	—
T21	—	—	VDD15	VDD15	—	—
T22	—	—	VDD15	VDD15	—	—
U13	—	—	VDD15	VDD15	—	—
U14	—	—	VDD15	VDD15	—	—
U15	—	—	VDD15	VDD15	—	—
U20	—	—	VDD15	VDD15	—	—

Industrial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORSO42G5	ORSO42G5-2BM484I	2	PBGAM	484	I
	ORSO42G5-1BM484I	1	PBGAM	484	I
ORSO82G5	ORSO82G5-2F680I	2	PBGAM (No Heat Spreader)	680	I
	ORSO82G5-1F680I	1	PBGAM (No Heat Spreader)	680	I
	ORSO82G5-2BM680I[2]	2	PBGAM (With Heat Spreader)	680	I
	ORSO82G5-1BM680I[2]	1	PBGAM (With Heat Spreader)	680	I

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.
2. BM680 package was converted to F680 via PCN#09A-08.

Lead-Free Packaging

Commercial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORSO42G5	ORSO42G5-3BMN484C	3	Lead-Free PBGAM	484	C
	ORSO42G5-2BMN484C	2	Lead-Free PBGAM	484	C
	ORSO42G5-1BMN484C	1	Lead-Free PBGAM	484	C
ORSO82G5	ORSO82G5-3FN680C	3	Lead-Free FPGA (No Heat Spreader)[2]	680	C
	ORSO82G5-2FN680C	2	Lead-Free FPGA (No Heat Spreader)[2]	680	C
	ORSO82G5-1FN680C	1	Lead-Free FPGA (No Heat Spreader)[2]	680	C

1. For all the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.
2. Refer to the Thermal Management document at www.latticesemi.com for Θ_{JA} and Θ_{JC} information.

Industrial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORSO42G5	ORSO42G5-2BMN484I	2	Lead-Free PBGAM	484	I
	ORSO42G5-1BMN484I	1	Lead-Free PBGAM	484	I
ORSO82G5	ORSO82G5-2FN680I	2	Lead-Free FPGA (No Heat Spreader)[2]	680	I
	ORSO82G5-1FN680I	1	Lead-Free FPGA (No Heat Spreader)[2]	680	I

1. For all the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.
2. Refer to the Thermal Management document at www.latticesemi.com for Θ_{JA} and Θ_{JC} information.