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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso82g5-1f680c

of differential 0.6 to 2.7 Gbit/s links. At the FPGA/Embedded Core interface, the data are transferred across 32-bit buses. The SERDES blocks themselves are organized as two blocks. Each of the data paths is identified with a block and channel identifier (i.e., AC, AD, BC, BD or AA,...,BD).

Each channel has a 32-bit TX bus, 32-bit RX bus, a recovered clock, a transmit clock input and a transmit start signal.

Figure 5. Basic Data Flows - SERDES Only Mode

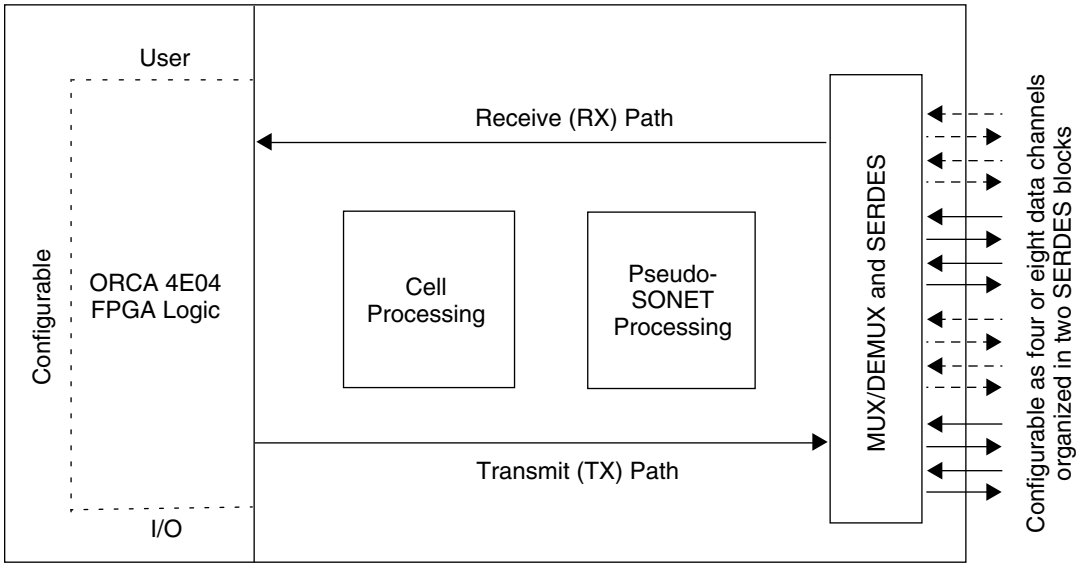
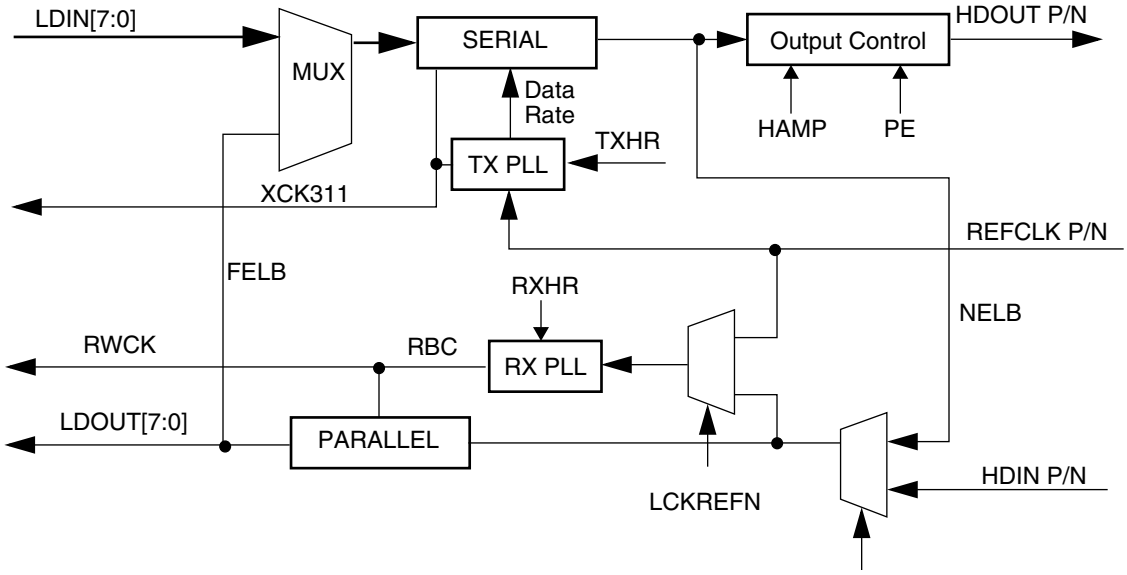


Figure 6 shows a block diagram of a single channel of the SERDES block. The transmitter section accepts either scrambled or un-scrambled data at the parallel input port. It also accepts the low-speed reference clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock. The serialized data are available at the differential CML output terminated in 86 Ω to drive either an optical transmitter, coaxial media or a circuit board/backplane.

Figure 6. SERDES Functional Block Diagram for One Channel



The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. This means that the receive clocks are asynchronous between channels. The retimed data are deserialized and presented as an 8-bit parallel data on the output port. Two-phase receive byte clocks are available synchronous with the parallel words.

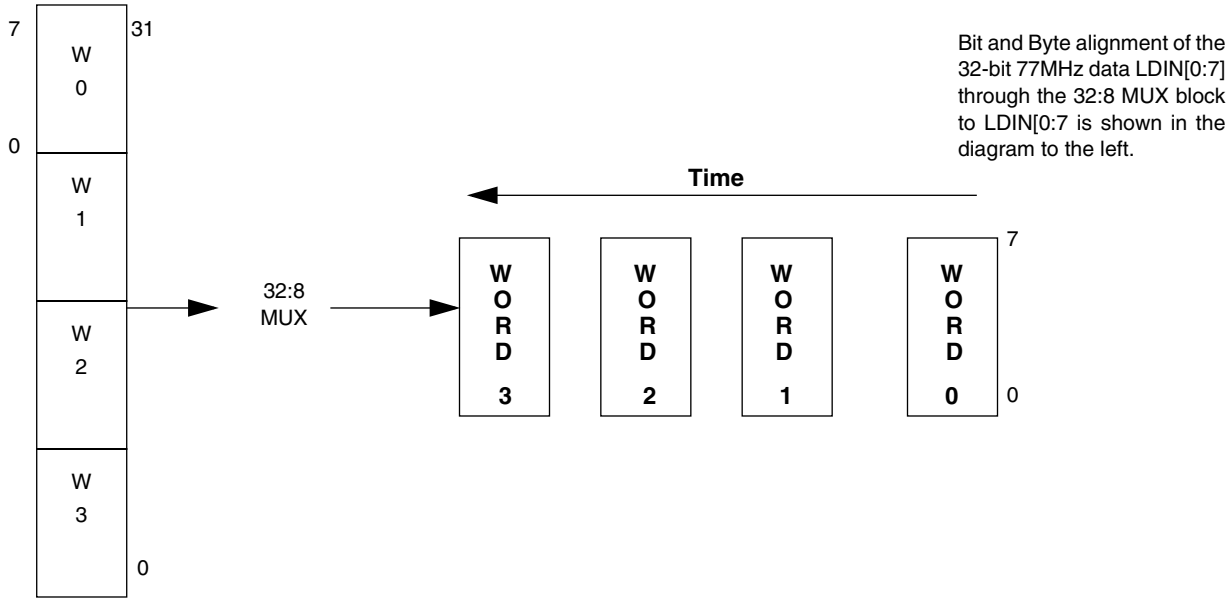
A fractional band-gap voltage generator is included on the design. An external resistor (3.32 kΩ ± 1%), connected between the pins REXT and VSSREXT generates the bias currents within the chip. This resistor should be able to handle at least 300 µA.

32:8 MUX

The MUX block is responsible for converting 32 bits of data at 77.76 MHz to 8 bits of data at 311.04 MHz. It will contain a small elastic store for clock domain transfer between the write clock from the FPGA to the divide-by-4 clock from the SERDES output clock (XCK311). It is recommended to use the clocking scheme shown later in Figure 27, Figure 28 and Figure 29 to guarantee that this elastic store will not be overrun. The 32:8 MUX is also responsible for producing the divide-by-4 clock from the SERDES output clock (XCK311) which is 311.04 MHz at a line rate of 2.488 Gbps.

In the MUX block 32-bit data synchronous to the 77.76 MHz is multiplexed to LDOUTx[7:0] synchronous to the 311.04 MHz SERDES output clock. Parallel 32-bit data can be received directly from the FPGA logic (SERDES only mode) or from the payload sub-block. Bit and byte alignment for the MUX block is shown in Figure 7.

Figure 7. Bit and Byte Alignment for MUX Block



The serialized data are available at the differential CML outputs to drive either an optical transmitter, coaxial media, or circuit board/backplane. The transmitter's CML output buffer is terminated on-chip by 86Ω to optimize the data eye as well as to reduce the number of discrete components required. The differential output swing reaches a maximum of 1.2 VPP in the normal amplitude mode. A half amplitude mode can be selected via configuration register bit HAMP_xx. Half amplitude mode can be used to reduce power dissipation when the transmission medium has minimal attenuation or for testing of the integrity (loss) of the physical medium.

A programmable preemphasis circuit is provided to boost the high frequencies in the transmit data signal to maximize the data eye opening at the far-end receiver. Preemphasis is particularly useful when the data are transmitted over backplanes or low-quality coax cables which have a frequency-dependent amplitude loss. For example, for FR4 material at 2.5 GHz, the attenuation compared to the 1.0 GHz value is about 3 dB. The attenuation is a result of skin effect loss of the PCB conductor and the dielectric loss of the PCB substrate. This attenuation causes intersymbol interface which results in the closing of the data eye at the receiver.

Supported Data Formats

The ORSO42G5 and ORSO82G5 in the SONET mode support the following formats:

- Single OC-48 on each of the channels at a bit rate of 2.488 Gbps.
- OC-192 received in block OC-48 format on four channels at a combined rate of 9.952 Gbps.

The ORSO42G5 and ORSO82G5 SERDES will operate at the OC-12 rate of 622 MHz. For this rate, REFCLK is set to 77 MHz and the SERDES is used in half rate mode. However the embedded core SONET framing/processing logic is fixed at the OC-48 rate and therefore can not talk directly with standard STS-12 devices. In order to interoperate with standard STS-12 devices, the user must bypass the SONET functionality in the ORSO embedded core (SERDES-only mode) and implement all framing, TOH and scrambling/descrambling functionality in FPGA logic.

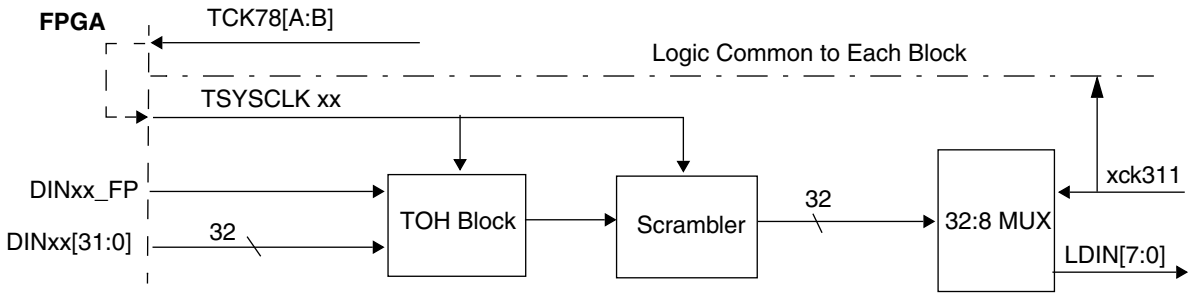
Figure 13 reveals the byte-ordering of the individual STS-48 streams. STS-192 is supported but it must be received in the block STS-48 format as shown in Figure 14. Each OC-48 stream is composed of byte-interleaved OC-1 data as described in GR-253 standard. Note that the SPE data is not touched by the core.

tee that this elastic store will not be overrun. The 32:8 MUX is also responsible for producing the divide-by-4 clock from the SERDES output clock (XCK311) which is 311.04 MHz at a line rate of 2.488 Gbps.

SONET Mode Transmit Timing

Figure 17 shows the transmit clocks and a recommended clocking scheme. As shown, TCK78[A,B] can be used to the source TSYSCLKxx signals. It is a requirement that TSYSCLKxx be frequency locked to the corresponding TCK78[A,B] clock signal derived from REFCLK_[A:B].

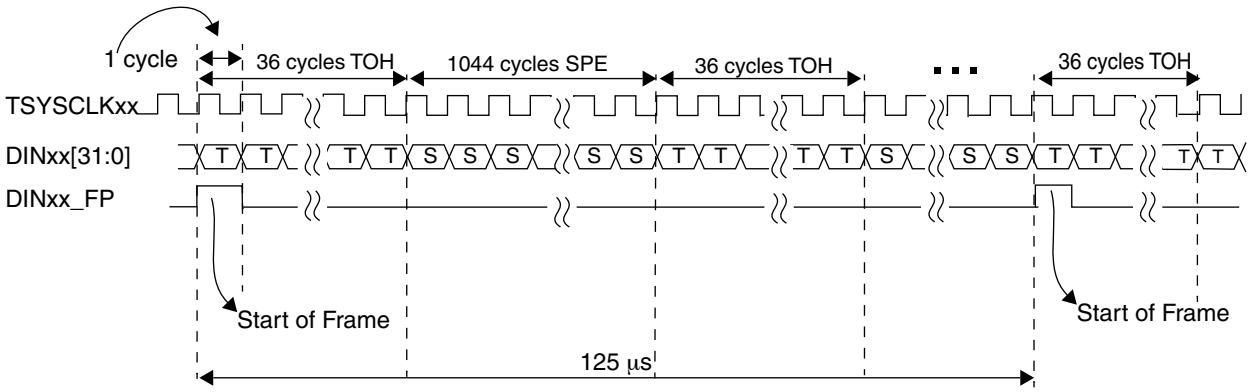
Figure 17. Transmit Clocking Diagram in SONET Mode



xx represents AC, AD, BC, BD (ORSO42G5) or AA, AB, AC, AD, BA, BB, BC, BD (ORSO82G5)

- When operating in SONET mode, the entire SONET frame is sent by the user. Optionally the TOH bytes can be overwritten by the transmit block (AUTO_SOH or AUTO_TOH) before sending to scrambler and SERDES block.
- Each SONET frame is 125 µs given a 155.52MHz reference clock.
- The frame starts with 36 clock cycles (77.76 MHz) of TOH followed by 1044 clock cycles of SPE, followed by 36 clock cycles of TOH, 1044 cycles of SPE etc. for all nine rows.

Figure 18. Transmit SONET Mode



xx represents AC, AD, BC, BD (ORSO42G5) or AA, AB, AC, AD, BA, BB, BC, BD (ORSO82G5).

SONET Mode Receive Path

The receiver block receives a byte from the SERDES blocks for each of the channels. The byte arrives at the receiver block at 311.04 MHz. This data are not frame-aligned or word aligned. The data are first passed through a divide-by-4 DEMUX which produces a 32-bit word at 77.76 MHz. Data from the DEMUX is then passed through a framer which aligns and frames the data. Data are processed based on cell mode or SONET mode.

In the SONET mode, the descrambled data are sent to an alignment FIFO that performs lane-to-lane deskew and aligns data within an alignment group to the RSYCLK clock domain. Both the write and read clocks to the align-

Section (B1) BIP-8 Calculator
The section BIP-8 B1 byte in a given STS-N frame contains the scrambled BIP value for all scrambled bytes of the previous frame. Except for the A1,A2 and J0 section overhead bytes, all bytes in a frame are scrambled. The Section (B1) BIP-8 is calculated as the even parity of all bits in the current STS-48 frame. This value is compared to the Section Overhead B1 byte of the next frame. B1 error counters are available that monitors the number of B1 errors on a per-channel basis. A B1 parity error flag is also generated as a software alarm bit.

Descrambler
The data from the framer is descrambled using the SONET/SDH standard generator polynomial $1 + x^6 + x^7$. The descrambling is performed in parallel on each 32-bit word per channel, synchronized to the frame pulse and can be disabled through the software register bit.

RDI (Remote Defect Indicator) Monitor
The line RDI (RDI-L) is monitored through bits 2-0 of the K2 byte. Within the 32-bit descrambled data, a pattern of "110" on bits 26-24 will indicate a RDI-L status. RDI-L must be detected in two consecutive frames before an RDI alarm register bit is set. If fast_frame_mode is enabled, then the RDI alarm register bit will be set if RDI-L is detected in one frame.

Receive FIFO
Clock domain transfers and multi-link de-skew are one of the most critical parts of this device. The main clock domain transfer for the datapath is handled by the receive FIFO. For each link, there are two FIFOs. A 24 x 33 FIFO is used in SONET mode.

The use of the FIFO is controlled by configuration bits.

- Data can be sent from the descrambler directly to the FPGA bypassing the alignment FIFO. Data from each channel will have an associated clock (RWCKxx at 77.76 MHz). Each channel will also provide a FP and SPE indicator along with the data. Descrambling can be inhibited through the DSCR_INH_xx control bit.
- Data can be sent directly from the 8:32 DEMUX block to the FPGA bypassing the alignment FIFO and SONET framer and descrambler. Data from each channel will have an associated clock. No SPE or FP indicator is provided with the data.

Receive FIFO in SONET mode
The receive FIFO used in SONET mode will allow for an inter-link skew of about 300 ns (24 x 32 = 768 bits, 400 ps per bit gives 307 ns). The FIFO is written at 77.76 MHz and read at 77.76 MHz. Once frame synchronization has occurred, the write control logic will cause data to be written to the memory. The write control block is required to insure that the word containing the first A1 byte is written to the same location (address 0) in the FIFO. The synchronization algorithm issues a sync pulse and sync error signals to the read control block based on the alignment option chosen. This sync pulse will coordinate the reading of the FIFOs.

The read control logic synchronizes the reading of the FIFO for the streams that are to be aligned. The block begins reading when the FIFO sync sub block signals that all of the applicable A1s with the appropriate margin have been written to the FIFO. All of the read blocks to be synchronized begin reading at the same time and same location in the memory (address 0). The block also takes the difference between the write and read address to indicate the relative skews between the links. If this difference exceeds a certain limit (programmable), then an alarm (alignment overflow) is provided to the register interface.

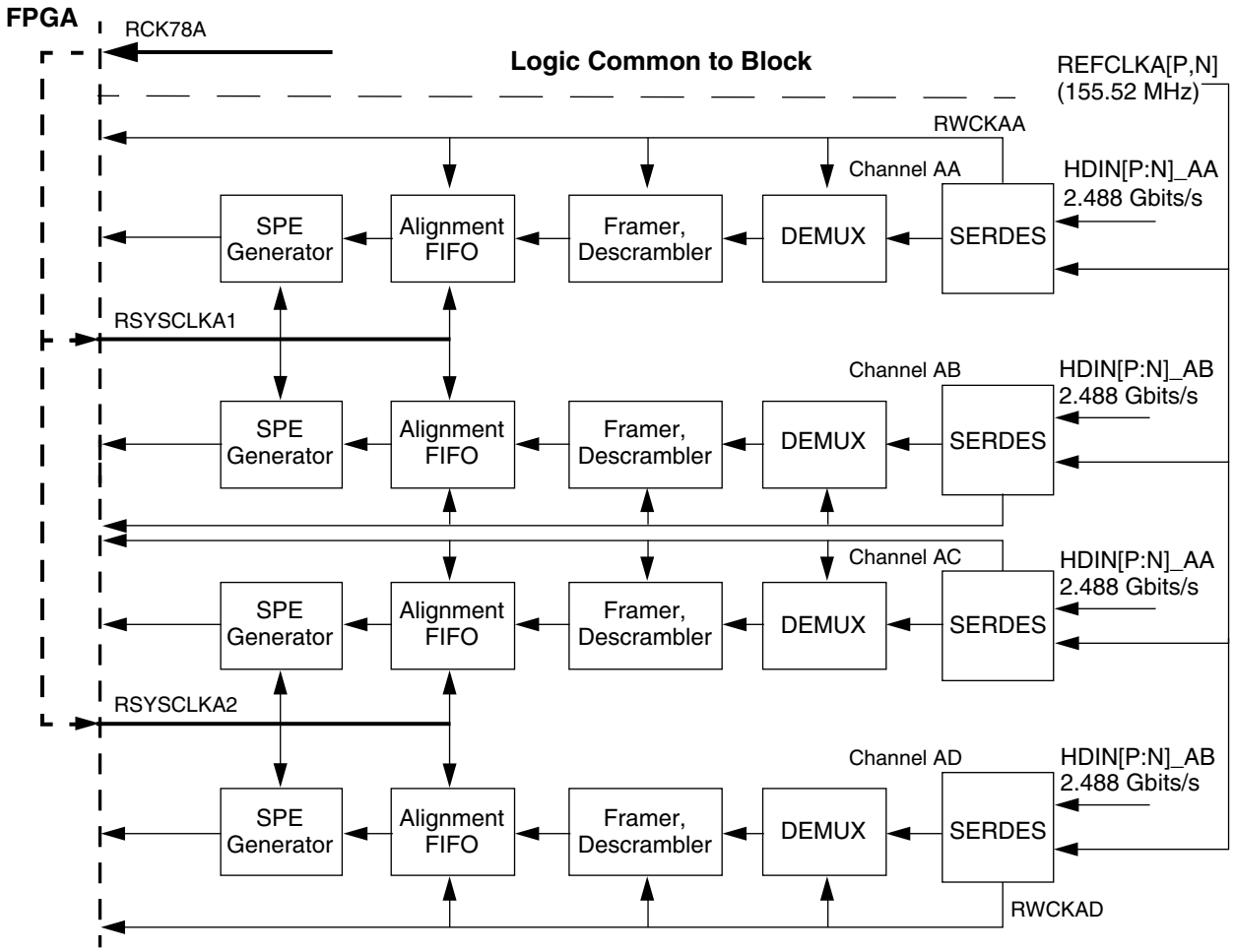
Multi-channel Alignment in SONET Mode – ORSO42G5
The alignment FIFO allows the transfer of all data to a common clock. The FIFO sync block allows the system to be configured to allow the frame alignment of multiple slightly varying data streams. This optional alignment ensures that matching SERDES streams will arrive at the FPGA end in perfect data sync. It is important to note that for all aligned channels in a group, the SERDES transmitters on the other side of the high-speed link must all be transmitting data at exactly the same frequency (0 ppm difference), i.e., using a common clock source.

The ORSO42G5 has a total of four channels (two per SERDES block). The incoming data of these channels can be synchronized in several ways, or they can be independent of one other. Two channels within a SERDES can be

SONET Mode Block Alignment – ORSO82G5

Figure 28 describes the clocks and recommended clocking for block alignment in the SONET mode. For block alignment, the low speed portion for each block should be sourced by a single clock. As the figure shows, for block A, RSYSCLKA1 and RSYSCLKA2 should be sourced by RCK78A. For block B, RSYSCLKB1 and RSYSCLKB2 should be sourced by RCLK78B. RCLK78A can be sourced by any channel in block A and RCLK78B can be sourced by any channel in block B.

Figure 28. Receive Clocking Diagram for Four-Channel Alignment in Block A – ORSO82G5



SONET Mode Octal Alignment – ORSO82G5

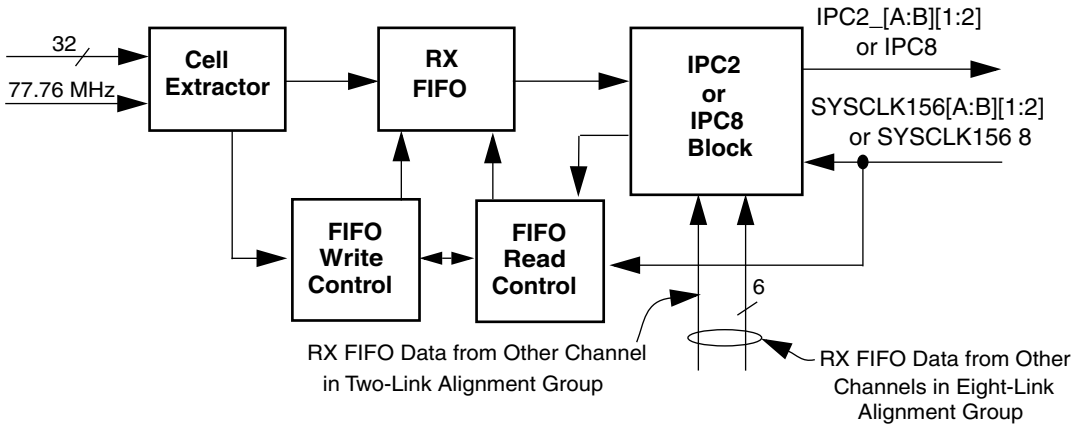
Figure 29 shows the clocking scheme for eight-channel alignment. In this application, all four clocks RSYSCLKA1, RSYSCLKA2, RSYSCLKB1 and RSYSCLKB2 should be sourced from a common clock. Either RCK78A or RCK78B can be used as a common clock source. The figure shows RCK78A being used as the clock source.

Cell Mode Receive Path

The receive logic blocks unique to the cell mode are shown in Figure 43 and are described in the next sections. Prior to reaching this logic the received data has been demultiplexed, frame aligned and descrambled by the SERDES and SONET logic and is formatted on a per channel basis as 32-bit words with an accompanying clock. The clock is a 77.76 MHz clock provided by the DEMUX block performing a divide-by-4 operation on RWCKxx.

The Data Extractor and receive FIFO (RXFIFO) process the data on a per channel basis. The receive FIFO also performs a clock domain transfer to the 156 MHz domain of the Input Port Controller (IPC2/8) blocks. The IPC2/8 blocks perform the two-link or eight-link (ORSO82G5 only) alignment functions. In two-link alignment mode, the received data are passed to the FPGA logic as 40-bit words at the 156 MHz rate. In eight-link alignment mode, the received data are passed to the FPGA logic as a single 160-bit word, again at the 156 MHz rate. Additional mode-dependent status information is also provided across the Core/FPGA interface.

Figure 43. Receive Path Logic Unique to Cell Mode



Cell Extractor

This block is used only in cell mode and does the following:

- Extracts User cells from the SPE
- Performs BIP calculation/checks to verify cell integrity
- Link Header Sequence Interrogation

Processing options include:

- Cell handling for invalid sequence (drop or pass to FPGA)
- S/W configurable ‘link removal’ due to excessive sequence errors

Data from the cell extractor block(s) is sent to the receive FIFO which aligns the data to the system clock domain and provides for deskew between the links.

Cell Extraction and BIP Calculation/Checking

The data from the descrambler are passed into the data extractor which strips the cell data from the payload of a SONET frame. The block extracts the BIP value from the data stream and also perform an internal cell BIP calculation. If the BIP value is not correct, an error flag bit will set in the status registers. The block also determines when the next Link Header is coming in the frame and what the cell sequence number contained within it should be. If the value of the cell sequence counter is not equal to the expected value, an error flag bit will set in the status registers and an error signal will be sent across the core/FPGA interface.

Table 14. RX Core/FPGA Interface Signals – ORSO82G5 (Continued)

33	—		
32	DOUTAB_B1_ERR		
[31:20]	DOUTAB[31:20]]	—	
[19:0]	DOUTAB[19:0]	IPC2_A1[19:0]	IPC8[139:120]
RXDAC[39:0]	SONET mode	IPC2 A2 Mode	IPC8 Mode
39	SYNC2_A2_OOS	—	
38	—	IPC2_A2_CELLDROP	—
37	—	IPC2_A2_CELLSTART	—
36	DOUTAC_FP	—	
35	DOUTAC_OOF		
34	DOUTAC_SPE	—	
33	—	IPC2_A2_CELL_BIP_ERR	—
32	DOUTAC_B1_ERR		
[31:20]	DOUTAC[31:20]]	—	
[19:0]	DOUTAC[19:0]	IPC2_A2[39:20]	IPC8[119:100]
RXDAD[39:0]	SONET Mode	IPC2 A2 Mode	IPC8 Mode
39	—	—	IPC8_CELLDROP
38	—	—	IPC8_CELLSTART
37	—	CELL_BEGIN_OK_A2	—
36	DOUTAD_FP	—	
35	DOUTAD_OOF		
34	DOUTAD_SPE	—	
RXDAD[39:0]	SONET Mode	IPC2 A2 Mode	IPC8 Mode
33	—	—	IPC8_CELL_BIP_ERR
32	DOUTAD_B1_ERR		
[31:20]	DOUTAD[31:20]	—	
[19:0]	DOUTAD[19:0]	IPC2_A2[19:0]	IPC8[99:80]
RXDBA[39:0]	SONET Mode	IPC2 B1 Mode	IPC8 Mode
39	SYNC2_B1_OOS	—	
38	—	IPC2_B1_CELLDROP	—
37	—	IPC2_B1_CELLSTART	—
36	DOUTBA_FP	—	
35	DOUTBA_OOF		
34	DOUTBA_SPE	—	
33	—	IPC2_B1_CELL_BIP_ERR	—
32	DOUTBA_B1_ERR		
[31:20]	DOUTBA[31:20]	—	
[19:0]	DOUTBA[19:0]	IPC2_B1[39:20]	IPC8[79:60]
RXDBB[39:0]	SONET Mode	IPC2 B1 Mode	IPC8 Mode
39	SYNC8_OOS	—	
38	—	—	SDO_BP_8

Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30826 - AC 30836 - AD 30926 - BC 30936 - BD	[0:5]	RSVD	00	Reserved	—
	[6]	AUTO_B1_xx		AUTO_B1_xx = 0, B1 is not inserted by the embedded core AUTO_B1_xx = 1, B1 is calculated and inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	Both
	[7]	AUTO_A1A2_xx		AUTO_A1A2_xx = 0, A1/A2 bytes are not inserted by the embedded core AUTO_A1A2_xx = 1, A1/A2 bytes inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	

Table 34. Per-Channel Control Register Descriptions – ORSO82G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30800 - AA 30810 - AB 30820 - AC 30830 - AD 30900 - BA 30910 - BB 30920 - BC 30930 - BD	[0:4]	RSVD	00	Reserved	—
	[5]	CELL_ALIGN_ERR_EN_xx		'1' = Alarm enabled for CELL_ALIGN_ERR_xx	Cell
	[6]	TX_URUN_ERR_EN_xx		'1' = Alarm enabled for TX_URUN_ERR_xx	Cell
	[7]	TX_ORUN_ERR_EN_xx		'1' = Alarm enabled for TX_ORUN_ERR_xx	Cell
30801 - AA 30811 - AB 30821 - AC 30831 - AD 30901 - BA 30911 - BB 30921 - BC 30931 - BD	[0]	RSVD	00	Reserved	—
	[1]	OOF_EN_xx		'1' = Alarm enabled for OOF_xx	Both
	[2]	EX_SEQ_ERR_EN_xx		'1' = Alarm enabled for EX_SEQ_ERR _xx	Cell
	[3]	SEQ_ERR_EN_xx		'1' = Alarm enabled for SEQ_ERR _xx	Cell
	[4]	CELL_BIP_ERR_EN_xx		'1' = Alarm enabled for CELL_BIP_ERR_xx	Cell
	[5]	B1_ERR_EN_xx		'1' = Alarm enabled for B1_ERR_xx	Both
	[6]	RX_FIFO_OVRUN_EN_xx		'1' = Alarm enabled for RX_FIFO_OVRUN_xx	Cell
	[7]	RDI_EN_xx		'1' = Alarm enabled for RDI_xx	Both
30802 - AA 30812 - AB 30822 - AC 30832 - AD 30902 - BA 30912 - BB 30922 - BC 30932 - BD	[0]	ENABLE_JUST_xx	00	ENABLE_JUST_xx =1 causes the core to interpret pointer bytes for positive or negative justification	SONET
	[1]	FMPU_STR_EN_xx		FMPU_STR_EN_xx = 1 enables a channel for alignment within a multi-channel alignment group	SONET
	[2:3]	FMPU_SYNMODE_xx		"00" - No channel alignment "01" - Twin channel alignment "10" - 4 channel alignment "11 - By-8 alignment	SONET
	[4]	DSCR_INH_xx		Descrambling Inhibit, DSCR_INH = 1 inhibits descrambling (in the Rx direction) and scrambling (in the Tx direction). When inhibiting the scrambler and descrambler the AUTO_B1_xx calculated and checked B1 value will always be incorrect.	Both
	[5]	FFRM_EN_xx		Fast Frame Enable, FFRM_EN=1 enables the fast frame mode.	Both
	[6]	AIS_ON_xx		Alarm Indication Signal (control), AIS_ON =1 forces AIS-L insertion.	Both
	[7]	AIS_ON_OOF_xx		Alarm Indication Signal on Out of Frame, AIS_ON_OOF =1 forces AIS-L insertion during OOF =1.	Both

Input Eye-Mask Characterization

Figure 51 provides an eye-mask characterization of the SERDES receiver input. The eye-mask is specified below for two different eye-mask heights. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance. Almost all detrimental characteristics of transmit signal and the interconnection link design result in eye-closure. This, combined with the eye-opening limitations of the line receiver, can provide a good indication of a link's ability to transfer data error-free.

The Clock and Data Recovery (CDR) portion of the ORSO42G5 and ORSO82G5 SERDES receiver has the ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth (about 3 MHz). The eye-mask specifications of Table 45 are for jitter frequencies above the PLL bandwidth of the CDR, which is a worst case condition. When jitter occurs at frequencies below the PLL bandwidth, the receiver jitter tolerance is significantly better. For this case error-free data detection can occur even with a completely closed eye-mask.

Figure 51. Receive Data Eye-Diagram Template (Differential)

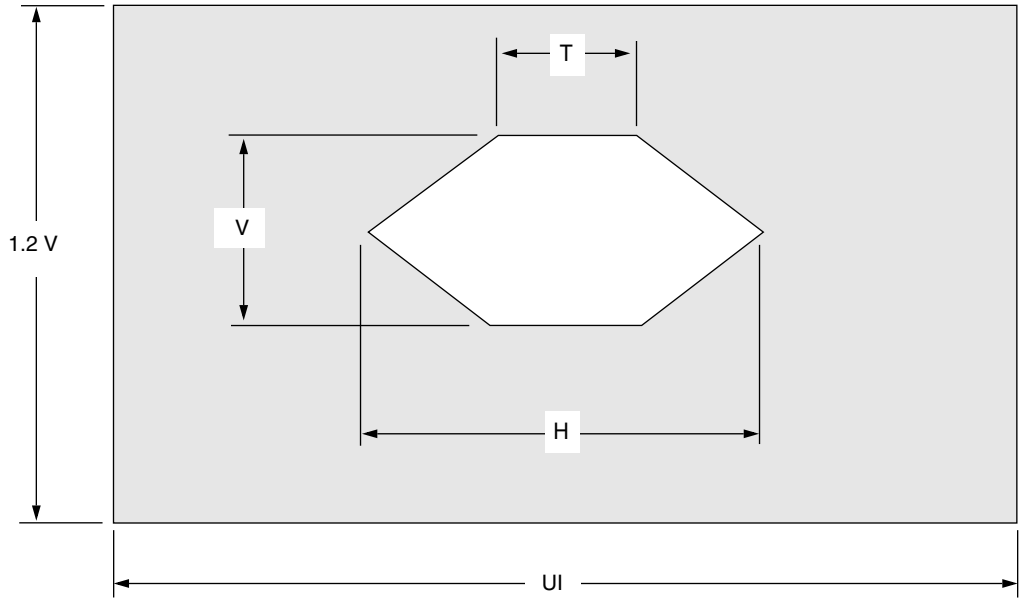


Table 45. Receiver Eye-Mask Specifications[1]

Parameter	Conditions	Value	Unit
Input Data			
Eye Opening Width (H)@ 2.7Gbps	V=175 mV diff[1]	0.55	UIP-P
Eye Opening Width (T)@ 2.7Gbps	V=175 mV diff[1]	0.15	UIP-P
Eye Opening Width (H)@ 2.7Gbps	V=600 mV diff[1]	0.35	UIP-P
Eye Opening Width (T)@ 2.7Gbps	V=600 mV diff[1]	0.10	UIP-P
Eye Opening Width (H)@ 2.5Gbps	V=175 mV diff[1]	0.42	UIP-P
Eye Opening Width (T)@ 2.5Gbps	V=175 mV diff[1]	0.15	UIP-P
Eye Opening Width (H)@ 2.5Gbps	V=600 mV diff[1]	0.33	UIP-P
Eye Opening Width (T)@ 2.5Gbps	V=600 mV diff[1]	0.10	UIP-P

1. With PRBS 2^7-1 data pattern, 10 MHz sinusoidal jitter, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply.

- Example connections are shown in Figure 52. The naming convention for the power supply sources shown in the figure are as follows:
  - Supply_1.5V Tx-Rx digital, auxiliary power pins
  - Supply_VDD_ANA Analog power pins
  - Supply VDDIB Input Rx buffer power pins
  - Supply_VDDOB Output Tx buffer power pins

Figure 52. Power Supply Filtering

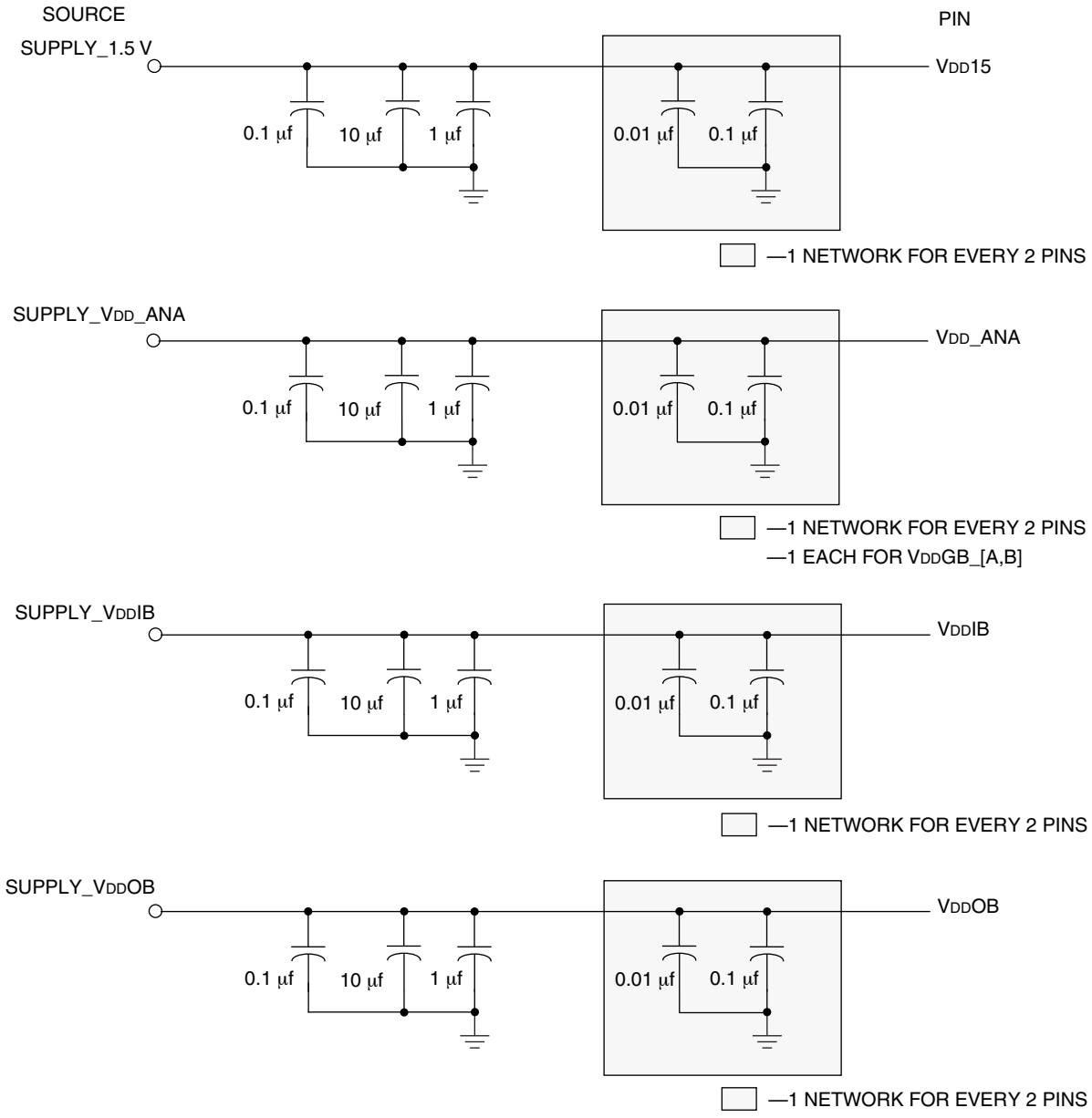


Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
C1	0 (TL)	7	IO	PL2C	PLL_CK0T/HPPLL	L1T
F3	0 (TL)	7	IO	PL3C	VREF_0_07	-
A1	-	-	VSS	VSS	-	-
D2	0 (TL)	7	IO	PL4D	D5	L2C
D1	0 (TL)	7	IO	PL4C	D6	L2T
E7	0 (TL)	-	VDDIO0	VDDIO0	-	-
E2	0 (TL)	8	IO	PL5D	HDC	L3C
E1	0 (TL)	8	IO	PL5C	LDC_N	L3T
G3	0 (TL)	8	IO	PL5A	-	-
G4	0 (TL)	9	IO	PL6C	D7	-
F2	0 (TL)	9	IO	PL7D	VREF_0_09	L4C
F1	0 (TL)	9	IO	PL7C	A17/PPC_A31	L4T
G2	0 (TL)	9	IO	PL8D	CS0_N	L5C
G1	0 (TL)	9	IO	PL8C	CS1	L5T
E8	0 (TL)	-	VDDIO0	VDDIO0	-	-
A2	-	-	VSS	VSS	-	-
H1	0 (TL)	10	IO	PL10D	INIT_N	L6C
H2	0 (TL)	10	IO	PL10C	DOUT	L6T
E5	-	-	VDD15	VDD15	-	-
H4	0 (TL)	10	IO	PL11D	VREF_0_10	-
H3	0 (TL)	10	IO	PL11C	A16/PPC_A30	-
J1	7 (CL)	1	IO	PL12D	A15/PPC_A29	L7C
J2	7 (CL)	1	IO	PL12C	A14/PPC_A28	L7T
J4	7 (CL)	1	IO	PL13C	D4	-
G7	-	-	VSS	VSS	-	-
J3	7 (CL)	2	IO	PL14D	RDY/BUSY_N/RCLK	-
K6	7 (CL)	-	VDDIO7	VDDIO7	-	-
K1	7 (CL)	2	IO	PL15D	A13/PPC_A27	L8C
K2	7 (CL)	2	IO	PL15C	A12/PPC_A26	L8T
K3	7 (CL)	3	IO	PL16C	-	-
K4	7 (CL)	3	IO	PL17D	A11/PPC_A25	-
G8	-	-	VSS	VSS	-	-
F8	-	-	VDD15	VDD15	-	-
K5	7 (CL)	4	IO	PL19D	RD_N/MPI_STRB_N	-
L1	7 (CL)	4	IO	PL20D	PLCK0C	L9C
L2	7 (CL)	4	IO	PL20C	PLCK0T	L9T
L6	7 (CL)	-	VDDIO7	VDDIO7	-	-
F9	-	-	VDD15	VDD15	-	-
G9	-	-	VSS	VSS	-	-
L3	7 (CL)	5	IO	PL21D	A10/PPC_A24	L10C
L4	7 (CL)	5	IO	PL21C	A9/PPC_A23	L10T
L5	7 (CL)	5	IO	PL22D	A8/PPC_A22	-
F10	-	-	VDD15	VDD15	-	-
G10	-	-	VSS	VSS	-	-

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
G19	-	-	VSS	VSS	-	-
R22	-	-	O	HDOUTP_BC	-	HSP_3
P21	-	-	VDDOB	VDDOB_BC	-	-
H16	-	-	VSS	VSS	-	-
P22	-	-	VDDIB	VDDIB_BD	-	-
K17	-	-	VDD_ANA	VDD_ANA	-	-
N22	-	-	I	HDINN_BD	-	HSN_4
H17	-	-	VSS	VSS	-	-
N21	-	-	I	HDINP_BD	-	HSP_4
K18	-	-	VDD_ANA	VDD_ANA	-	-
H18	-	-	VSS	VSS	-	-
K19	-	-	VDD_ANA	VDD_ANA	-	-
P20	-	-	VDDOB	VDDOB_BD	-	-
M22	-	-	O	HDOUTN_BD	-	HSN_5
H19	-	-	VSS	VSS	-	-
M21	-	-	O	HDOUTP_BD	-	HSP_5
N20	-	-	VDDOB	VDDOB_BD	-	-
L16	-	-	VSS	VSS	-	-
L17	-	-	VSS	VSS	-	-
M20	-	-	VDDOB	VDDOB_AD	-	-
L22	-	-	O	HDOUTP_AD	-	HSP_6
L18	-	-	VSS	VSS	-	-
L21	-	-	O	HDOUTN_AD	-	HSN_6
L20	-	-	VDDOB	VDDOB_AD	-	-
N16	-	-	VDD_ANA	VDD_ANA	-	-
L19	-	-	VSS	VSS	-	-
N17	-	-	VDD_ANA	VDD_ANA	-	-
K22	-	-	I	HDINP_AD	-	HSP_7
M16	-	-	VSS	VSS	-	-
K21	-	-	I	HDINN_AD	-	HSN_7
N18	-	-	VDD_ANA	VDD_ANA	-	-
K20	-	-	VDDIB	VDDIB_AD	-	-
M17	-	-	VSS	VSS	-	-
J20	-	-	VDDOB	VDDOB_AC	-	-
J21	-	-	O	HDOUTP_AC	-	HSP_8
M18	-	-	VSS	VSS	-	-
J22	-	-	O	HDOUTN_AC	-	HSN_8
H20	-	-	VDDOB	VDDOB_AC	-	-
N19	-	-	VDD_ANA	VDD_ANA	-	-
M19	-	-	VSS	VSS	-	-
P16	-	-	VDD_ANA	VDD_ANA	-	-
H21	-	-	I	HDINP_AC	-	HSP_9
R16	-	-	VSS	VSS	-	-
H22	-	-	I	HDINN_AC	-	HSN_9

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
P6	-	-	VDD15	VDD15	-	-
A11	1 (TC)	5	IO	PT16D	VREF_1_05	L70C
B11	1 (TC)	5	IO	PT16C	-	L70T
L12	-	-	VSS	VSS	-	-
D9	1 (TC)	6	IO	PT15D	-	L71C
C9	1 (TC)	6	IO	PT15C	-	L71T
G15	1 (TC)	-	VDDIO1	VDDIO1	-	-
B10	1 (TC)	6	IO	PT14D	-	L72C
A10	1 (TC)	6	IO	PT14C	VREF_1_06	L72T
B9	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L73C
A9	0 (TL)	1	IO	PT13C	MPI_ACK_N	L73T
D8	0 (TL)	1	IO	PT12D	M0	L74C
C8	0 (TL)	1	IO	PT12C	M1	L74T
A22	-	-	VSS	VSS	-	-
B8	0 (TL)	2	IO	PT12B	MPI_CLK	L75C
A8	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L75T
C7	0 (TL)	2	IO	PT11D	M2	L76C
D7	0 (TL)	2	IO	PT11C	M3	L76T
E9	0 (TL)	-	VDDIO0	VDDIO0	-	-
E6	0 (TL)	2	IO	PT11A	MPI_TEA_N	-
F6	-	-	VDD15	VDD15	-	-
B7	0 (TL)	3	IO	PT9D	VREF_0_03	L77C
A7	0 (TL)	3	IO	PT9C	-	L77T
A6	0 (TL)	3	IO	PT8D	D0	L78C
B6	0 (TL)	3	IO	PT8C	TMS	L78T
C6	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L79C
D6	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L79T
B1	-	-	VSS	VSS	-	-
A5	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L80C
B5	0 (TL)	4	IO	PT6C	D3	L80T
C5	0 (TL)	5	IO	PT5D	D1	L81C
D5	0 (TL)	5	IO	PT5C	D2	L81T
B2	-	-	VSS	VSS	-	-
A4	0 (TL)	5	IO	PT4D	TDI	L82C
B4	0 (TL)	5	IO	PT4C	TCK	L82T
E10	0 (TL)	-	VDDIO0	VDDIO0	-	-
B22	-	-	VSS	VSS	-	-
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L83C
D4	0 (TL)	6	IO	PT2C	PLL_CK1T/PPLL	L83T
A3	-	-	O	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	-
B3	-	-	IO	PCCLK	CCLK	-
F7	-	-	VDD15	VDD15	-	-
C3	-	-	IO	PDONE	DONE	-
E3	-	-	VDD33	VDD33	-	-

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
P15	-	-	VDD15	VDD15	-	-
R6	-	-	VDD15	VDD15	-	-
R15	-	-	VDD15	VDD15	-	-
T4	-	-	VDD15	VDD15	-	-
W19	-	-	VDD15	VDD15	-	-
Y3	-	-	VDD15	VDD15	-	-
Y19	-	-	VDD15	VDD15	-	-
Y20	-	-	VDD15	VDD15	-	-
T15	-	-	VDD15	VDD15	-	-
T16	-	-	VDD15	VDD15	-	-
U4	-	-	VDD15	VDD15	-	-
T12	-	-	VDD15	VDD15	-	-
T13	-	-	VDD15	VDD15	-	-
T14	-	-	VDD15	VDD15	-	-
T6	-	-	VDD15	VDD15	-	-
T7	-	-	VDD15	VDD15	-	-
T10	-	-	VDD15	VDD15	-	-
T11	-	-	VDD15	VDD15	-	-
G5	0 (TL)	-	VDDIO0	VDDIO0	-	-
H5	0 (TL)	-	VDDIO0	VDDIO0	-	-
J5	0 (TL)	-	VDDIO0	VDDIO0	-	-
V17	5 (BC)	-	VDDIO5	VDDIO5	-	-
W17	5 (BC)	-	VDDIO5	VDDIO5	-	-
W18	5 (BC)	-	VDDIO5	VDDIO5	-	-
M6	7 (CL)	-	VDDIO7	VDDIO7	-	-
N6	7 (CL)	-	VDDIO7	VDDIO7	-	-
U5	-	-	VDD15	VDD15	-	-
U17	-	-	VDD15	VDD15	-	-
V5	-	-	VDD15	VDD15	-	-
V18	-	-	VDD15	VDD15	-	-
R18	-	-	VSS	VSS	-	-
R19	-	-	VSS	VSS	-	-
T19	-	-	VSS	VSS	-	-
U19	-	-	VSS	VSS	-	-
U20	-	-	VSS	VSS	-	-
V19	-	-	VSS	VSS	-	-
V20	-	-	VSS	VSS	-	-
W20	-	-	VSS	VSS	-	-
Y21	-	-	VSS	VSS	-	-
Y22	-	-	VSS	VSS	-	-
L13	-	-	VSS	VSS	-	-
L14	-	-	VSS	VSS	-	-
M8	-	-	VSS	VSS	-	-
M9	-	-	VSS	VSS	-	-

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
W18	—	—	VSS	VSS	—	—
V2	7 (CL)	5	IO	PL21D	A10/PPC_A24	L17C_A0
V3	7 (CL)	5	IO	PL21C	A9/PPC_A23	L17T_A0
W19	—	—	VSS	VSS	—	—
V4	7 (CL)	5	IO	PL21B	—	L18C_A0
V5	7 (CL)	5	IO	PL21A	—	L18T_A0
W4	7 (CL)	5	IO	PL22D	A8/PPC_A22	L19C_A0
W3	7 (CL)	5	IO	PL22C	VREF_7_05	L19T_A0
W1	7 (CL)	5	IO	PL22B	—	L20C_A0
Y1	7 (CL)	5	IO	PL22A	—	L20T_A0
Y2	7 (CL)	5	IO	PL23D	—	L21C_D0
AA1	7 (CL)	5	IO	PL23C	—	L21T_D0
Y13	—	—	VSS	VSS	—	—
Y4	7 (CL)	5	IO	PL23B	—	L22C_A0
Y3	7 (CL)	5	IO	PL23A	—	L22T_A0
Y5	7 (CL)	6	IO	PL24D	PLCK1C	L23C_A0
W5	7 (CL)	6	IO	PL24C	PLCK1T	L23T_A0
U3	7 (CL)	—	VDDIO7	VDDIO7	—	—
AB1	7 (CL)	6	IO	PL24B	—	L24C_D0
AA2	7 (CL)	6	IO	PL24A	—	L24T_D0
AB2	7 (CL)	6	IO	PL25D	VREF_7_06	L25C_D0
AC1	7 (CL)	6	IO	PL25C	A7/PPC_A21	L25T_D0
Y14	—	—	VSS	VSS	—	—
AA4	7 (CL)	6	IO	PL25B	—	—
AB4	7 (CL)	6	IO	PL26D	A6/PPC_A20	L26C_A0
AB3	7 (CL)	6	IO	PL26C	A5/PPC_A19	L26T_A0
W2	7 (CL)	—	VDDIO7	VDDIO7	—	—
AD1	7 (CL)	7	IO	PL26B	—	—
AE1	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	L27C_D0
AD2	7 (CL)	7	IO	PL27C	VREF_7_07	L27T_D0
AC3	7 (CL)	7	IO	PL27B	—	L28C_A0
AC4	7 (CL)	7	IO	PL27A	—	L28T_A0
AF1	7 (CL)	8	IO	PL28D	A4/PPC_A18	L29C_D0
AE2	7 (CL)	8	IO	PL28C	VREF_7_08	L29T_D0
AB5	7 (CL)	8	IO	PL29D	A3/PPC_A17	L30C_A0
AA5	7 (CL)	8	IO	PL29C	A2/PPC_A16	L30T_A0
Y15	—	—	VSS	VSS	—	—
AD3	7 (CL)	8	IO	PL29B	—	—
AG1	7 (CL)	8	IO	PL30D	A1/PPC_A15	L31C_D0
AF2	7 (CL)	8	IO	PL30C	A0/PPC_A14	L31T_D0
AD4	7 (CL)	8	IO	PL30B	—	L32C_D0
AE3	7 (CL)	8	IO	PL30A	—	L32T_D0
AD5	7 (CL)	8	IO	PL31D	DP0	L33C_A0
AC5	7 (CL)	8	IO	PL31C	DP1	L33T_A0

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM12	6 (BL)	9	IO	PB12B	—	L28C_A0
AP12	6 (BL)	9	IO	PB12C	VREF_6_09	L29T_A0
AP13	6 (BL)	9	IO	PB12D	D25	L29C_A0
AM13	6 (BL)	9	IO	PB13A	—	L30T_D0
AN14	6 (BL)	9	IO	PB13B	—	L30C_D0
V17	—	—	VSS	VSS	—	—
AP14	6 (BL)	10	IO	PB13C	D26	L31T_A0
AP15	6 (BL)	10	IO	PB13D	D27	L31C_A0
AK13	6 (BL)	10	IO	PB14A	—	L32T_A0
AK14	6 (BL)	10	IO	PB14B	—	L32C_A0
AM14	6 (BL)	10	IO	PB14C	VREF_6_10	L33T_A0
AL14	6 (BL)	10	IO	PB14D	D28	L33C_A0
AP17	6 (BL)	11	IO	PB15A	—	L34T_A0
AP16	6 (BL)	11	IO	PB15B	—	L34C_A0
AM15	6 (BL)	11	IO	PB15C	D29	L35T_D0
AN16	6 (BL)	11	IO	PB15D	D30	L35C_D0
AM17	6 (BL)	11	IO	PB16A	—	L36T_A0
AM16	6 (BL)	11	IO	PB16B	—	L36C_A0
AP18	6 (BL)	11	IO	PB16C	VREF_6_11	L37T_A0
AP19	6 (BL)	11	IO	PB16D	D31	L37C_A0
AL16	5 (BC)	1	IO	PB17A	—	L1T_D0
AK15	5 (BC)	1	IO	PB17B	—	L1C_D0
N22	—	—	VSS	VSS	—	—
AN18	5 (BC)	1	IO	PB17C	—	L2T_A0
AN19	5 (BC)	1	IO	PB17D	—	L2C_A0
AP20	5 (BC)	1	IO	PB18A	—	L3T_A0
AP21	5 (BC)	1	IO	PB18B	—	L3C_A0
AL17	5 (BC)	1	IO	PB18C	VREF_5_01	L4T_D0
AK16	5 (BC)	1	IO	PB18D	—	L4C_D0
P13	—	—	VSS	VSS	—	—
AM19	5 (BC)	2	IO	PB19A	—	L5T_A0
AM18	5 (BC)	2	IO	PB19B	—	L5C_A0
P14	—	—	VSS	VSS	—	—
AN20	5 (BC)	2	IO	PB19C	PBCK0T	L6T_A0
AM20	5 (BC)	2	IO	PB19D	PBCK0C	L6C_A0
AK17	5 (BC)	2	IO	PB20A	—	L7T_D0
AL18	5 (BC)	2	IO	PB20B	—	L7C_D0
AL11	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP22	5 (BC)	2	IO	PB20C	VREF_5_02	L8T_D0
AN21	5 (BC)	2	IO	PB20D	—	L8C_D0
AM22	5 (BC)	2	IO	PB21A	—	L9T_A0
AM21	5 (BC)	2	IO	PB21B	—	L9C_A0
AP23	5 (BC)	3	IO	PB21C	—	L10T_D0
AN22	5 (BC)	3	IO	PB21D	VREF_5_03	L10C_D0

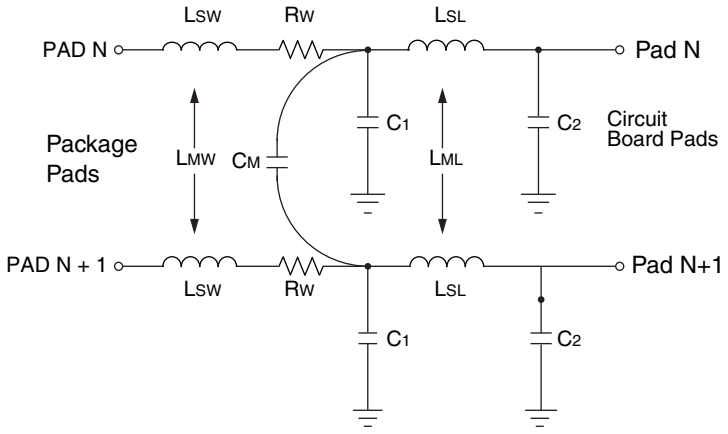
Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
W31	—	—	VSS	VSS	—	—
V30	—	—	VDDOB	VDDOB_BD	—	—
W33	—	—	O	HDOUTN_BD	—	—
H33	—	—	VSS	VSS	—	—
W34	—	—	O	HDOUTP_BD	—	—
V31	—	—	VDDOB	VDDOB_BD	—	—
H34	—	—	VSS	VSS	—	—
J32	—	—	VSS	VSS	—	—
U31	—	—	VDDOB	VDDOB_AD	—	—
T34	—	—	O	HDOUTP_AD	—	—
M32	—	—	VSS	VSS	—	—
T33	—	—	O	HDOUTN_AD	—	—
U30	—	—	VDDOB	VDDOB_AD	—	—
T31	—	—	VSS	VSS	—	—
R34	—	—	I	HDINP_AD	—	—
N32	—	—	VSS	VSS	—	—
R33	—	—	I	HDINN_AD	—	—
T30	—	—	VDDIB	VDDIB_AD	—	—
U32	—	—	VSS	VSS	—	—
R31	—	—	VDDOB	VDDOB_AC	—	—
P34	—	—	O	HDOUTP_AC	—	—
U33	—	—	VSS	VSS	—	—
P33	—	—	O	HDOUTN_AC	—	—
R30	—	—	VDDOB	VDDOB_AC	—	—
P31	—	—	VSS	VSS	—	—
N34	—	—	I	HDINP_AC	—	—
U34	—	—	VSS	VSS	—	—
N33	—	—	I	HDINN_AC	—	—
P30	—	—	VDDIB	VDDIB_AC	—	—
V32	—	—	VSS	VSS	—	—
M34	—	—	O	HDOUTP_AB	—	—
V33	—	—	VSS	VSS	—	—
M33	—	—	O	HDOUTN_AB	—	—
N31	—	—	VDDOB	VDDOB_AB	—	—
M31	—	—	VSS	VSS	—	—
L34	—	—	I	HDINP_AB	—	—
V34	—	—	VSS	VSS	—	—
L33	—	—	I	HDINN_AB	—	—
N30	—	—	VDDIB	VDDIB_AB	—	—
K34	—	—	O	HDOUTP_AA	—	—
K33	—	—	O	HDOUTN_AA	—	—
M30	—	—	VDDOB	VDDOB_AA	—	—
L32	—	—	VDD_ANA	VDD_ANA	—	—
L31	—	—	VSS	VSS	—	—

Table 54. ORCA Typical Package Parasitics

L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
3.8	1.3	250	1.0	1.0	0.3	2.8-5	0.5 -1

Figure 53. Package Parasitics



Package Outline Drawings

Package Outline Drawings for the 484-ball PBGAM (fpBGA) used for the ORSO42G5 and 680-ball PBGAM (fpBGA) used for the ORSO82G5 are available at the Package Diagrams section of the Lattice Semiconductor web site at www.latticesemi.com.