Lattice Semiconductor Corporation - ORSO82G5-1FN680C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso82g5-1fn680c

Embedded Function Features

- High-speed SERDES programmable serial data rates of 0.6 Gbps to 2.7 Gbps.
- Asynchronous operation per receive channel (separate PLL per channel).
- Transmit pre-emphasis (programmable) for improved receive data eye opening.
- Provides a 10 Gbps backplane interface to switch fabric using four work and, with the ORSO82G5, four protect 2.5 Gbit/s links. Also supports port cards at rates between 0.6 Gbps and 2.7 Gbps.
- Allows wide range of applications for SONET network termination, as well as generic data moving for high-speed backplane data transfer.
- No knowledge of SONET/SDH needed in generic applications. Simply supply data (75 MHz-168.75 MHz clock) and at least a single frame pulse.
- High-Speed Interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- Four- or eight-channel HSI functions provide 2.7 Gbps serial user data interface per channel for a total chip bandwidth of >10Gbps or >20 Gbps (full duplex).
- SERDES has low-power CML buffers and support for 1.5V/1.8V I/Os.
- SERDES HSI automatically recovers from loss-of-clock once its reference clock returns to normal operating state.
- Powerdown option of SERDES HSI receiver and/or transmitter on a per-channel basis.
- Ability to mix half-rate and full-rate between the channels with the same reference clock.
- Ability to configure each SERDES block independently with its own reference clock.
- STS-48 framing in SONET mode.
- Programmable enable of SONET scrambler/descrambler, A1/A2 insertion and B1 generation and checking.
- Insertion and checking of link assignment values to facilitate interconnection and debugging of backplanes.
- Optional AIS-L insertion during loss-of-frame.
- Optional RDI-L insertion to indicate remote far-end defects for maintenance capabilities.
- SPE signal marks payload bytes in SONET mode.
- Frame alignment across multiple ORSO42G5 and ORSO82G5 devices for work/protect switching at STS-768/STM-256 and above rates.
- Supports transparent mode where Transport OverHead (TOH) bytes are user-generated in the FPGA.
- Supports two modes of in-band management and configuration with TOH byte extraction/insertion by the Embedded core. A1/A2 and B1 insertion can be independently enabled.
  - AUTO_SOH where the embedded core inserts the A1/A2 framing bytes, performs the B1 calculation and inserts the B1 byte. All other bytes are passed through unchanged from the FPGA logic as in transparent mode.
  - AUTO_TOH where all of the overhead bytes are set by the embedded core. Most of the bytes are set to zero. At the receive side, all of the TOH bytes except those set to a non-zero value can be ignored.
- Optional A1/A2 corruption, B1 byte corruption, and K2 byte corruption for system debug purposes.
- Built-in boundary scan (*IEEE*® 1149.1 and 1149.2 JTAG), including the SERDES interface.
- FIFOs align incoming data across all eight channels (ORSO82G5 only), groups of four channels, or groups of two channels. Optional ability to bypass alignment FIFOs for asynchronous operation between channels is also provided. (Each channel includes its own recovered clock and frame pulse).

- Optional cell processing blocks included. Cell processing includes cell creation, extraction, idle cell insertion and deletion asynchronous from line rates. Four cell sizes supported:
  - 77 bytes per cell (75 bytes of data payload)
  - 81 bytes per cell (79 bytes of data payload)
  - 85 bytes per cell (83 bytes of data payload)
  - 93 bytes per cell (91 bytes of data payload)
- Automatic cell striping across either pairs of SERDES links or, for the ORSO82G5, all eight SERDES links.
- Addition of two 4K X 36 dual-port RAMs accessible by the programmable logic.

Programmable Features

- High-performance programmable logic:
  - 0.16 µm 7-level metal technology.
  - Internal performance of >250 MHz.
  - Over 400K usable system gates.
  - Meets multiple I/O interface standards.
  - 1.5V operation (30% less power than 1.8V operation) translates to greater performance.
- Traditional I/O selections:
  - LVTTL (3.3V) and LVCMOS (2.5V, and 1.8V) I/Os.
  - Per pin-selectable I/O clamping diodes provide 3.3V PCI compliance.
  - Individually programmable drive capability:
    24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - Two slew rates supported (fast and slew-limited).
  - Fast-capture input latch and input Flip-Flop (FF)/latch for reduced input setup time and zero hold time.
  - Fast open-drain drive capability.
  - Capability to register 3-state enable signal.
  - Off-chip clock drive capability.
  - Two-input function generator in output path.
- New programmable high-speed I/O:
  - Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I and II), HSTL (Class I, III, IV), ZBT, and DDR.
  - Double-ended: LVDS, bused-LVDS, and LVPECL. Programmable (on/off), internal parallel termination (100 Ω) is also supported for these I/Os.
- New capability to (de)multiplex I/O signals:
  - New DDR on both input and output.
  - New 2x and 4x downlink and uplink capability per I/O.
- Enhanced twin-block Programmable Function Unit (PFU):
  - Eight 16-bit Look-Up Tables (LUTs) per PFU.
  - Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - 32 x 4 RAM per PFU, configurable as single-port or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the Supplemental Logic and Interconnect Cell (SLIC) decoders as bank drivers.
  - Soft-Wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing which reduces routing congestion and improves speed.
  - Flexible fast access to PFU inputs from routing.
  - Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.

The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. This means that the receive clocks are asynchronous between channels. The retimed data are deserialized and presented as an 8-bit parallel data on the output port. Two-phase receive byte clocks are available synchronous with the parallel words.

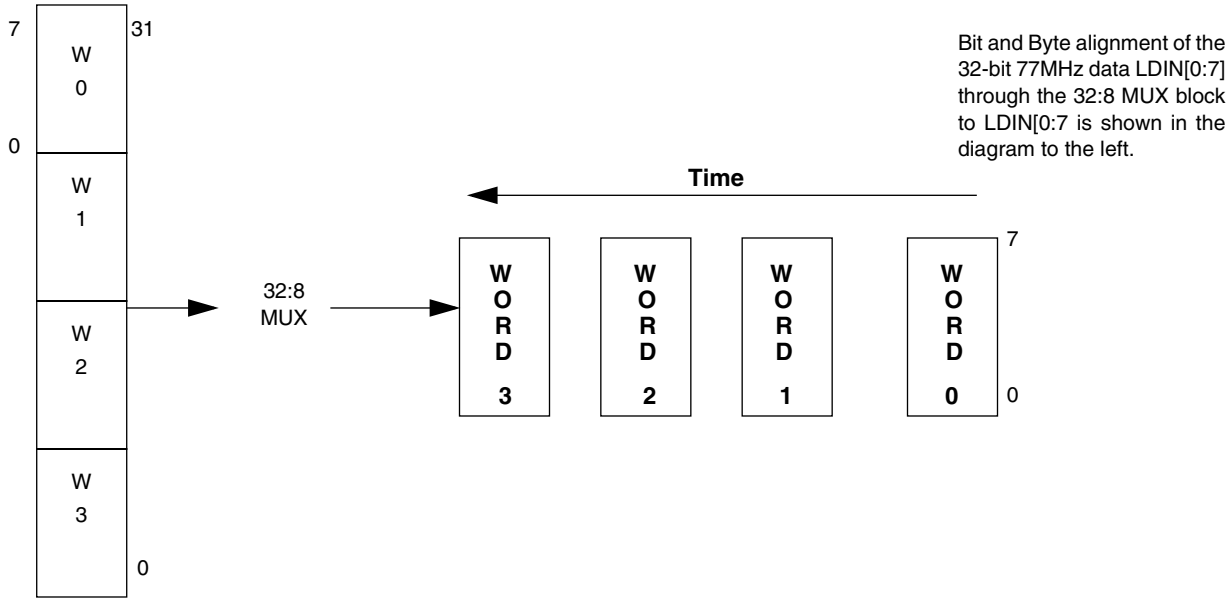
A fractional band-gap voltage generator is included on the design. An external resistor (3.32 kΩ ± 1%), connected between the pins REXT and VSSREXT generates the bias currents within the chip. This resistor should be able to handle at least 300 µA.

32:8 MUX

The MUX block is responsible for converting 32 bits of data at 77.76 MHz to 8 bits of data at 311.04 MHz. It will contain a small elastic store for clock domain transfer between the write clock from the FPGA to the divide-by-4 clock from the SERDES output clock (XCK311). It is recommended to use the clocking scheme shown later in Figure 27, Figure 28 and Figure 29 to guarantee that this elastic store will not be overrun. The 32:8 MUX is also responsible for producing the divide-by-4 clock from the SERDES output clock (XCK311) which is 311.04 MHz at a line rate of 2.488 Gbps.

In the MUX block 32-bit data synchronous to the 77.76 MHz is multiplexed to LDOUTx[7:0] synchronous to the 311.04 MHz SERDES output clock. Parallel 32-bit data can be received directly from the FPGA logic (SERDES only mode) or from the payload sub-block. Bit and byte alignment for the MUX block is shown in Figure 7.

Figure 7. Bit and Byte Alignment for MUX Block



The serialized data are available at the differential CML outputs to drive either an optical transmitter, coaxial media, or circuit board/backplane. The transmitter's CML output buffer is terminated on-chip by 86Ω to optimize the data eye as well as to reduce the number of discrete components required. The differential output swing reaches a maximum of 1.2 VPP in the normal amplitude mode. A half amplitude mode can be selected via configuration register bit HAMP_xx. Half amplitude mode can be used to reduce power dissipation when the transmission medium has minimal attenuation or for testing of the integrity (loss) of the physical medium.

A programmable preemphasis circuit is provided to boost the high frequencies in the transmit data signal to maximize the data eye opening at the far-end receiver. Preemphasis is particularly useful when the data are transmitted over backplanes or low-quality coax cables which have a frequency-dependent amplitude loss. For example, for FR4 material at 2.5 GHz, the attenuation compared to the 1.0 GHz value is about 3 dB. The attenuation is a result of skin effect loss of the PCB conductor and the dielectric loss of the PCB substrate. This attenuation causes intersymbol interface which results in the closing of the data eye at the receiver.

The receive PLL has two modes of operation as follows: lock to reference and lock to data with retiming. The control bit LCKREFN_xx selects the operating mode. When setup to lock to data and no data or invalid data are present on the HDINP and HDINN pins, the receive VCO will not lock to data and its frequency can drift outside of the nominal ±100 ppm range. Under this condition, the receive PLL will lock to REFCLK for a fixed time interval and then will attempt to lock to receive data. The process of attempting to lock to data, then locking to clock will repeat until valid input data exists. The default mode is lock to reference.

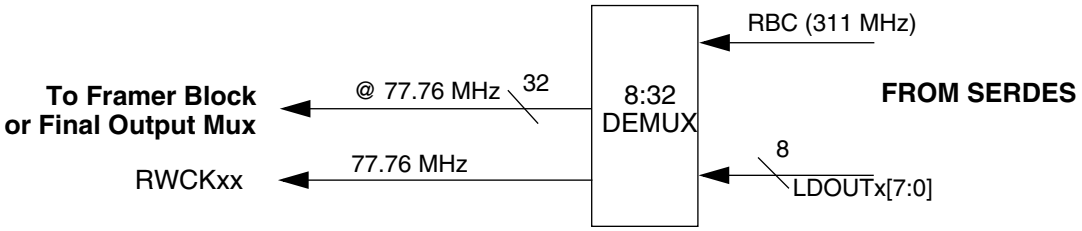
The recovered byte clock (RBC0) is only centered on the data when operating in the lock to data mode. In the lock to reference mode, RBC0 is not centered on the data and may not capture the correct byte value.

The SERDES receives MSB first and LSB last. Hence LDOUTx[7] is the bit that is received first and LDOUTx[0] is the bit that is received last.

8:32 DEMUX

The SERDES provides an eight bit data bus, and a clock, RBC0, which has a rising edge which occurs in the center of the valid data region. The DEMUX block will create one 32-bit data word from the single 8-bit bus. The DEMUX block will also provide a 77.76 MHz clock (divide-by-4 clock of RBC0) called RWCKxx to the rest of the logic blocks such as the framer, descrambler, cell extractor and FIFOs.

Figure 9. 8:32 DEMUX Block



In the DEMUX block, LDOUTx[7:0] is demultiplexed to a 32-bit data bus synchronous to the derived 77.76 MHz clock generated by dividing the 311.04 MHz clock by four. The 77.76 MHz clock is used by the remaining embedded blocks, as well as being fed to the FPGA. Receive data from the DEMUX block is unframed. Parallel data can be sent directly to the FPGA logic (SERDES only mode) or to the framer block for processing. Bit and byte alignment for the DEMUX block is shown in Figure 10.

ation will be based on the system frame pulse (DINxx_FP) received from the FPGA logic, hence it is recommended that, for multi-channel alignment at the receiver, the frame pulses for the channels in an alignment group be synchronized. The data are then scrambled before being sent to the SERDES.

In the receive direction, the two SONET blocks process the receiving channels which can be treated as STS-192 streams or as independent STS-48 streams.The clocks for the received data are recovered from the received serial data streams and a serial to parallel conversion is performed on the data. The frame format of the incoming data are reconstructed (optional). The data then is descrambled using the standard SONET polynomial and a B1 parity error check is performed on the data from the previously transmitted frame.

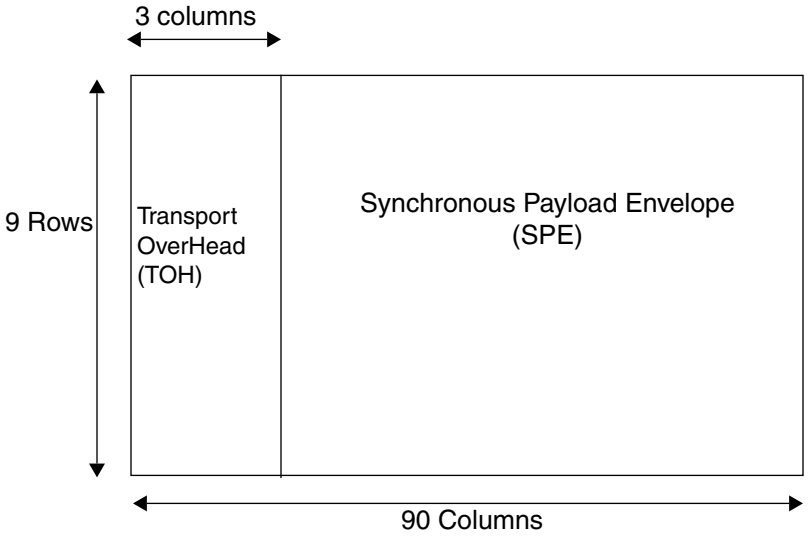
In the SONET mode, the incoming serial data streams can be aligned by groups of two, four or, in the ORSO82G5, eight. When doing multichannel alignment of two or more data streams, the receiver can handle the data streams with frame offsets of up to 18 78MHz clock cycles due to timing skews between cards and along backplane traces or other transmission medium. For multichannel alignment capability to operate properly, it should be noted that while the skew between channels can be very large, they must operate at the exact same frequency (0 ppm frequency deviation), thus requiring that the transmitters sourcing the data being received be driven by the same clock source. It is highly recommended that the frame pulses, DINxx_FP, for all links in an alignment group be synchronized. (See Table 11 and Table 12 for details of the core/FPGA transmit direction signal assignments.)

The received data streams are processed and passed to the FPGA logic as 32-bit words. In SONET mode, DOUTxx[31:0] carries the 32 bit data from the alignment FIFO of the respective channel and an accompanying frame pulse, DOUTxx_FP. Other core/FPGA carries miscellaneous information such as OOF, BIPERR, and SPE indicator. (See Table 13 and 14 for details of the core/FPGA receive direction signal assignments.)

Basic SONET Frame Format

An STS-N frame can be broadly divided into the Transport OverHead (TOH) and the Synchronous Payload Envelope (SPE) areas. The TOH comprises of bytes that are used for framing, error detection and various other functions. The start of the SPE can begin at any point in a SONET frame. The start of the SPE is determined using the pointer bytes located in the TOH. The basic STS-1 frame is shown in Figure 12. Higher rate STS_N signals are created by byte interleaving N STS-1 signals. Some TOH bytes have slightly different functions in STS-N frames than in the basic STS-1 frame. The ORSO42G5 and ORSO82G5 offer two options for processing the TOH bytes, as discussed in a later section.

Figure 12. STS-1 Frame Format



Supported Data Formats

The ORSO42G5 and ORSO82G5 in the SONET mode support the following formats:

- Single OC-48 on each of the channels at a bit rate of 2.488 Gbps.
- OC-192 received in block OC-48 format on four channels at a combined rate of 9.952 Gbps.

The ORSO42G5 and ORSO82G5 SERDES will operate at the OC-12 rate of 622 MHz. For this rate, REFCLK is set to 77 MHz and the SERDES is used in half rate mode. However the embedded core SONET framing/processing logic is fixed at the OC-48 rate and therefore can not talk directly with standard STS-12 devices. In order to interoperate with standard STS-12 devices, the user must bypass the SONET functionality in the ORSO embedded core (SERDES-only mode) and implement all framing, TOH and scrambling/descrambling functionality in FPGA logic.

Figure 13 reveals the byte-ordering of the individual STS-48 streams. STS-192 is supported but it must be received in the block STS-48 format as shown in Figure 14. Each OC-48 stream is composed of byte-interleaved OC-1 data as described in GR-253 standard. Note that the SPE data is not touched by the core.

Figure 13. Byte Ordering of Input/Output Interface in STS-48 Mode

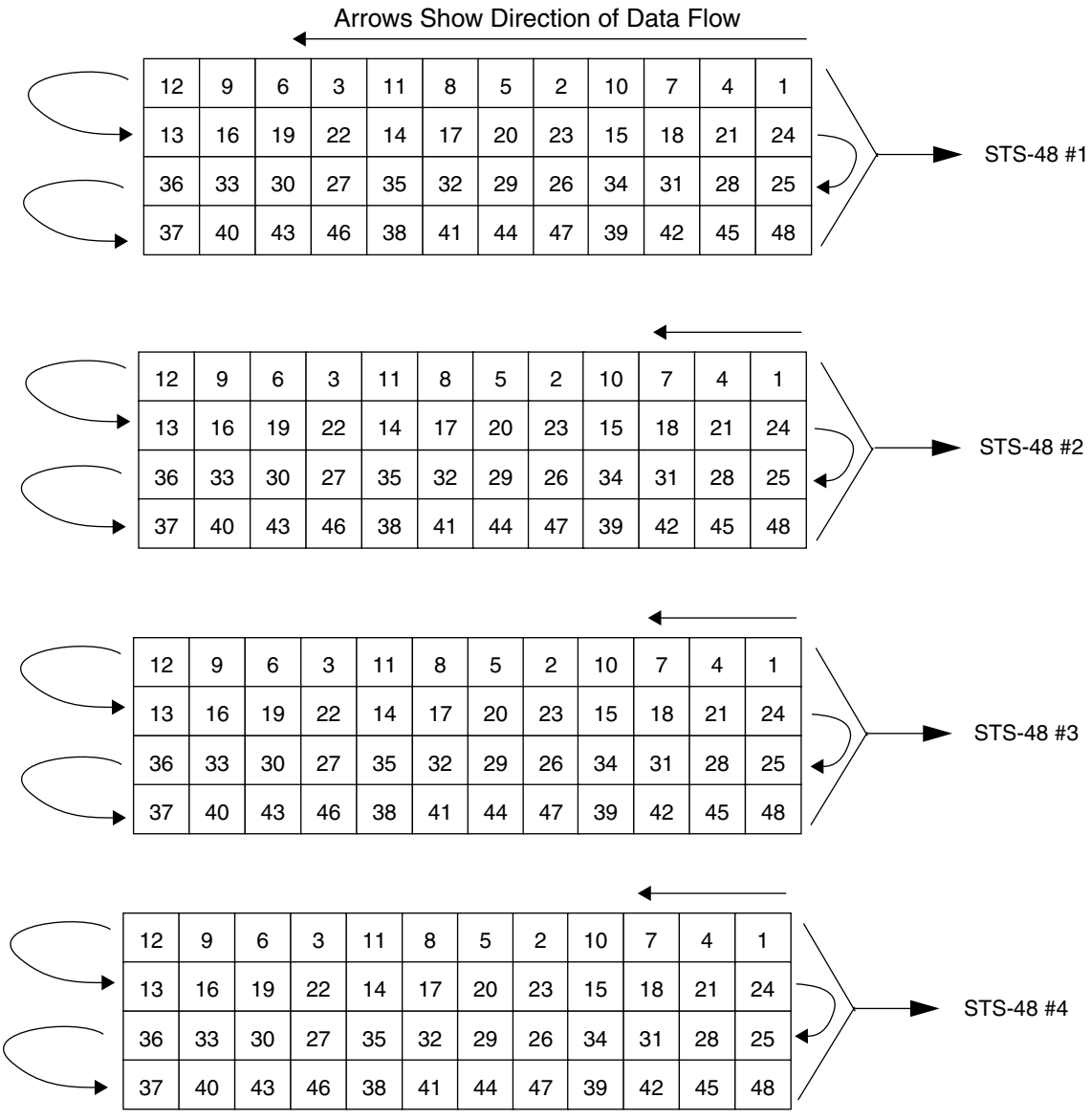


Figure 14. Byte Ordering of Input/Output Interface in STS-192 (Block STS-48) Mode

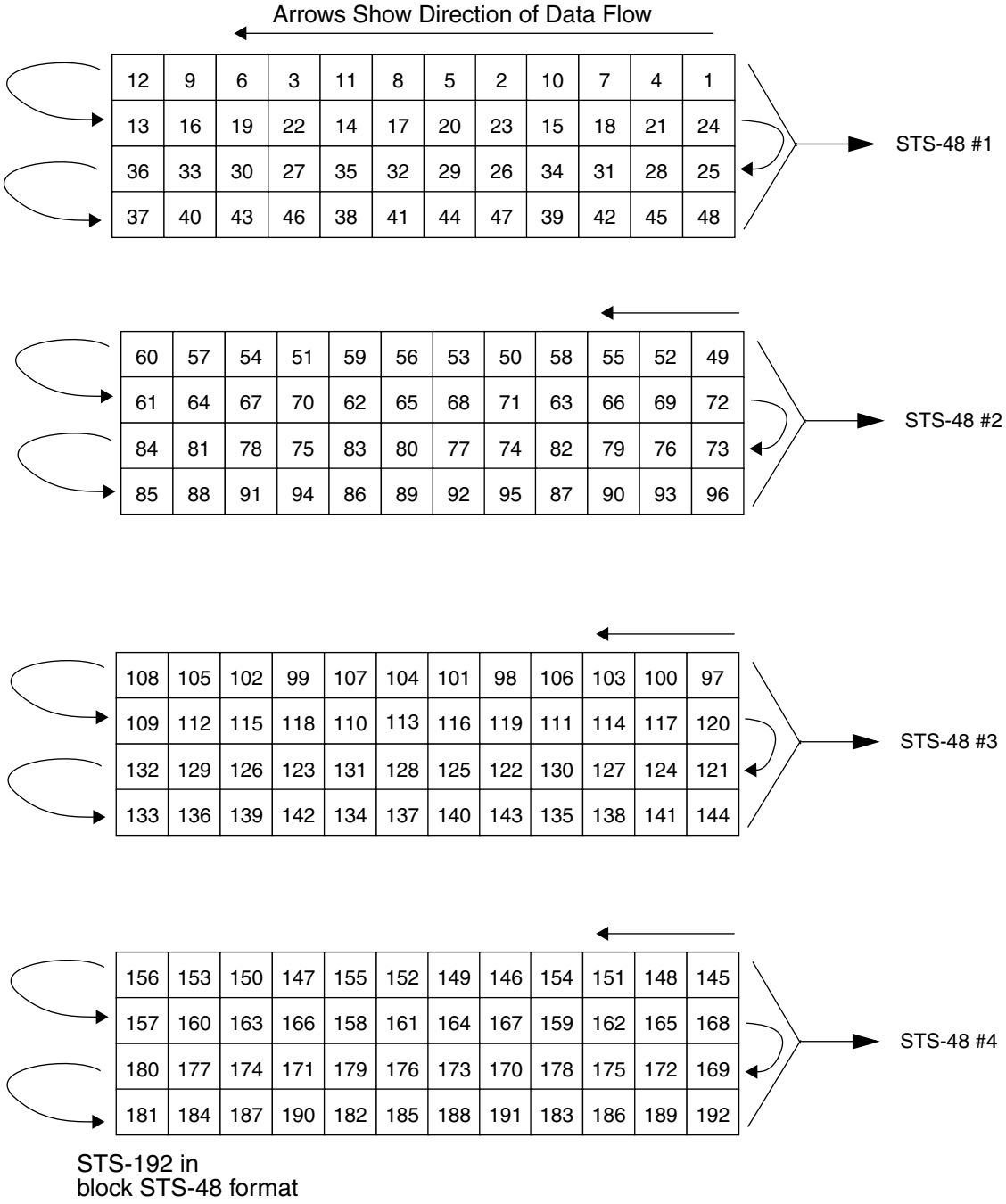
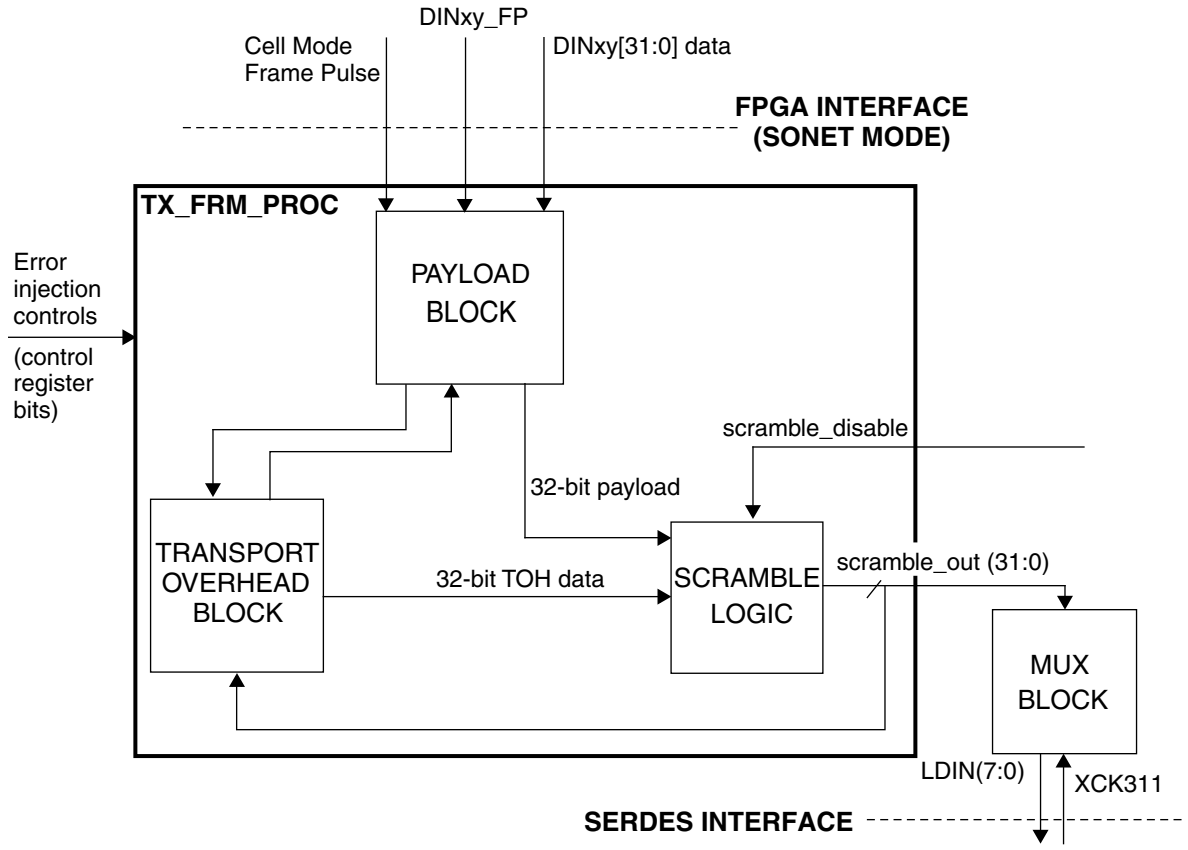


Figure 16. TX Frame Processor (TFP) Block Diagram



Payload Sub-block

The Payload sub block is activated by the cell mode frame pulse (cell mode) or DINxx_FP from FPGA (SONET mode). A pulse on this signal indicates the start of a frame.

In SONET mode, only two types of data bytes are in each frame:

- TOH bytes
- SPE data bytes

There are N x 3 (N = 48) bytes of TOH per row and there are a total of 9 rows in a SONET frame. The rest of the bytes in each row are SPE data bytes in SONET mode.

TOH Sub-block

This block is responsible formatting the 144 (48 x 3) bytes of TOH at the beginning of each row of the transport frame. All TOH bytes may be transmitted transparently from the FPGA logic using the transparent mode. Alternately, some or all TOH bytes may be inserted by the TOH block (AUTO_SOH and AUTO_TOH mode). The TOH data is transferred across the FPGA/core interface as 32-bit words, hence 36 clock cycles (12 x 3) are needed to transfer a TOH row. TOH insertion is controlled by software register bits as shown in the Register Map tables.

Section (B1) BIP-8 Calculator
The section BIP-8 B1 byte in a given STS-N frame contains the scrambled BIP value for all scrambled bytes of the previous frame. Except for the A1,A2 and J0 section overhead bytes, all bytes in a frame are scrambled. The Section (B1) BIP-8 is calculated as the even parity of all bits in the current STS-48 frame. This value is compared to the Section Overhead B1 byte of the next frame. B1 error counters are available that monitors the number of B1 errors on a per-channel basis. A B1 parity error flag is also generated as a software alarm bit.

Descrambler
The data from the framer is descrambled using the SONET/SDH standard generator polynomial $1 + x^6 + x^7$. The descrambling is performed in parallel on each 32-bit word per channel, synchronized to the frame pulse and can be disabled through the software register bit.

RDI (Remote Defect Indicator) Monitor
The line RDI (RDI-L) is monitored through bits 2-0 of the K2 byte. Within the 32-bit descrambled data, a pattern of "110" on bits 26-24 will indicate a RDI-L status. RDI-L must be detected in two consecutive frames before an RDI alarm register bit is set. If fast_frame_mode is enabled, then the RDI alarm register bit will be set if RDI-L is detected in one frame.

Receive FIFO
Clock domain transfers and multi-link de-skew are one of the most critical parts of this device. The main clock domain transfer for the datapath is handled by the receive FIFO. For each link, there are two FIFOs. A 24 x 33 FIFO is used in SONET mode.

The use of the FIFO is controlled by configuration bits.

- Data can be sent from the descrambler directly to the FPGA bypassing the alignment FIFO. Data from each channel will have an associated clock (RWCKxx at 77.76 MHz). Each channel will also provide a FP and SPE indicator along with the data. Descrambling can be inhibited through the DSCR_INH_xx control bit.
- Data can be sent directly from the 8:32 DEMUX block to the FPGA bypassing the alignment FIFO and SONET framer and descrambler. Data from each channel will have an associated clock. No SPE or FP indicator is provided with the data.

Receive FIFO in SONET mode
The receive FIFO used in SONET mode will allow for an inter-link skew of about 300 ns (24 x 32 = 768 bits, 400 ps per bit gives 307 ns). The FIFO is written at 77.76 MHz and read at 77.76 MHz. Once frame synchronization has occurred, the write control logic will cause data to be written to the memory. The write control block is required to insure that the word containing the first A1 byte is written to the same location (address 0) in the FIFO. The synchronization algorithm issues a sync pulse and sync error signals to the read control block based on the alignment option chosen. This sync pulse will coordinate the reading of the FIFOs.

The read control logic synchronizes the reading of the FIFO for the streams that are to be aligned. The block begins reading when the FIFO sync sub block signals that all of the applicable A1s with the appropriate margin have been written to the FIFO. All of the read blocks to be synchronized begin reading at the same time and same location in the memory (address 0). The block also takes the difference between the write and read address to indicate the relative skews between the links. If this difference exceeds a certain limit (programmable), then an alarm (alignment overflow) is provided to the register interface.

Multi-channel Alignment in SONET Mode – ORSO42G5
The alignment FIFO allows the transfer of all data to a common clock. The FIFO sync block allows the system to be configured to allow the frame alignment of multiple slightly varying data streams. This optional alignment ensures that matching SERDES streams will arrive at the FPGA end in perfect data sync. It is important to note that for all aligned channels in a group, the SERDES transmitters on the other side of the high-speed link must all be transmitting data at exactly the same frequency (0 ppm difference), i.e., using a common clock source.

The ORSO42G5 has a total of four channels (two per SERDES block). The incoming data of these channels can be synchronized in several ways, or they can be independent of one other. Two channels within a SERDES can be

SPE Generator

The SPE generator in the ORSO42G5 and ORSO82G5 is used to indicate the payload and overhead portions of a SONET frame. It is present in the SONET data path only. The SPE generator generates row, column and STS counters based on the frame pulse received from the (24 x 33) alignment FIFO or from the descrambler if alignment FIFOs are bypassed. It also retimes the 32-bit data in order to align it with the SPE indicator. The SPE generator will also detect negative or positive pointer justification (if justification is enabled) by looking at the ID bits in the H1 and H2 bytes and adjust the SPE indicator for the STS-1 frame being justified as follows:

- During positive pointer justification, the SPE will be low during H3 byte and the SPE byte following it.
- During negative pointer justification, the SPE will be high during H3 byte.
- During no justification, the SPE will be low during H3 byte.

This block only detects the incoming pointer bytes for SPE generation. This capability can be enabled by software control. By default, the SPE generator will ignore any pointer justification. This block has no capability of any pointer processing, pointer checking or pointer mover operation and ignores “new data” indications from the SONET specification.

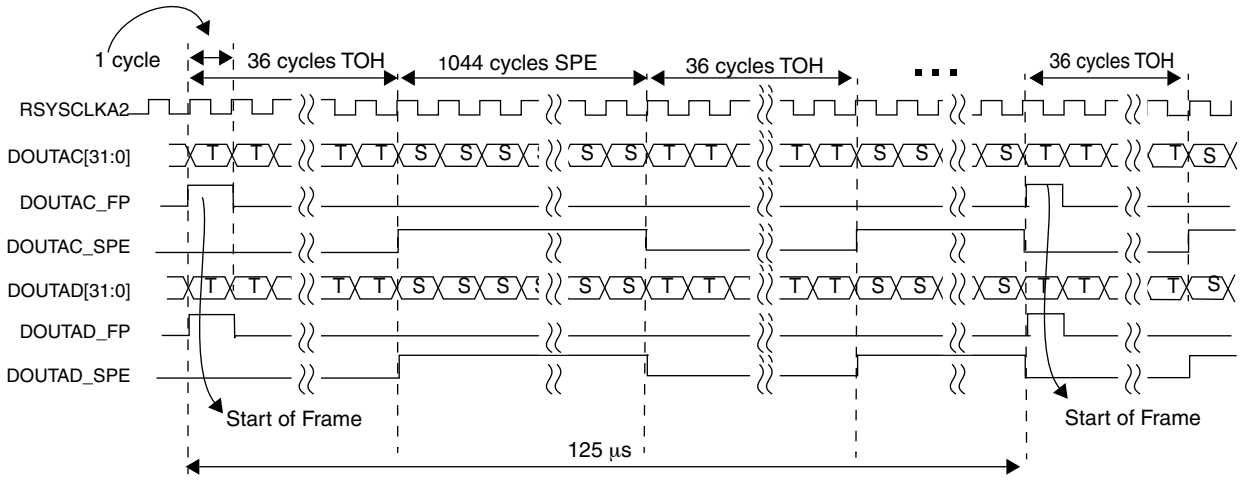
SONET Mode Receive Timing – ORSO42G5

This section contains timing diagrams for major interfaces of this block to the FPGA logic when SONET frames are to be transferred.

- When operating in SONET mode, the entire SONET frame is sent to the FPGA. In multi-channel alignment mode(s), data from all channels within an alignment group are aligned to the A1A2 framing bytes.
- Each SONET frame is 125μs. The frame starts with 36 clock cycles (77.76 MHz) of TOH followed by 1044 clock cycles of SPE, followed by 36 clock cycles of TOH, 1044 cycles of SPE.
- The DOUTxx_SPE signal indicates TOH or SPE in the data (low for TOH, high for SPE)
- Twin pairs are AC, AD (group A2) and BC, BD (group B2)

Figure 32 shows the SONET twin alignment mode timing for the ORSO42G5. The frame pulse and SPE indicators are show for each of the two channels (AC, AD) in twin alignment.

Figure 30. Receive Clocking Diagram for SONET Mode Twin Alignment in Block A – ORSO42G5



Clocks
RSYSCLKA2 is the read clock used for group A2
RSYSBLKB2 is the read clock used for group B2

Data
T Represents TOH
S Represents SPE
DOUTxx-SPE is high for SPE, low for TOH

Table 14. RX Core/FPGA Interface Signals – ORSO82G5 (Continued)

37	—	CELL_BEGIN_OK_B1	—
36	DOUTBB_FP	—	
35	DOUTBB_OOF		
34	DOUTBB_SPE	—	
33	—		
32	DOUTBB_B1_ERR		
[31:20]	DOUTBB[31:20]	—	
[19:0]	DOUTBB[19:0]	IPC2_B1[19:0]	IPC8[59:40]
RXDBC[39:0]	SONET Mode	IPC2 B2 Mode	IPC8 Mode
39	SYNC2_B2_OOS	—	
38	—	IPC2_B2_CELLDROP	—
37	—	IPC2_B2_CELLSTART	—
36	DOUTBC_FP	—	
35	DOUTBC_OOF		
34	DOUTBC_SPE	—	
33	—	IPC2_B2_CELL_BIP_ERR	—
32	DOUTBC_B1_ERR		
[31:20]	DOUTBC[31:20]	—	
[19:0]	DOUTBC[19:0]	IPC2_B2[39:20]	IPC8[39:20]
RXDBD[39:0]	SONET Mode	IPC2 B2 Mode	IPC8 Mode
39	—		
38	SYNC4_B_OOS	—	
37	—	CELL_BEGIN_OK_B2	—
36	DOUTBD_FP	—	
35	DOUTBD_OOF		
34	DOUTBD_SPE	—	
33	—		
32	DOUTBD_B1_ERR		
[31:20]	DOUTBD[31:20]	—	
[19:0]	DOUTBD[19:0]	IPC2_B2[19:0]	IPC8[19:0]

- Toggle SOFT_RESET once all clocks have stabilized
  - 30A06 01
  - 30A06 00

3. SONET Alignment FIFO Resynchronization – ORSO42G5

If during operation a link goes OOF the alignment group will continue to run without the errored channel. To realign this link with the rest of group once the OOF condition is cleared the group may need to be resynchronized. This operation (for 4 channel alignment in block A) is shown below.

- Toggle the FMPU_RESYNC2_A2 register bit to reset the alignment FIFO group.
  - 30A04 04
  - 30A04 00

This sequence will stop traffic temporarily on all links in the alignment grouping.

4. Two-Link Cell Mode Initialization – ORSO42G5

This sample initialization uses 2-link cell mode on all links (A1, A2, B1, and B2). Auto_Bundle and Auto_Remove are both used for these links. The GSWRST_[A:B] Rejoin method is used.

- Set SERDES PLL to Lock to Data signal and Auto_TOH mode (per channel, all channels)
  - 30824 and 30834 82
- Enable Auto_Remove and Rejoin
  - 30A03 1B
- Set 2-link cell mode for groups A2 and B2
  - 30A05 0A
- Toggle SOFT_RESET
  - 30A06 01
  - 30A06 00
- Set the TX_CFG_DONE bit to indicate the transmitter is completely configured
  - 30A07 01
- Toggle GSWRST_[A:B] to clear the RX FIFOs
  - 30005 20
  - 30105 20
  - 30005 00
  - 30105 00
- Turn Off Rejoin (clear the Rejoin register bits) and enable Auto_Bundle
  - 30A03 49

Sample Initialization Sequences – ORSO82G5

The following paragraphs show sample control register write sequences for initialization and resynchronization for the major modes of the device. Hexadecimal values will be shown for the data to be written into the control registers. For these values bit 0 will be the MSb while bit 7 is the LSb. For the per-channel control registers, only the first register address is shown. The other per-channel control registers must also be initialized for the desired mode.

1. SERDES-Only Mode Initialization – ORSO82G5

- Set SERDES Only mode (per channel, channel AA selected for sample initialization)
  - 30803 40
- Set SERDES PLL to Lock to Data signal (per channel, channel AA selected for sample initialization)
  - 30804 80

Figure 48. Block Diagram, Embedded Core Memory Slice

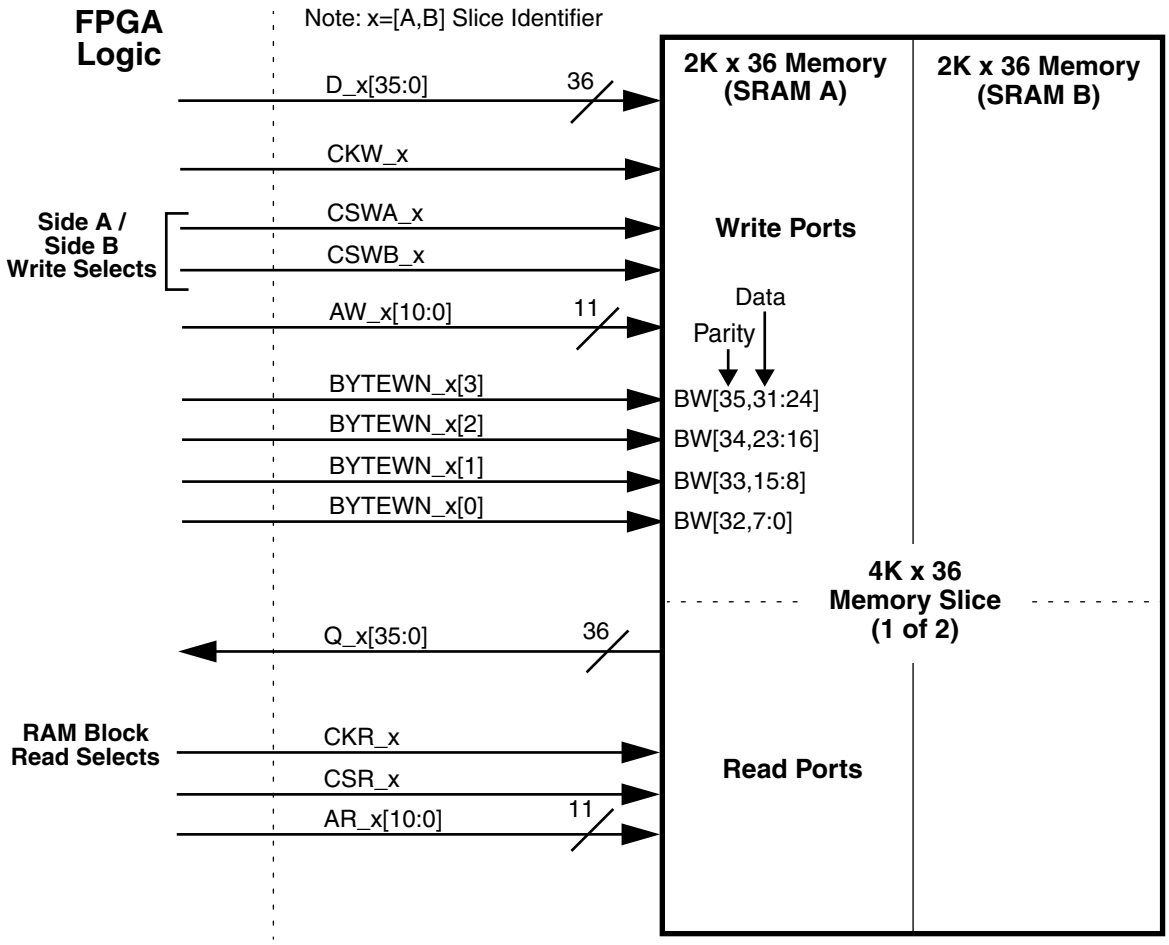


Figure 49. Minimum Timing Specs for Memory Blocks-Write Cycle (-1 Speed Grade)

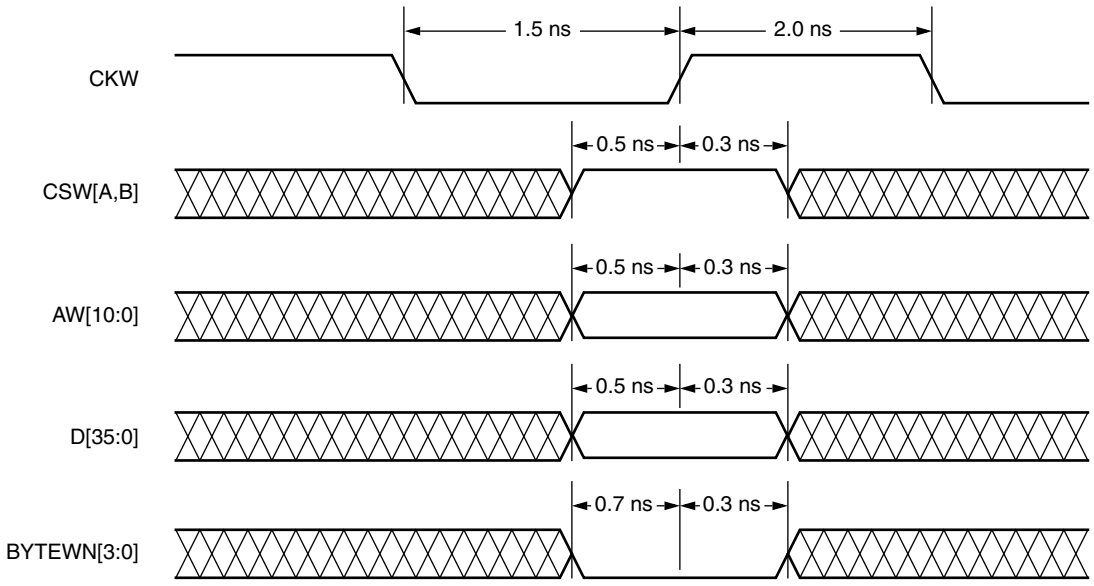


Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A0D	[0]	RSVD	00	Reserved	—
	[1]	SYNC4_B_OVFL		SYNC8_OOS = 1 indicates that the alignment FIFO(s) in the links in block B are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[2]	SYNC2_B2_OVFL		SYNC2_B2_OVFL = 1 indicates that the alignment FIFO(s) in the links BC and BD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[3]	SYNC2_B1_OVFL		SYNC2_B1_OVFL = 1 indicates that the alignment FIFO(s) in the links BA and BB are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[4]	SYNC4_A_OVFL		SYNC4_A_OVFL = 1 indicates that the alignment FIFO(s) in the links in block A are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[5]	SYNC2_A2_OVFL		SYNC2_A2_OVFL = 1 indicates that the alignment FIFO(s) in the links AC and AD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[6]	SYNC2_A1_OVFL		SYNC2_A1_OVFL = 1 indicates that the alignment FIFO(s) in the links AA and AB are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[7]	SYNC8_OVFL		SYNC8_OVFL = 1 Indicates that the alignment FIFO(s) in eight-links are near overflow (At the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
30A0E	[0:2]	RSVD	00	Reserved	—
	[3]	BDL_ALIGN_ERR_B2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs BC and BD	Cell
	[4]	BDL_ALIGN_ERR_B1		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs BA and BB	Cell
	[5]	BDL_ALIGN_ERR_A2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs AC and AD	Cell
	[6]	BDL_ALIGN_ERR_A1		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs AA and AB	Cell
	[7]	BDL_ALIGN_ERR_ALL8		BDL_ALIGN_ERR_ALL8 = 1 -indicates that an alignment error has occurred in cell group of all eight-links	Cell

- Example connections are shown in Figure 52. The naming convention for the power supply sources shown in the figure are as follows:
  - Supply_1.5V Tx-Rx digital, auxiliary power pins
  - Supply_VDD_ANA Analog power pins
  - Supply VDDIB Input Rx buffer power pins
  - Supply_VDDOB Output Tx buffer power pins

Figure 52. Power Supply Filtering

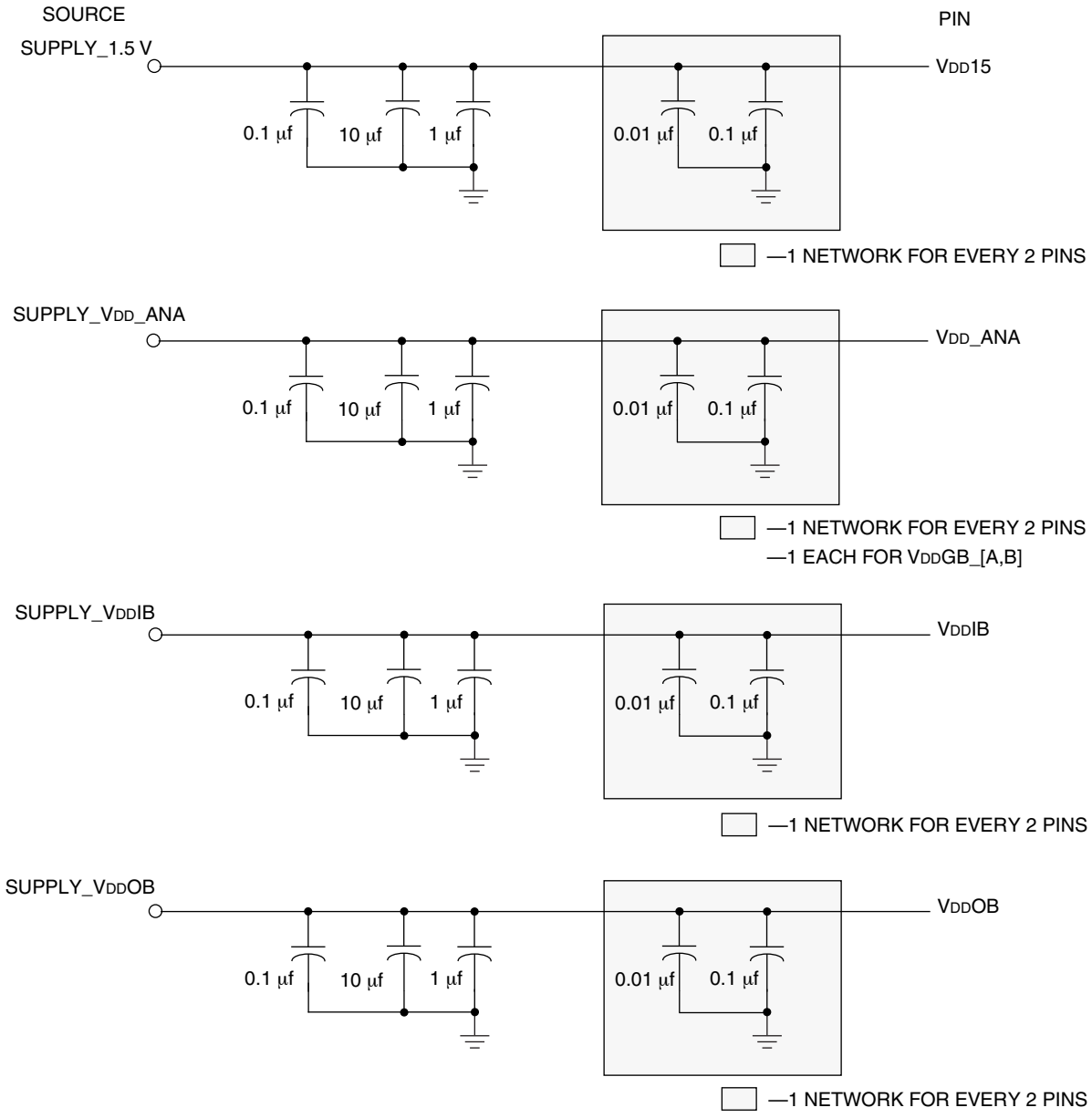


Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AB20	—	—	Vss	Vss	—	—
C3	—	—	VDD33	VDD33	—	—
E4	—	—	O	PRD_DATA	RD_DATA/TDO	—
F5	—	—	I	PRESET_N	RESET_N	—
G5	—	—	I	PRD_CFG_N	RD_CFG_N	—
D3	—	—	I	PPRGRM_N	PRGRM_N	—
A2	0 (TL)	—	VDDIO0	VDDIO0	—	—
F4	0 (TL)	7	IO	PL2D	PLL_CK0C/HPPLL	L21C_A0
G4	0 (TL)	7	IO	PL2C	PLL_CK0T/HPPLL	L21T_A0
B3	0 (TL)	—	VDDIO0	VDDIO0	—	—
C2	0 (TL)	7	IO	PL3D	—	L22C_D0
B1	0 (TL)	7	IO	PL3C	VREF_0_07	L22T_D0
A1	—	—	Vss	VSS	—	—
J5	0 (TL)	7	IO	PL4D	D5	L23C_A0
H5	0 (TL)	7	IO	PL4C	D6	L23T_A0
B7	0 (TL)	—	VDDIO0	VDDIO0	—	—
E3	0 (TL)	8	IO	PL4B	—	L24C_A0
F3	0 (TL)	8	IO	PL4A	VREF_0_08	L24T_A0
C1	0 (TL)	8	IO	PL5D	HDC	L25C_D0
D2	0 (TL)	8	IO	PL5C	LDC_N	L25T_D0
A34	—	—	VSS	VSS	—	—
G3	0 (TL)	8	IO	PL5B	—	L26C_D0
H4	0 (TL)	8	IO	PL5A	—	L26T_D0
E2	0 (TL)	9	IO	PL6D	TESTCFG	L27C_D0
D1	0 (TL)	9	IO	PL6C	D7	L27T_D0
C5	0 (TL)	—	VDDIO0	VDDIO0	—	—
F2	0 (TL)	9	IO	PL7D	VREF_0_09	L28C_D0
E1	0 (TL)	9	IO	PL7C	A17/PPC_A31	L28T_D0
AA13	—	—	VSS	VSS	—	—
J4	0 (TL)	9	IO	PL7B	—	L29C_D0
K5	0 (TL)	9	IO	PL7A	—	L29T_D0
H3	0 (TL)	9	IO	PL8D	CS0_N	L30C_D0
G2	0 (TL)	9	IO	PL8C	CS1	L30T_D0
C9	0 (TL)	—	VDDIO0	VDDIO0	—	—
L5	0 (TL)	9	IO	PL8B	—	L31C_D0
K4	0 (TL)	9	IO	PL8A	—	L31T_D0
H2	0 (TL)	10	IO	PL9D	—	L32C_D0
J3	0 (TL)	10	IO	PL9C	—	L32T_D0
AA14	—	—	VSS	VSS	—	—
M5	0 (TL)	10	IO	PL9B	—	—
F1	0 (TL)	10	IO	PL10D	INIT_N	L33C_A0
G1	0 (TL)	10	IO	PL10C	DOUT	L33T_A0
K3	0 (TL)	10	IO	PL11D	VREF_0_10	L34C_D0
J2	0 (TL)	10	IO	PL11C	A16/PPC_A30	L34T_D0

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
W31	—	—	VSS	VSS	—	—
V30	—	—	VDDOB	VDDOB_BD	—	—
W33	—	—	O	HDOUTN_BD	—	—
H33	—	—	VSS	VSS	—	—
W34	—	—	O	HDOUTP_BD	—	—
V31	—	—	VDDOB	VDDOB_BD	—	—
H34	—	—	VSS	VSS	—	—
J32	—	—	VSS	VSS	—	—
U31	—	—	VDDOB	VDDOB_AD	—	—
T34	—	—	O	HDOUTP_AD	—	—
M32	—	—	VSS	VSS	—	—
T33	—	—	O	HDOUTN_AD	—	—
U30	—	—	VDDOB	VDDOB_AD	—	—
T31	—	—	VSS	VSS	—	—
R34	—	—	I	HDINP_AD	—	—
N32	—	—	VSS	VSS	—	—
R33	—	—	I	HDINN_AD	—	—
T30	—	—	VDDIB	VDDIB_AD	—	—
U32	—	—	VSS	VSS	—	—
R31	—	—	VDDOB	VDDOB_AC	—	—
P34	—	—	O	HDOUTP_AC	—	—
U33	—	—	VSS	VSS	—	—
P33	—	—	O	HDOUTN_AC	—	—
R30	—	—	VDDOB	VDDOB_AC	—	—
P31	—	—	VSS	VSS	—	—
N34	—	—	I	HDINP_AC	—	—
U34	—	—	VSS	VSS	—	—
N33	—	—	I	HDINN_AC	—	—
P30	—	—	VDDIB	VDDIB_AC	—	—
V32	—	—	VSS	VSS	—	—
M34	—	—	O	HDOUTP_AB	—	—
V33	—	—	VSS	VSS	—	—
M33	—	—	O	HDOUTN_AB	—	—
N31	—	—	VDDOB	VDDOB_AB	—	—
M31	—	—	VSS	VSS	—	—
L34	—	—	I	HDINP_AB	—	—
V34	—	—	VSS	VSS	—	—
L33	—	—	I	HDINN_AB	—	—
N30	—	—	VDDIB	VDDIB_AB	—	—
K34	—	—	O	HDOUTP_AA	—	—
K33	—	—	O	HDOUTN_AA	—	—
M30	—	—	VDDOB	VDDOB_AA	—	—
L32	—	—	VDD_ANA	VDD_ANA	—	—
L31	—	—	VSS	VSS	—	—

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: ΘJA, ψJC, and ΘJC. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

ΘJA

This is the thermal resistance from junction to ambient (theta-JA):

$$\Theta_{JA} = \frac{T_J - T_A}{Q} \quad (1)$$

where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, ΘJA is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that ΘJA is expressed in units of °C/W.

ψJC

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance and it is defined by:

$$\psi_{JC} = \frac{T_J - T_C}{Q} \quad (2)$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the ΘJA measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψJC is also expressed in units of °C/W.

ΘJC

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\Theta_{JC} = \frac{T_J - T_C}{Q} \quad (3)$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates ΘJC from ψJC. ΘJC is a true thermal resistance and is expressed in units of °C/W.

ΘJB

This is the thermal resistance from junction to board. It is defined by:

$$\Theta_{JB} = \frac{T_J - T_B}{Q} \quad (4)$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads.

Note that ΘJB is expressed in units of °C/W and that this parameter and the way it is measured are still being discussed by the JEDEC committee.

FPSC Maximum Junction Temperature

Once the power dissipated by the FPSC has been determined, the maximum junction temperature of the FPSC can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Derating calculations for other temperatures than 85 °C and for other voltages can be made within the ispLEVER software environment. Using the maximum ambient temperature, T_{Amax}, and the power dissipated by the device, Q (expressed in °C), the maximum junction temperature is approximated by:

$$T_{Jmax} = T_{Amax} + (Q \cdot \Theta_{JB}) \quad (5)$$

Package Thermal Characteristics

The thermal characteristics of the 484-ball PBGAM (fpBGA with heat spreader) used for the ORT42G5, 680-ball PBGAM (fpBGA with heat spreader) and 680-ball fpBGA used for the ORT82G5 are available in the Thermal Management section of the Lattice web site at www.latticesemi.com.

Heat Sink Vendors for BGA Packages

The estimated worst-case power requirements for the ORSO42G5 and ORSO82G5 are in the 3 W to 5 W range. Consequently, for most applications an external heat sink will be required. Table 53 lists, in alphabetical order, heat sink vendors who advertise heat sinks aimed at the BGA market.

Table 53. Heat Sink Vendors

Vendor	Location	Phone
Aavid Thermal Technology	Laconia, NH	(603) 527-2152
Chip Coolers	Warwick, RI	(800) 227-0254
IERC	Burbank, CA	(818) 842-7277
R-Theta	Buffalo, NY	(800) 388-5428
Sanyo Denki	Torrance, CA	(310) 783-5400
Thermalloy	Dallas, TX	(214) 243-4321
Wakefield Engineering	Wakefield, MA	(617) 246-0874

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 54 lists eight parasitics associated with the ORCA packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 54 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.