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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

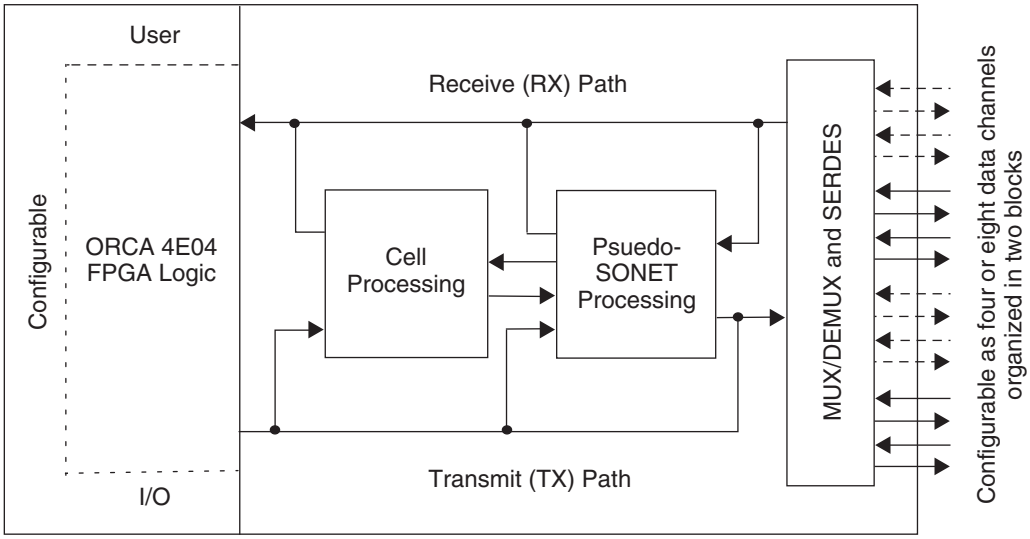
Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso82g5-1fn680i

Table of Contents

- Support for OC-48 and OC-192 (in block OC-48) formats.
- SONET framing, scrambling and SONET Mode channel alignment.
- Performance monitoring functions such as Bit Interleaved Parity (BIP-8) generation and checking and Out-Of-Frame (OOF) and Remote Defect Indication (RDI-L) detection.
- Cell Mode cell creation and extraction, idle cell insertion/deletion, destriping and striping functions.
- Additionally, there are two independent memory blocks in the core. Each embedded RAM block has a capacity of 4K words by 36 bits.

The ORSO42G5 and ORSO82G5 embedded cores contain, respectively, four-channel and eight-channel clock and data recovery macrocells and logical blocks performing functions such as SONET framing, scrambling/descrambling and cell processing. The channels each operate from 0.6 to 2.7 Gbps with per channel CDR functionality. The CDR interface enables high-speed asynchronous serial data transfer between system devices. Devices can be on the same PC-board, on separate boards connected across a backplane, or connected by cables. Figure 2 shows a top level block diagram of the backplane driver logic in the embedded core (embedded RAM not shown).

Figure 2. Top Level Block Diagram ORSO42G5 and ORSO82G5 Embedded Cores



ORSO42G5 and ORSO82G5 Main Operating Modes - Overview

The ORSO42G5 and ORSO82G5 support four and eight 0.6 to 2.7 Gbps serial data channels respectively, which can operate independently or can be combined together (aligned) to achieve higher bit rates. The mode of operation of the core is defined by a set of control registers, which can be written through the system bus interface. The status of the core is stored in a set of status registers, which can be read through the system bus interface.

The serial data channels support OC-48 rates on each channel. The standard OC-48 rate, 2.488 Gbits, is used as the nominal data rate for the technical discussions that follow. OC-192 is also supported but is transmitted and received in block OC-48 links. The scrambled data stream conforms to the GR-255 specified polynomial sequence of $1+x^6+x^7$.

There are three main operating modes in the ORSO42G5 and ORSO82G5 as described below:

- SERDES only (bypass) mode
- SONET mode
- Cell mode
  - Two-link sub-mode
  - Eight-link sub-mode (ORSO82G5 only)

Table 2. Transmit PLL Clock and Data Rates

Data Rate	Reference Clock	TCK78x	Rate
0.6 Gbps	75.00 MHz	18.75 MHz	Half
1.0 Gbps	125.00 MHz	31.25 MHz	Half
1.244 Gbps	155.52 MHz	38.88 MHz	Half
1.35 Gbps	168.75 MHz	42.19 MHz	Half
2.0 Gbps	125.00 MHz	61.50 MHz	Full
2.488 Gbps	155.52 MHz	77.76 MHz	Full
2.7 Gbps	168.75 MHz	84.38 MHz	Full

Notes:
1. The selection of full-rate or half-rate for a given reference clock speed is set by the TXHR bit in the transmit control register and can be set per channel. (For cell mode all channels of a group must have the same TXHR selection.)

The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. This means that the receive clocks are asynchronous between channels. The retimed data are deserialized and presented as a 8-bit parallel data on the output port. RWCKx receive byte clocks are divide-by-4 clocks of the RBC (recovered byte clock) clock provided by the SERDES. This is the clock used in the internal receive functions of the embedded core.

The reference clock is also used by the receive PLL for operation when the input data are not toggling appropriately. Table 3 shows the relationship between the data rates, the reference clock, and the RWCKx clocks.

Table 3. Receive PLL Clock and Data Rates

Data Rate	Reference Clock	RWCKx Clocks	Rate
0.6 Gbps	75.00 MHz	18.75 MHz	Half
1.0 Gbps	125.00 MHz	31.25 MHz	Half
1.244 Gbps	155.52 MHz	38.88 MHz	Half
1.35 Gbps	168.75 MHz	42.19 MHz	Half
2.0 Gbps	125.00 MHz	61.50 MHz	Full
2.488 Gbps	155.52 MHz	77.76 MHz	Full
2.7 Gbps	168.75 MHz	84.38 MHz	Full

Note: The selection of full-rate or half-rate for a given reference clock speed is set by the RXHR bit in the receive control register and can be set per channel. (For cell mode all channels of a group must have the same RXHR selection).

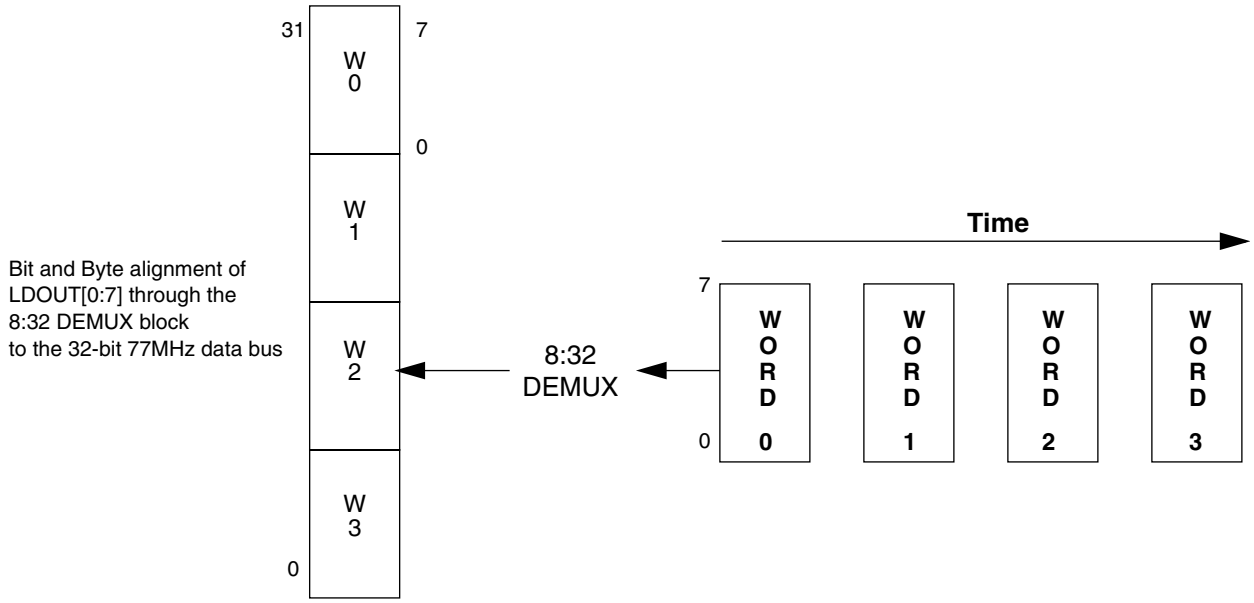
The differential reference clock is distributed to all channels in a SERDES block. Each channel has a differential buffer to isolate the clock from the other channels. The input clock is preferably a differential signal; however, the device can operate with a single-ended input. The input reference clock directly impacts the transmit data eye, so the clock should have low jitter. In particular, jitter components in the DC-5 MHz range should be minimized.

Detailed Description - SERDES Only Mode

The SERDES only (or bypass) mode is the simplest of the three operating modes for the ORSO42G5 and ORSO82G5. In this mode, all of the SONET and cell logic block functions are bypassed and data are transferred directly between the MUX and DEMUX blocks to and from the FPGA interface. This mode is utilized when the user wants to perform all data processing and uses only the SERDES portion of the Embedded Core. For example, this mode could be utilized to replace an existing design using stand-alone SERDES and FPGAs.

The basic data paths in the transmit and receive directions are shown in Figure 5. In general, the descriptions in this section are written to describe the SERDES only mode, although the “SERDES blocks” are also used in SONET and cell mode operation. At the backplane interface, data are transmitted and received serially over pairs

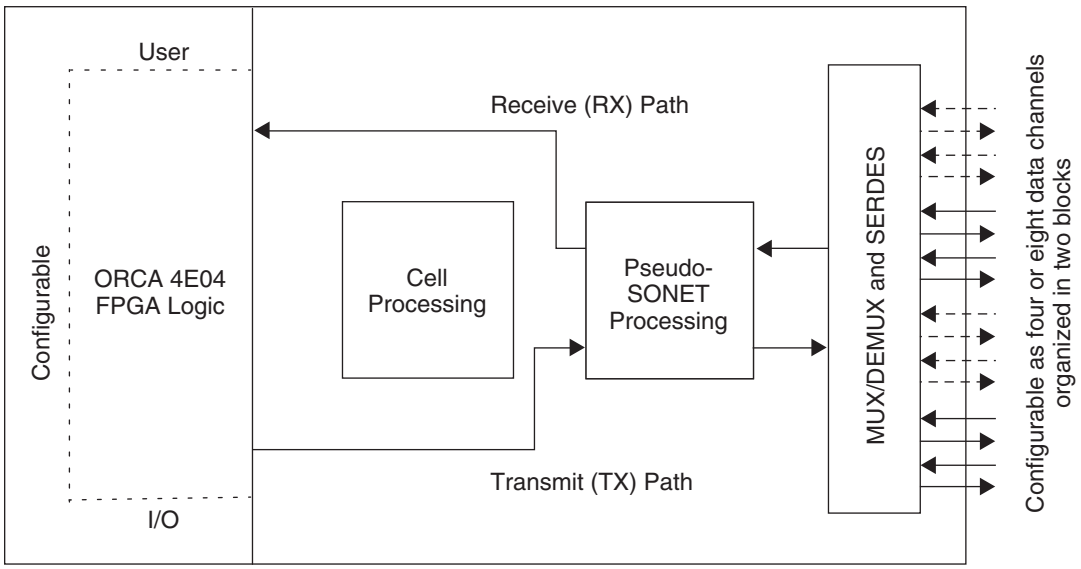
Figure 10. Bit and Byte Alignment for DEMUX Block



SONET Mode Operation – Detailed Description

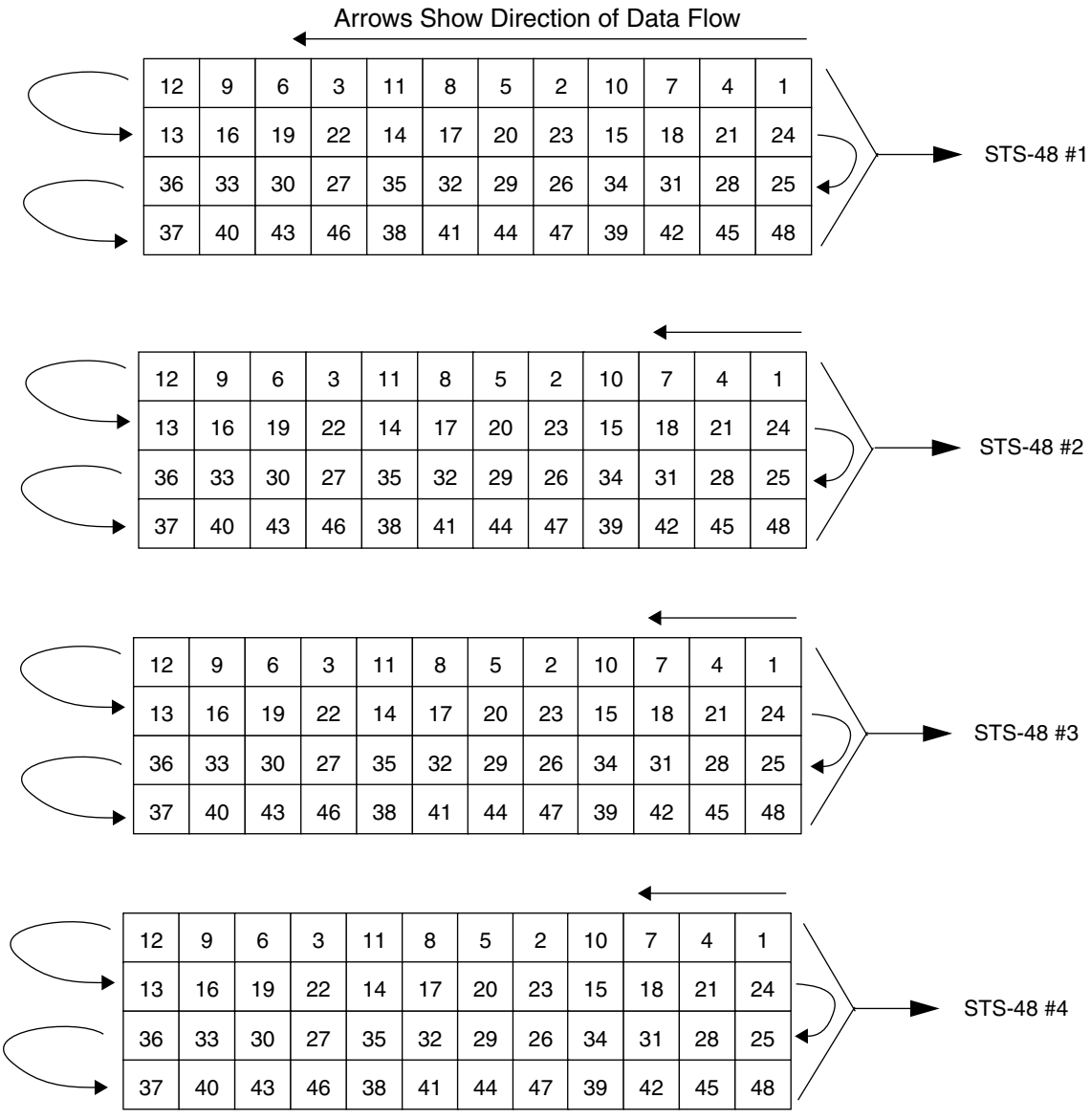
The following sections describe the data processing performed in the SONET logic blocks. The basic data flows in the SONET Mode are shown in Figure 11. At a top level, the descriptions are separated into processing in the transmit path (FPGA to serial link) and processing in the receive path (serial link to FPGA). In general, the descriptions in the next sections are written to describe SONET mode operation, although some of the "SONET logic blocks" are also used in cell mode operation. The various processing options are selected by setting bits in control registers and status information is written to status registers. Both types of registers can be written and/or read from the System Bus. Memory maps and descriptions for the registers are given in Table 21 through Table 36.

Figure 11. Basic Data Flows - SONET Mode



In the SONET mode, the transmit block receives 32-bit wide data from the FPGA (DINxx) on each of its channels along with a frame pulse (DINxx_FP) per channel and a transmit clock (TSYCLKxx). Typically this will represent a STS-48 stream on each link. The data are first passed through a TOH block which will generate all the timing pulses that are required to isolate individual overhead bytes (e.g., A1, A2, B1, D1-D3, etc.). The timing pulse gener-

Figure 13. Byte Ordering of Input/Output Interface in STS-48 Mode

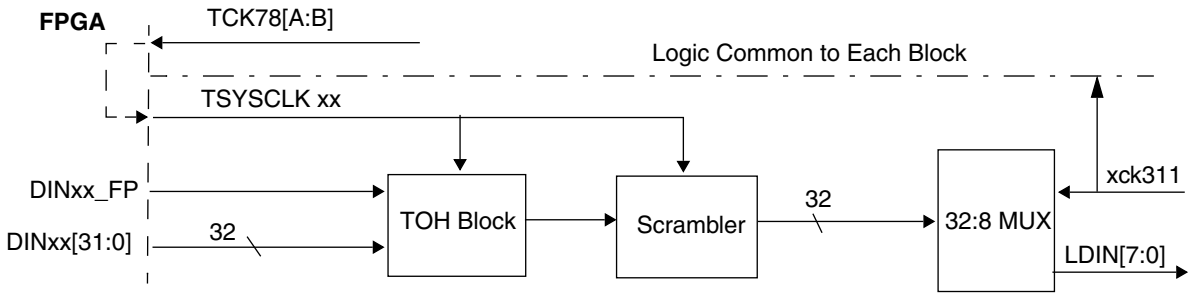


tee that this elastic store will not be overrun. The 32:8 MUX is also responsible for producing the divide-by-4 clock from the SERDES output clock (XCK311) which is 311.04 MHz at a line rate of 2.488 Gbps.

SONET Mode Transmit Timing

Figure 17 shows the transmit clocks and a recommended clocking scheme. As shown, TCK78[A,B] can be used to the source TSYSCLKxx signals. It is a requirement that TSYSCLKxx be frequency locked to the corresponding TCK78[A,B] clock signal derived from REFCLK_[A:B].

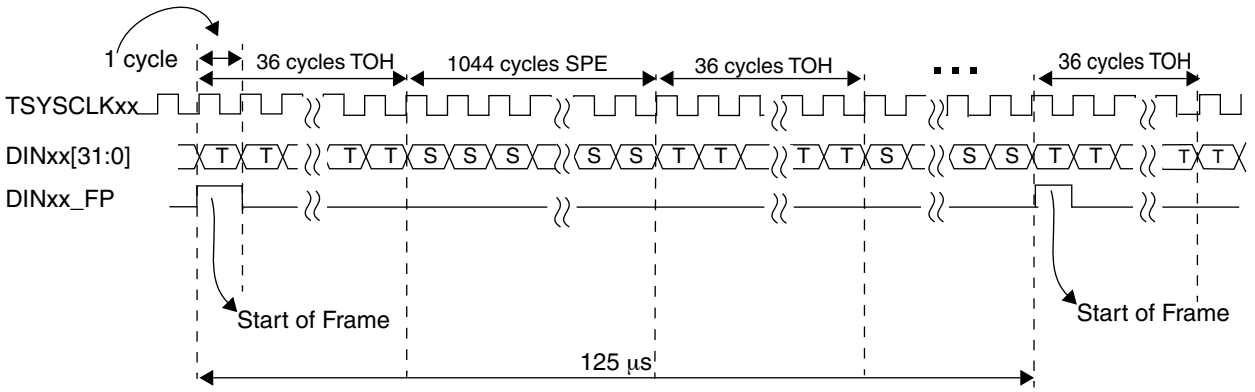
Figure 17. Transmit Clocking Diagram in SONET Mode



xx represents AC, AD, BC, BD (ORSO42G5) or AA, AB, AC, AD, BA, BB, BC, BD (ORSO82G5)

- When operating in SONET mode, the entire SONET frame is sent by the user. Optionally the TOH bytes can be overwritten by the transmit block (AUTO_SOH or AUTO_TOH) before sending to scrambler and SERDES block.
- Each SONET frame is 125 µs given a 155.52MHz reference clock.
- The frame starts with 36 clock cycles (77.76 MHz) of TOH followed by 1044 clock cycles of SPE, followed by 36 clock cycles of TOH, 1044 cycles of SPE etc. for all nine rows.

Figure 18. Transmit SONET Mode



xx represents AC, AD, BC, BD (ORSO42G5) or AA, AB, AC, AD, BA, BB, BC, BD (ORSO82G5).

SONET Mode Receive Path

The receiver block receives a byte from the SERDES blocks for each of the channels. The byte arrives at the receiver block at 311.04 MHz. This data are not frame-aligned or word aligned. The data are first passed through a divide-by-4 DEMUX which produces a 32-bit word at 77.76 MHz. Data from the DEMUX is then passed through a framer which aligns and frames the data. Data are processed based on cell mode or SONET mode.

In the SONET mode, the descrambled data are sent to an alignment FIFO that performs lane-to-lane deskew and aligns data within an alignment group to the RSYCLK clock domain. Both the write and read clocks to the align-

frame pulse, is less than the minimum threshold set by RX_FIFO_MIN. In the memory map section OOS is referred to as SYNC2_[A2,B2]_OOS, SYNC4_OOS. OVFL is referred to as SYNC2_[A2,B2]_OVFL, SYNC4_OVFL.

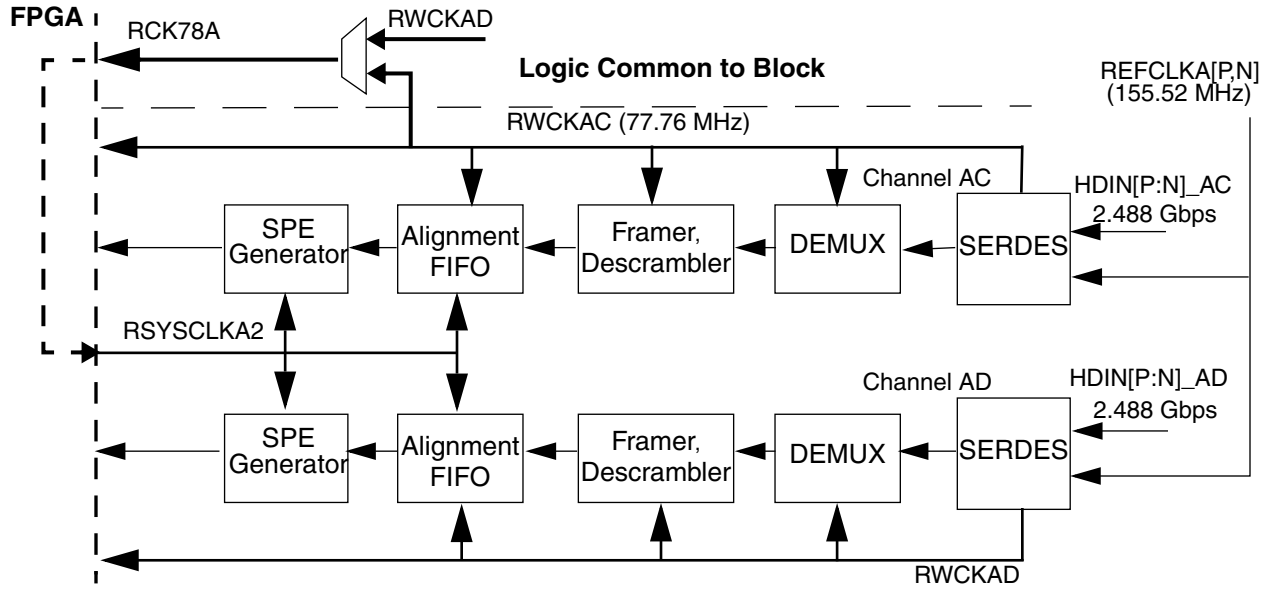
Receive Clocking for Multi-channel Alignment – ORSO42G5

There are a total of seven clocks for the receive path, from FPGA to the core. The two used in SONET mode are RSYSCLKA2 (for block A), and RSYSCLKB2 (for block B). The following diagrams show the recommended clock distribution approaches for SONET mode multi-channel alignment modes. Cell mode alignment is discussed in the section describing the Input Port Controller (IPC).)

SONET Mode Twin Alignment – ORSO42G5

Figure 22 describes the clocking scheme for twin alignment. In twin alignment, the valid channel pairs are AC,AD in block A and BC,BD in block B. The figure provides the clocking scheme for block A as an example. RSYSCLKA2 should be sourced from RCK78A, RWCKAC or RWCKAD. For the ORSO42G5, the use of RCK78A is recommended since it uses primary clock routing resources. This clocking approach provides the required 0 ppm clock frequency matching for each pair and provides flexibility in applications where the two pairs are received from asynchronous sources.

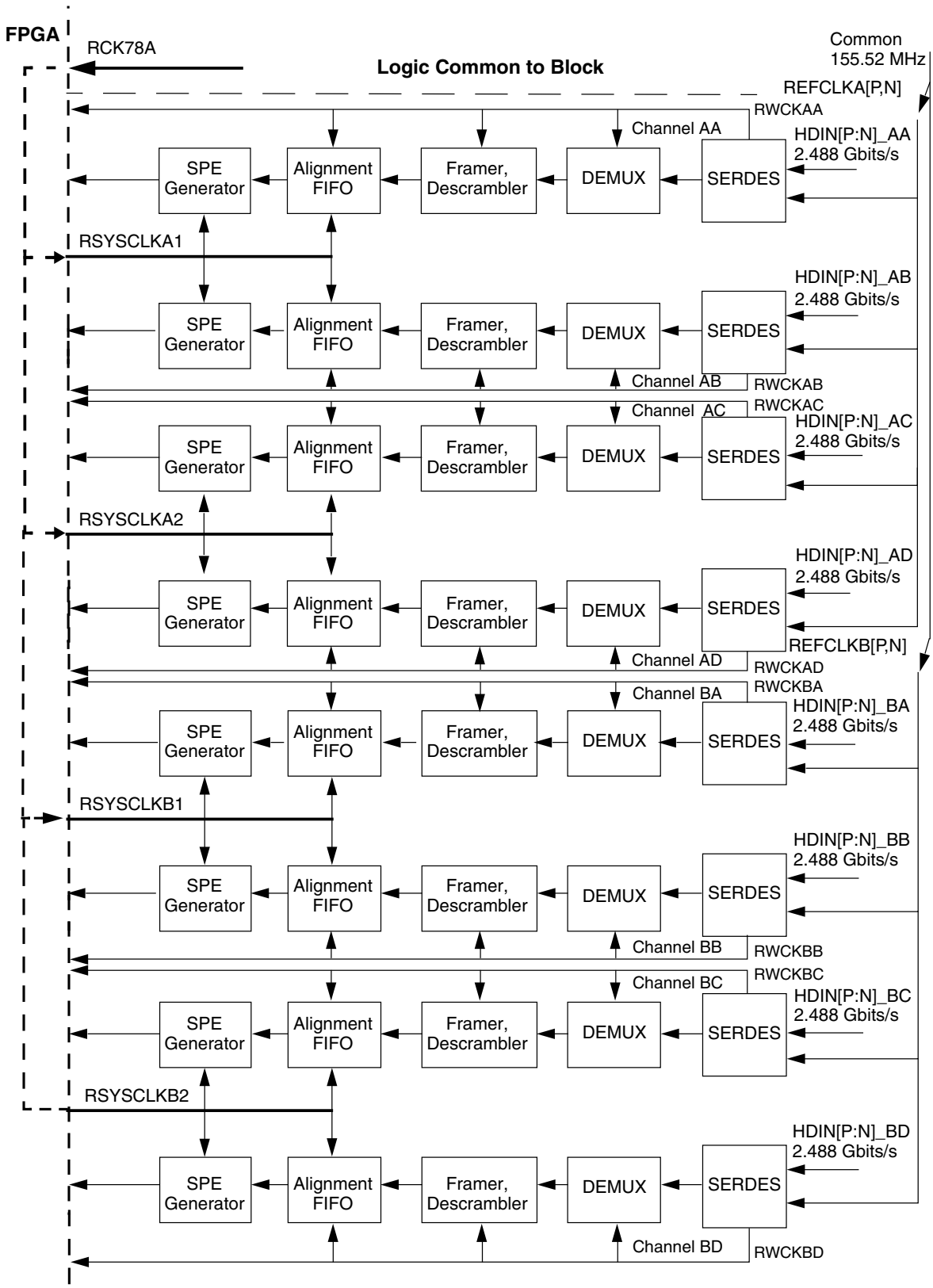
Figure 22. Receive Clocking Diagram for Twin Alignment in Block A – ORSO42G5



SONET Mode Quad Alignment – ORSO42G5

Figure 23 shows the clocking scheme for four-channel alignment. In this application, both clocks RSYSCLKA2 and RSYSCLKB2 should be sourced from a common clock. Either RCK78A or RCK78B can be used as a common clock source. The figure shows RCK78A being used as the clock source.

Figure 29. Receive Clocking Diagram for SONET Mode Eight-Channel Alignment – ORSO82G5



ORSO42G5 Configuration

At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

- Setting bit 1 to one in registers at locations 30002, 30012, 30102 and 30112 powers down the legacy logic. (Note that the reset value for these bits is 0.)
- Setting bit 1 to zero (reset condition) in the register at locations 30802, 30812, 30902 and 30912 removes the legacy logic from any alignment group.

Register settings for SONET multi-channel alignment are shown in Table 7.

Table 7. Multichannel Alignment Modes – ORSO42G5

Register Bits FMPU_SYNMODE_xx[2:3]	Mode
00	No multichannel alignment
01	Twin channel alignment
11	Four channel alignment

Note: xx = [AC,AD,BC,BD]

To align two channels in SERDES A:

- FMPU_SYNMODE_AC = 01 (Register Location 30822)
- FMPU_SYNMODE_AD = 01 (Register Location 30832)

To align two channels in SERDES B:

- FMPU_SYNMODE_BC = 01 (Register Location 30922)
- FMPU_SYNMODE_BD = 01 (Register Location 30932)

To align all four channels:

- FMPU_SYNMODE_AC = 11 (Register Location 30822)
- FMPU_SYNMODE_AD = 11 (Register Location 30832)
- FMPU_SYNMODE_BC = 11 (Register Location 30922)
- FMPU_SYNMODE_BD = 11 (Register Location 30932)

To enable/disable multi-channel alignment of individual channels within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled

where xx = [AC,AD,BC,BD]

To resynchronize a multichannel alignment group set the following bits to one, and then set to zero:

- FMPU_RESYNC4 for four channels, AC, AD, BC and BD. (Register Location 30A04, bit 7)
- FMPU_RESYNCA2 for dual channels, AC and AD. (Register Location 30A04, bit 2)
- FMPU_RESYNCB2 for dual channels, BC and BD. (Register Location 30A04, bit 5)

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bits to one, and then set to zero.

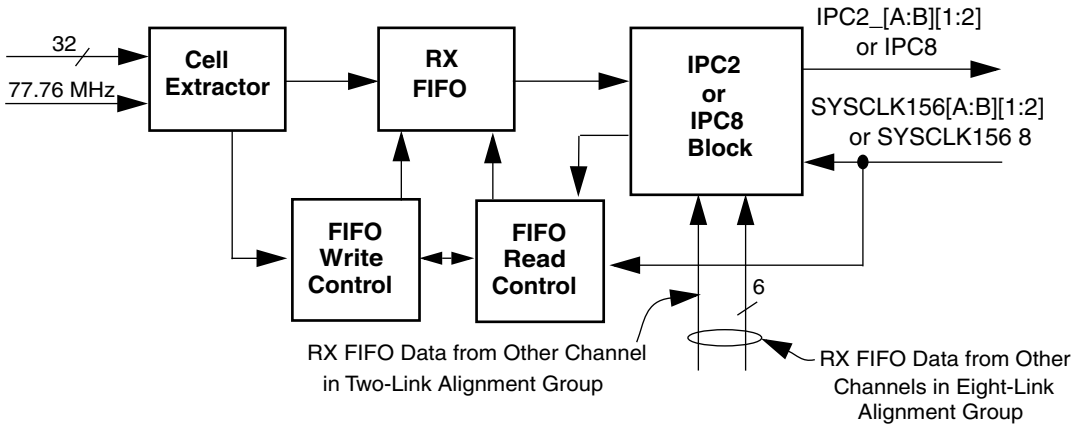
- FMPU_RESYNC1_xx (Register Locations 30824, 20834, 30924 and 30934, bit 7) where xx is one of AC, AD, BC or BD.

Cell Mode Receive Path

The receive logic blocks unique to the cell mode are shown in Figure 43 and are described in the next sections. Prior to reaching this logic the received data has been demultiplexed, frame aligned and descrambled by the SERDES and SONET logic and is formatted on a per channel basis as 32-bit words with an accompanying clock. The clock is a 77.76 MHz clock provided by the DEMUX block performing a divide-by-4 operation on RWCKxx.

The Data Extractor and receive FIFO (RXFIFO) process the data on a per channel basis. The receive FIFO also performs a clock domain transfer to the 156 MHz domain of the Input Port Controller (IPC2/8) blocks. The IPC2/8 blocks perform the two-link or eight-link (ORSO82G5 only) alignment functions. In two-link alignment mode, the received data are passed to the FPGA logic as 40-bit words at the 156 MHz rate. In eight-link alignment mode, the received data are passed to the FPGA logic as a single 160-bit word, again at the 156 MHz rate. Additional mode-dependent status information is also provided across the Core/FPGA interface.

Figure 43. Receive Path Logic Unique to Cell Mode



Cell Extractor

This block is used only in cell mode and does the following:

- Extracts User cells from the SPE
- Performs BIP calculation/checks to verify cell integrity
- Link Header Sequence Interrogation

Processing options include:

- Cell handling for invalid sequence (drop or pass to FPGA)
- S/W configurable ‘link removal’ due to excessive sequence errors

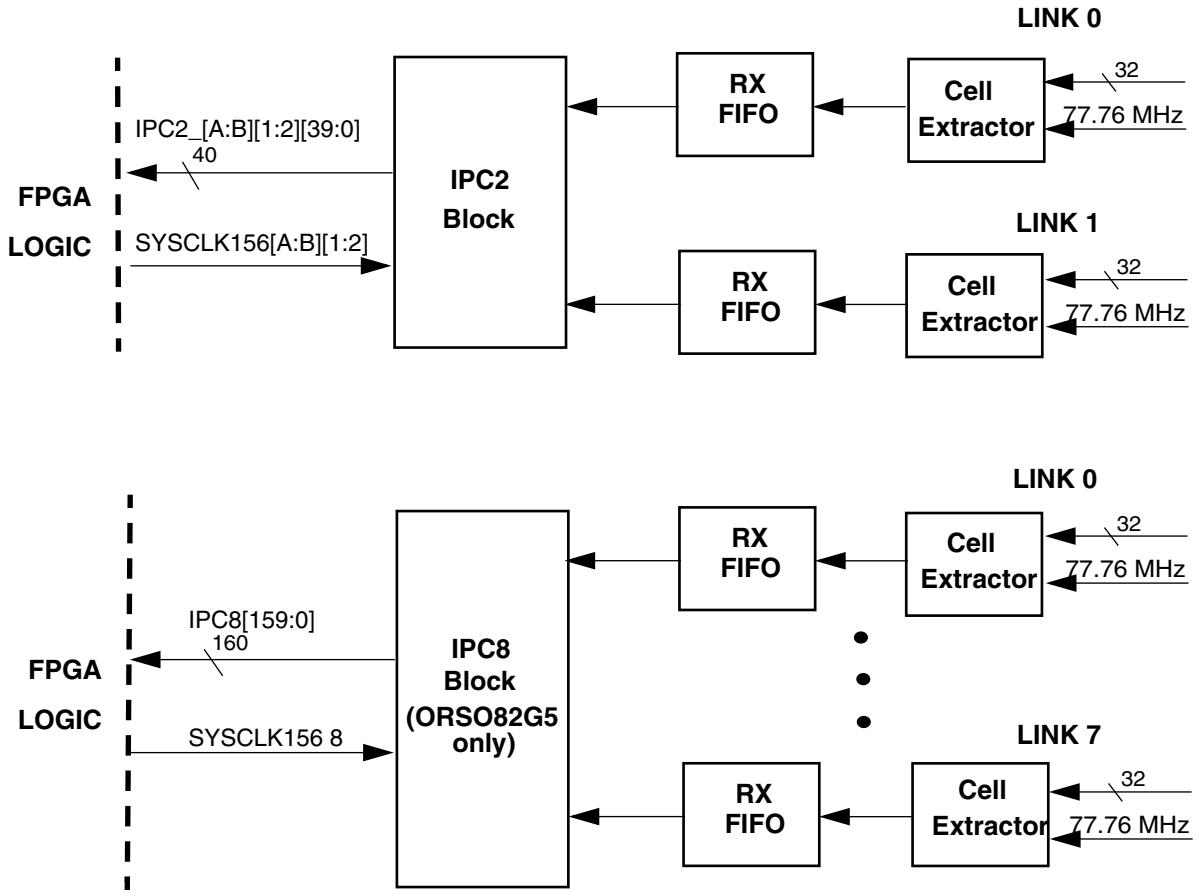
Data from the cell extractor block(s) is sent to the receive FIFO which aligns the data to the system clock domain and provides for deskew between the links.

Cell Extraction and BIP Calculation/Checking

The data from the descrambler are passed into the data extractor which strips the cell data from the payload of a SONET frame. The block extracts the BIP value from the data stream and also perform an internal cell BIP calculation. If the BIP value is not correct, an error flag bit will set in the status registers. The block also determines when the next Link Header is coming in the frame and what the cell sequence number contained within it should be. If the value of the cell sequence counter is not equal to the expected value, an error flag bit will set in the status registers and an error signal will be sent across the core/FPGA interface.

- Insuring group bundles are properly aligned.
- Scheduling reads from the RX FIFOs. Cells are read one at a time from the configured links.
- Parsing the cell data into payload data (along with selected header information). Cells which have errors that make them unusable (such as BIP or sequence number errors) are thrown away. This dropping of errored cells can be disabled through register bits CELL_BIP_INH_xx and CELL_SEQ_INX_xx.

Figure 44. IPC2 and IPC8 Block Diagrams



There are 5 IPC blocks in the embedded core. There is an IPC2 block for every channel pair:

- IPC2_A1 combines links from channels AA,AB (ORSO82G5 only)
- IPC2_A2 combines links from channels AC,AD
- IPC2_B1 combines links from channels BA,BB (ORSO82G5 only)
- IPC2_B2 combines links from channels BC,BD

The IPC8 block combines cells from all eight aligned links and transmits them to the FPGA logic (ORSO82G5 only).

Before an IPC can begin reading data from the Rx FIFOs and assembling cells, it must first align all FIFOs in a port bundle. This is accomplished by handshaking signals between the framer and the IPC. The framer indicates to the IPC that framing has been acquired. The framer does not start filling the FIFOs, however, until the next A1/A2 SONET signal.

- Toggle SOFT_RESET once all clocks have stabilized
  - 30A06 01
  - 30A06 00

3. SONET Alignment FIFO Resynchronization – ORSO42G5

If during operation a link goes OOF the alignment group will continue to run without the errored channel. To realign this link with the rest of group once the OOF condition is cleared the group may need to be resynchronized. This operation (for 4 channel alignment in block A) is shown below.

- Toggle the FMPU_RESYNC2_A2 register bit to reset the alignment FIFO group.
  - 30A04 04
  - 30A04 00

This sequence will stop traffic temporarily on all links in the alignment grouping.

4. Two-Link Cell Mode Initialization – ORSO42G5

This sample initialization uses 2-link cell mode on all links (A1, A2, B1, and B2). Auto_Bundle and Auto_Remove are both used for these links. The GSWRST_[A:B] Rejoin method is used.

- Set SERDES PLL to Lock to Data signal and Auto_TOH mode (per channel, all channels)
  - 30824 and 30834 82
- Enable Auto_Remove and Rejoin
  - 30A03 1B
- Set 2-link cell mode for groups A2 and B2
  - 30A05 0A
- Toggle SOFT_RESET
  - 30A06 01
  - 30A06 00
- Set the TX_CFG_DONE bit to indicate the transmitter is completely configured
  - 30A07 01
- Toggle GSWRST_[A:B] to clear the RX FIFOs
  - 30005 20
  - 30105 20
  - 30005 00
  - 30105 00
- Turn Off Rejoin (clear the Rejoin register bits) and enable Auto_Bundle
  - 30A03 49

Sample Initialization Sequences – ORSO82G5

The following paragraphs show sample control register write sequences for initialization and resynchronization for the major modes of the device. Hexadecimal values will be shown for the data to be written into the control registers. For these values bit 0 will be the MSb while bit 7 is the LSb. For the per-channel control registers, only the first register address is shown. The other per-channel control registers must also be initialized for the desired mode.

1. SERDES-Only Mode Initialization – ORSO82G5

- Set SERDES Only mode (per channel, channel AA selected for sample initialization)
  - 30803 40
- Set SERDES PLL to Lock to Data signal (per channel, channel AA selected for sample initialization)
  - 30804 80

Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30824 - AC 30834 - AD 30924 - BC 30934 - BD	[0]	LCKREFN_xx	00	0 = Lock receiver to reference clock (REFCLK) 1 = Lock receiver to HDINxx data	Both
	[1]	LOOPENB_xx		LOOPENB_xx =1 Enable high-speed internal loopback from TX to RX. Disable the HDOUT buffers.	Both
	[2]	DISABLE_TX_xx		Disable Transmitter, For DISABLE_TX = 1 the TX Link is disabled. The disabled link is ignored by the Output Port Controller (OPC) and internally generated idle cells are transmitted on the link.fIf the link is disabled during the transmission of a cell on the link, the entire cell is transmitted before the link is declared invalid.	Cell
	[3]	DISABLE_RX_xx		Disable Receiver, DISABLE_RX = 1 disables the RX link for cell processing by the Input Port Controller (IPC). The IPC will not read cells from a link if this bit is set for that link	Cell
	[4]	CELL_BIP_INH_xx		Cell BIP (Check) Inhibit, CELL_BIP_INH = 1 prevents cells from being dropped due to a Cell BIP error, in the RX path. If this bit is not set, then cells will be dropped automatically if a cell bip error is detected by the core. The CELLDROP signal across the core-FPGA interface will be active only if this bit is NOT set.	Cell
	[5]	CELL_SEQ_INH_xx		Cell Sequence (Checking) Inhibit, CELL_SEQ_INH = 1 prevents cells in the RX path from being dropped due to a sequence error. If this bit is not set, then cells will be dropped automatically if a sequence error is detected internally. The CELLDROP signal across the core-FPGA interface will be active only if this bit is NOT set.	Cell
	[6]	AUTO_TOH_xx		Automatic TOH Generation, AUTO_TOH_xx =1 enables the TX core to automatically generate TOH bytes. All the FORCE_* register bits are valid if this bit is set. This bit should be set to 1 in Cell Mode. It can be set to 1or 0 in SONET Mode. If this bit is not set, then user has to provide all the TOH bytes or use the AUTO_SOH mode.	SONET
	[7]	FMPU_RESYNC1_xx		Single channel alignment FIFO reset. Rising edge sensitive. Write a 0 and then a 1 to enable this bit. When enabled, the read pointer in the alignment FIFO is reset to the middle of the FIFO. This bit is valid only when FMPU_SYNMODE_xx = 00 (no multi channel alignment)	SONET
30825 - AC 30835 - AD 30925 - BC 30935 - BD	[0:7]	LINK_NUM_TX_xx	00	Transmit Link Number, This value is transmitted in the “F1” byte of the TOH. This value is used to verify that the links are connected properly and is only used in the AUTO_TOH mode.	Both

Table 27. Per-Channel Status Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
3082A - AC 3083A - AD 3092A - BC 3093A - BD	[0:4]	RSVD	00	Reserved	—
	[5]	STAT_CELL_ALIGN_ERR_xx		STAT_CELL_ALIGN_ERR_xx = 1 same as CELL_ALIGN_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[6]	STAT_TX_URUN_ERR_xx		STAT_TX_URUN_ERR_xx = 1 same as TX_URUN_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[7]	STAT_TX_ORUN_ERR_xx		STAT_TX_ORUN_ERR_xx = 1 same as TX_ORUN_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
3082B -AC 3083B - AD 3092B - BC 3093B - BD	[0]	RSVD	00	Reserved	—
	[1]	STAT_OOF_xx		STAT_OOF_xx = 1 same as OOF_xx except that a 1 on this bit can NOT cause an interrupt	Both
	[2]	STAT_EX_SEQ_ERR_xx		STAT_EX_SEQ_ERR_xx = 1 same as EX_SEQ_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[3]	STAT_SEQ_ERR_xx		STAT_SEQ_ERR_xx = 1 same as SEQ_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[4]	STAT_CELL_BIP_ERR_xx		STAT_CELL_BIP_ERR_xx = 1 same as CELL_BIP_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[5]	STAT_B1_ERR_xx		STAT_B1_ERR_xx = 1 same as B1_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Both
	[6]	STAT_RX_FIFO_OVRUN_xx		STAT_RX_FIFO_OVRUN_xx = 1 same as RX_FIFO_OVRUN_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[7]	STAT_RDI_xx		STAT_RDI_xx = 1 same as RDI_xx except that a 1 on this bit can NOT cause an interrupt	Both
3082C - AC 3083C - AD 3092C - BC 3093C - BD	[0:7]	LINK_NUM_RX_xx	00	Link number received that is stored in the F1 byte position of the SONET TOH	Both
3082E - AC 3083E AD 3092E- BC 3093E - BD	[0:5]	RSVD	00	Reserved	—
	[6]	CH248_SYNC_xx		CH248_SYNC_xx = 1 indicates that A1A2 bytes have been detected by link xx for multi-channel alignment	SONET
	[7]	RX_LINK_GOOD_xx		RX_LINK_GOOD_xx = 1 indicates that frame has been acquired and the link has been stable. Goes high at an A1A2 boundary but can go low at any point in a frame due to excessive errors	Cell

Table 34. Per-Channel Control Register Descriptions – ORSO82G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30800 - AA 30810 - AB 30820 - AC 30830 - AD 30900 - BA 30910 - BB 30920 - BC 30930 - BD	[0:4]	RSVD	00	Reserved	—
	[5]	CELL_ALIGN_ERR_EN_xx		'1' = Alarm enabled for CELL_ALIGN_ERR_xx	Cell
	[6]	TX_URUN_ERR_EN_xx		'1' = Alarm enabled for TX_URUN_ERR_xx	Cell
	[7]	TX_ORUN_ERR_EN_xx		'1' = Alarm enabled for TX_ORUN_ERR_xx	Cell
30801 - AA 30811 - AB 30821 - AC 30831 - AD 30901 - BA 30911 - BB 30921 - BC 30931 - BD	[0]	RSVD	00	Reserved	—
	[1]	OOF_EN_xx		'1' = Alarm enabled for OOF_xx	Both
	[2]	EX_SEQ_ERR_EN_xx		'1' = Alarm enabled for EX_SEQ_ERR _xx	Cell
	[3]	SEQ_ERR_EN_xx		'1' = Alarm enabled for SEQ_ERR _xx	Cell
	[4]	CELL_BIP_ERR_EN_xx		'1' = Alarm enabled for CELL_BIP_ERR_xx	Cell
	[5]	B1_ERR_EN_xx		'1' = Alarm enabled for B1_ERR_xx	Both
	[6]	RX_FIFO_OVRUN_EN_xx		'1' = Alarm enabled for RX_FIFO_OVRUN_xx	Cell
	[7]	RDI_EN_xx		'1' = Alarm enabled for RDI_xx	Both
30802 - AA 30812 - AB 30822 - AC 30832 - AD 30902 - BA 30912 - BB 30922 - BC 30932 - BD	[0]	ENABLE_JUST_xx	00	ENABLE_JUST_xx =1 causes the core to interpret pointer bytes for positive or negative justification	SONET
	[1]	FMPU_STR_EN_xx		FMPU_STR_EN_xx = 1 enables a channel for alignment within a multi-channel alignment group	SONET
	[2:3]	FMPU_SYNMODE_xx		"00" - No channel alignment "01" - Twin channel alignment "10" - 4 channel alignment "11 - By-8 alignment	SONET
	[4]	DSCR_INH_xx		Descrambling Inhibit, DSCR_INH = 1 inhibits descrambling (in the Rx direction) and scrambling (in the Tx direction). When inhibiting the scrambler and descrambler the AUTO_B1_xx calculated and checked B1 value will always be incorrect.	Both
	[5]	FFRM_EN_xx		Fast Frame Enable, FFRM_EN=1 enables the fast frame mode.	Both
	[6]	AIS_ON_xx		Alarm Indication Signal (control), AIS_ON =1 forces AIS-L insertion.	Both
	[7]	AIS_ON_OOF_xx		Alarm Indication Signal on Out of Frame, AIS_ON_OOF =1 forces AIS-L insertion during OOF =1.	Both

Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A05	[0:2]	ERRCNT_CH	00	Error Count Channel Select, Control bits to select which channel's Section B1 error and Cell BIP error counts are recorded by the BIP_ERR_CNT and CELL_BIP_ERR_CNT registers. "000" - Channel AA, "001" - Channel AB, "010" - Channel AC, "011" - Channel AD, "100" - Channel BA, "101" - Channel BB, "110" - Channel BC, "111" - Channel BD	Both
	[3]	CELL_MODE_A1		Cell Mode Enable, CELL_MODE_A1 = 1 enables cell mode for the channel group AA and AB.	Cell
	[4]	CELL_MODE_A2		Cell Mode Enable, CELL_MODE_A2 = 1 enables cell mode for the channel group AC and AD.	Cell
	[5]	CELL_MODE_B1		Cell Mode Enable, CELL_MODE_B1 = 1 enables cell mode for the channel group BA and BB.	Cell
	[6]	CELL_MODE_B2		Cell Mode Enable, CELL_MODE_B2 = 1 enables cell mode for the channel group BC and BD.	Cell
	[7]	CELL_MODE_ALL		Cell Mode Enable, CELL_MODE_ALL = 1 enables cell mode for 8-link cell mode. CELL_MODE_[A1,A2,B1,B2] bits are not valid.	Cell
30A06	[0:4]	RSVD	00	Reserved	—
	[5:6]	RESET_PHASE		Reset Phase, Two bits to select delay phase for delaying the soft reset bit SOFT_RESET with respect to the synchronizing clock. Four delay phases can be selected through the values "00", "01", "10" and "11".	Both
	[7]	SOFT_RESET		Soft Reset, SOFT_RESET=1 resets the embedded core flip flops except for the software registers. This bit does not affect the state of the registers inside the SERDES blocks.	Both
30A07	[0:6]	RSVD	00	Reserved	—
	[7]	TX_CFG_DONE		Transmitter Configuration Done, Edge sensitive bit to indicate that all TX configuration bits are set. After all register bits have been set for Transmit direction, write a 0 and then a 1 to this bit.	Cell

Table 47. Pin Descriptions (Continued)

Symbol	I/O	Description
MPI_ACK	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_CLK	I	This is the PowerPC synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the Embedded System Bus. If MPI is used this will be the AMBA bus clock.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_TEA	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_RTRY	O	This pin requests the MPC860 to relinquish the bus and retry the cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
D[0:31]	I/O	Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	O	D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.[1]
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.[1]
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.[1]
TESTCFG (ORSO82G5 only)	I	During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user programmable I/O pin.[1]

1. The FPGA States of Operation section in the ORCA Series 4 FPGAs data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Table 48. FPSC Function Pin Descriptions (Continued)

Symbol	I/O	Description
HDOUTN_AB	O	High-speed CML transmit data output—SERDES Block A, channel B (not available in ORSO42G5).
HDOUTP_AB	O	High-speed CML transmit data output—SERDES Block A, channel B (not available in ORSO42G5).
HDOUTN_AC	O	High-speed CML transmit data output—SERDES Block A, channel C.
HDOUTP_AC	O	High-speed CML transmit data output—SERDES Block A, channel C.
HDOUTN_AD	O	High-speed CML transmit data output—SERDES Block A, channel D.
HDOUTP_AD	O	High-speed CML transmit data output—SERDES Block A, channel D.
HDOUTN_BA	O	High-speed CML transmit data output—SERDES Block B, channel A (not available in ORSO42G5).
HDOUTP_BA	O	High-speed CML transmit data output—SERDES Block B, channel A (not available in ORSO42G5).
HDOUTN_BB	O	High-speed CML transmit data output—SERDES Block B, channel B (not available in ORSO42G5).
HDOUTP_BB	O	High-speed CML transmit data output—SERDES Block B, channel B (not available in ORSO42G5).
HDOUTN_BC	O	High-speed CML transmit data output—SERDES Block B, channel C.
HDOUTP_BC	O	High-speed CML transmit data output—SERDES Block B, channel C.
HDOUTN_BD	O	High-speed CML transmit data output—SERDES Block B, channel D.
HDOUTP_BD	O	High-speed CML transmit data output—SERDES Block B, channel D.
Power and Ground		
VDDIB_AA	—	1.8V/1.5V power supply for high-speed serial input buffers (ORSO82G5 only).
VDDIB_AB	—	1.8V/1.5V power supply for high-speed serial input buffers (ORSO82G5 only).
VDDIB_AC	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_AD	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BA	—	1.8V/1.5V power supply for high-speed serial input buffers (ORSO82G5 only).
VDDIB_BB	—	1.8V/1.5V power supply for high-speed serial input buffers (ORSO82G5 only).
VDDIB_BC	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BD	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDOB_AA	—	1.8V/1.5V power supply for high-speed serial output buffers (ORSO82G5 only).
VDDOB_AB	—	1.8V/1.5V power supply for high-speed serial output buffers (ORSO82G5 only).
VDDOB_AC	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_AD	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BA	—	1.8V/1.5V power supply for high-speed serial output buffers (ORSO82G5 only).
VDDOB_BB	—	1.8V/1.5V power supply for high-speed serial output buffers (ORSO82G5 only).
VDDOB_BC	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BD	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDGB_A	—	1.5V guard band power supply.
VDDGB_B	—	1.5V guard band power supply.
VDD_ANA	—	1.5V Power supplies for SERDES analog transmit and receive circuitry.

1. Should be externally connected on board to 3.3V pull-up resistor.

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
M3	7 (CL)	6	IO	PL24D	PLCK1C	L11C
M4	7 (CL)	6	IO	PL24C	PLCK1T	L11T
N4	7 (CL)	6	IO	PL25C	A7/PPC_A21	-
M2	7 (CL)	6	IO	PL26D	A6/PPC_A20	L12C
M1	7 (CL)	6	IO	PL26C	A5/PPC_A19	L12T
N3	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	-
F11	-	-	VDD15	VDD15	-	-
N5	7 (CL)	8	IO	PL28D	A4/PPC_A18	-
M5	7 (CL)	-	VDDIO7	VDDIO7	-	-
N2	7 (CL)	8	IO	PL29D	A3/PPC_A17	L13C
N1	7 (CL)	8	IO	PL29C	A2/PPC_A16	L13T
G11	-	-	VSS	VSS	-	-
P2	7 (CL)	8	IO	PL30D	A1/PPC_A15	L14C
P1	7 (CL)	8	IO	PL30C	A0/PPC_A14	L14T
F12	-	-	VDD15	VDD15	-	-
P3	7 (CL)	8	IO	PL31D	DP0	L15C
P4	7 (CL)	8	IO	PL31C	DP1	L15T
R4	6 (BL)	1	IO	PL32D	D8	L16C
R3	6 (BL)	1	IO	PL32C	VREF_6_01	L16T
R2	6 (BL)	1	IO	PL33D	D9	L17C
R1	6 (BL)	1	IO	PL33C	D10	L17T
G12	-	-	VSS	VSS	-	-
T3	6 (BL)	2	IO	PL34D	-	-
P5	6 (BL)	-	VDDIO6	VDDIO6	-	-
T2	6 (BL)	2	IO	PL34B	-	L18C
T1	6 (BL)	2	IO	PL34A	-	L18T
U1	6 (BL)	3	IO	PL35B	D11	L19C
U2	6 (BL)	3	IO	PL35A	D12	L19T
R5	6 (BL)	-	VDDIO6	VDDIO6	-	-
V1	6 (BL)	3	IO	PL36B	VREF_6_03	L20C
V2	6 (BL)	3	IO	PL36A	D13	L20T
G13	-	-	VSS	VSS	-	-
W2	6 (BL)	4	IO	PL37B	-	L21C
W1	6 (BL)	4	IO	PL37A	VREF_6_04	L21T
Y1	6 (BL)	4	IO	PL39D	PLL_CK7C/HPPLL	L22C
Y2	6 (BL)	4	IO	PL39C	PLL_CK7T/HPPLL	L22T
U3	-	-	I	PTEMP	PTEMP	-
F13	-	-	VDD15	VDD15	-	-
V4	-	-	IO	LVDS_R	LVDS_R	-
V3	-	-	VDD33	VDD33	-	-
F17	-	-	VDD15	VDD15	-	-
W3	6 (BL)	5	IO	PB2A	DP2	-
AA2	6 (BL)	5	IO	PB2C	PLL_CK6T/PPLL	L23T
AB2	6 (BL)	5	IO	PB2D	PLL_CK6C/PPLL	L23C

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
AA3	6 (BL)	5	IO	PB4A	VREF_6_05	L24T
AB3	6 (BL)	5	IO	PB4B	DP3	L24C
T5	6 (BL)	-	VDDIO6	VDDIO6	-	-
H7	-	-	VSS	VSS	-	-
Y4	6 (BL)	6	IO	PB5C	VREF_6_06	L25T
W4	6 (BL)	6	IO	PB5D	D14	L25C
T8	6 (BL)	-	VDDIO6	VDDIO6	-	-
AA4	6 (BL)	7	IO	PB6C	D15	L26T
AB4	6 (BL)	7	IO	PB6D	D16	L26C
H8	-	-	VSS	VSS	-	-
W5	6 (BL)	7	IO	PB7C	D17	L27T
Y5	6 (BL)	7	IO	PB7D	D18	L27C
T9	6 (BL)	-	VDDIO6	VDDIO6	-	-
AA5	6 (BL)	7	IO	PB8C	VREF_6_07	L28T
AB5	6 (BL)	7	IO	PB8D	D19	L28C
H9	-	-	VSS	VSS	-	-
V6	6 (BL)	8	IO	PB9C	D20	-
G6	-	-	VDD15	VDD15	-	-
W6	6 (BL)	8	IO	PB10C	VREF_6_08	L29T
Y6	6 (BL)	8	IO	PB10D	D22	L29C
H10	-	-	VSS	VSS	-	-
AA6	6 (BL)	9	IO	PB11C	D23	L30T
AB6	6 (BL)	9	IO	PB11D	D24	L30C
U6	6 (BL)	-	VDDIO6	VDDIO6	-	-
W7	6 (BL)	9	IO	PB12C	VREF_6_09	L31T
Y7	6 (BL)	9	IO	PB12D	D25	L31C
H11	-	-	VSS	VSS	-	-
V7	6 (BL)	10	IO	PB14A	-	-
U7	6 (BL)	-	VDDIO6	VDDIO6	-	-
AA7	6 (BL)	10	IO	PB14C	VREF_6_10	L32T
AB7	6 (BL)	10	IO	PB14D	D28	L32C
V8	6 (BL)	11	IO	PB15A	-	-
H12	-	-	VSS	VSS	-	-
W8	6 (BL)	11	IO	PB15C	D29	L33T
Y8	6 (BL)	11	IO	PB15D	D30	L33C
U8	6 (BL)	11	IO	PB16A	-	-
AA8	6 (BL)	11	IO	PB16C	VREF_6_11	L34T
AB8	6 (BL)	11	IO	PB16D	D31	L34C
V9	5 (BC)	1	IO	PB17A	-	-
W9	5 (BC)	1	IO	PB17C	-	L35T
Y9	5 (BC)	1	IO	PB17D	-	L35C
U9	5 (BC)	1	IO	PB18A	-	-
AA9	5 (BC)	1	IO	PB18C	VREF_5_01	L36T
AB9	5 (BC)	1	IO	PB18D	-	L36C