Lattice Semiconductor Corporation - ORSO82G5-2FN680C Datasheet

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso82g5-2fn680c

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Dual Port RAMs

There are two independent memory blocks in the core. Each memory block has a capacity of 4K words by 36 bits. It has one read port, one write port, and four byte-write-enable (active-low) signals. The read data from the memory block is registered so that it works as a pipelined synchronous memory block. These memory blocks are completely independent of the backplane driver blocks. They are only accessible from the FPGA logic and are not connected to the system bus.

FPSC Configuration - Overview

Configuration of the ORSO42G5 and ORSO82G5 occurs in two stages: FPGA bit stream configuration and embedded core setup.

Prior to becoming operational, the FPGA goes through a sequence of states, including power-up, initialization, configuration, start-up, and operation. The FPGA logic is configured by standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet.

The options for the embedded core are set via registers that are accessed through the FPGA system bus. The system bus can be driven by an external PPC compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block, that drives the system by using the user interface and uses very little FPGA logic, is available in the *MPI/System Bus* application note (TN1017). This IP block sets up the embedded core via a state machine and allows the ORSO42G5 and ORSO82G5 to work in an independent system without an external MicroProcessor Interface.

Table 2. Transmit PLL Clock and Data Rates

Data Rate	Reference Clock	TCK78x	Rate
0.6 Gbps	75.00 MHz	18.75 MHz	Half
1.0 Gbps	125.00 MHz	31.25 MHz	Half
1.244 Gbps	155.52 MHz	38.88 MHz	Half
1.35 Gbps	168.75 MHz	42.19 MHz	Half
2.0 Gbps	125.00 MHz	61.50 MHz	Full
2.488 Gbps	155.52 MHz	77.76 MHz	Full
2.7 Gbps	168.75 MHz	84.38 MHz	Full

Notes:
1. The selection of full-rate or half-rate for a given reference clock speed is set by the TXHR bit in the transmit control register and can be set per channel. (For cell mode all channels of a group must have the same TXHR selection.)

The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. This means that the receive clocks are asynchronous between channels. The retimed data are deserialized and presented as a 8-bit parallel data on the output port. RWCKx receive byte clocks are divide-by-4 clocks of the RBC (recovered byte clock) clock provided by the SERDES. This is the clock used in the internal receive functions of the embedded core.

The reference clock is also used by the receive PLL for operation when the input data are not toggling appropriately. Table 3 shows the relationship between the data rates, the reference clock, and the RWCKx clocks.

Table 3. Receive PLL Clock and Data Rates

Data Rate	Reference Clock	RWCKx Clocks	Rate
0.6 Gbps	75.00 MHz	18.75 MHz	Half
1.0 Gbps	125.00 MHz	31.25 MHz	Half
1.244 Gbps	155.52 MHz	38.88 MHz	Half
1.35 Gbps	168.75 MHz	42.19 MHz	Half
2.0 Gbps	125.00 MHz	61.50 MHz	Full
2.488 Gbps	155.52 MHz	77.76 MHz	Full
2.7 Gbps	168.75 MHz	84.38 MHz	Full

Note: The selection of full-rate or half-rate for a given reference clock speed is set by the RXHR bit in the receive control register and can be set per channel. (For cell mode all channels of a group must have the same RXHR selection).

The differential reference clock is distributed to all channels in a SERDES block. Each channel has a differential buffer to isolate the clock from the other channels. The input clock is preferably a differential signal; however, the device can operate with a single-ended input. The input reference clock directly impacts the transmit data eye, so the clock should have low jitter. In particular, jitter components in the DC-5 MHz range should be minimized.

Detailed Description - SERDES Only Mode

The SERDES only (or bypass) mode is the simplest of the three operating modes for the ORSO42G5 and ORSO82G5. In this mode, all of the SONET and cell logic block functions are bypassed and data are transferred directly between the MUX and DEMUX blocks to and from the FPGA interface. This mode is utilized when the user wants to perform all data processing and uses only the SERDES portion of the Embedded Core. For example, this mode could be utilized to replace an existing design using stand-alone SERDES and FPGAs.

The basic data paths in the transmit and receive directions are shown in Figure 5. In general, the descriptions in this section are written to describe the SERDES only mode, although the “SERDES blocks” are also used in SONET and cell mode operation. At the backplane interface, data are transmitted and received serially over pairs

Figure 14. Byte Ordering of Input/Output Interface in STS-192 (Block STS-48) Mode

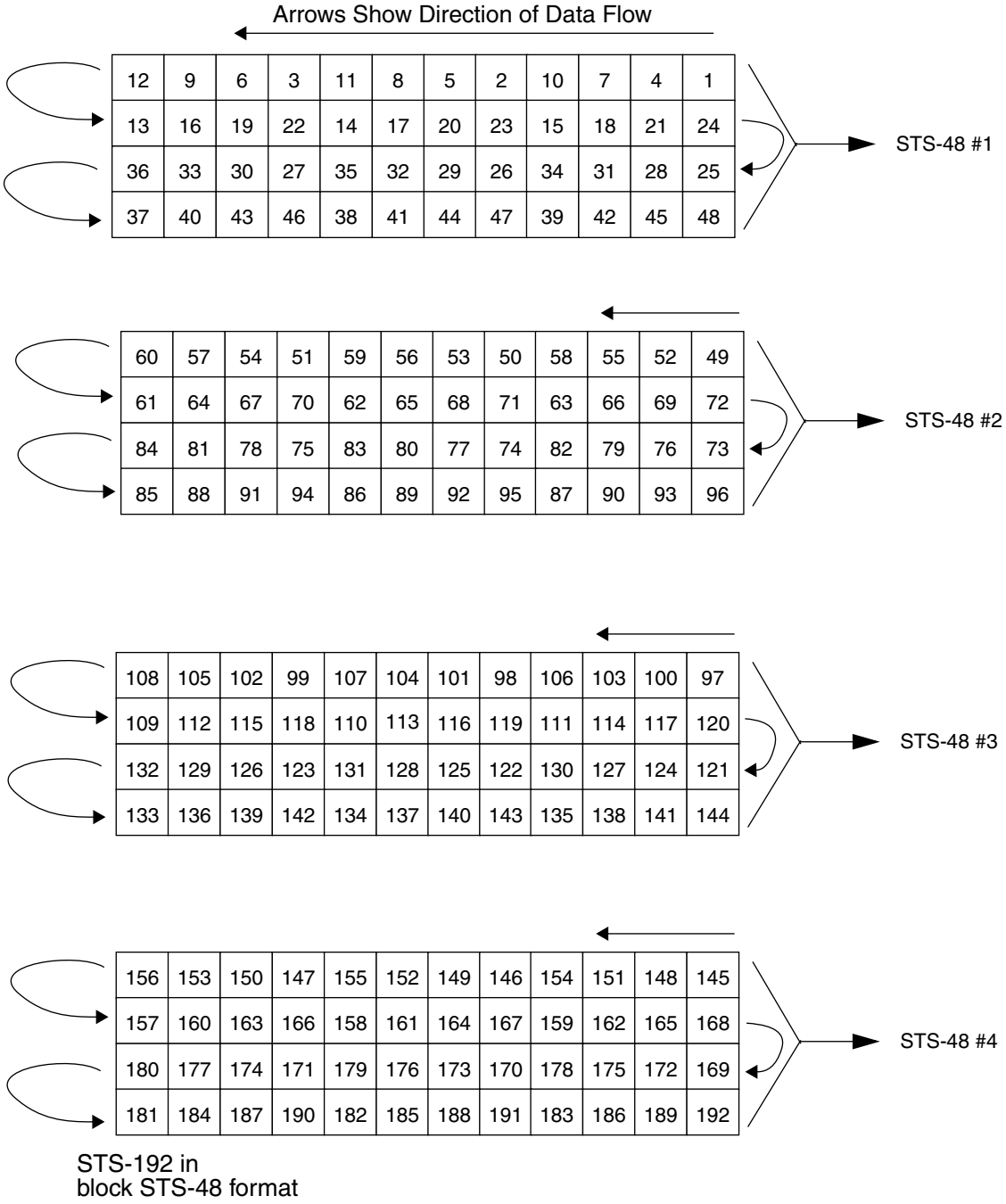


Table 5. Inserted TOH Values (All 0x) in AUTO_SOH Mode

A1 = F6	A2 = 28	J0
B1 = calculated, 1st. STS-1 B1 = 00, other STS-1s	E1	F1
D1	D2	D3
H1	H2	H3
B2	K1	K2
D4	D5	D6
D7	D8	D9
D10	D11	D12
S1	M1	E2

The TOH values inserted in AUTO_SOH mode are shown in Table 5. If a specific value is not listed in the table, the bytes are transmitted transparently from the FPGA logic as in the transparent mode. Optionally K2 can be inserted by the core using the FORCE_RDI_xx control register bits. A1/A2 and B1 insertion can be independently enabled.

The TOH values inserted in AUTO_TOH mode are shown in Table 6. The values are for all STS-1s in the STS-48 frame unless noted otherwise.

Table 6. Inserted TOH Values (All 0x) in AUTO_TOH Mode

A1 = F6	A2 = 28	J0 = STS-1 ID, every 4th. STS-1 J0 = 00, other STS-1s
B1 = calculated, 1st. STS-1 B1 = 00, other STS-1s	E1 = 00	F1 = link number, 1st. STS-1 F1 = 00, other STS-1s
D1 = 00	D2 = 00	D3 = 00
H1 = 62, 1st. STS-1 H1 = 93 other STS-1s	H2 = 0A, 1st. STS-1 H2 = FF other STS-1s	H3 = 00
B2 = 00	K1 = 00	K2 = 06 for RDI, K2 = 00 otherwise, 1st. STS-1 K2 = 00, other STS-1s
D4 = 00	D5 = 00	D6 = 00
D7 = 00	D8 = 00	D9 = 00
D10 = 00	D11 = 00	D12 = 00
S1 = 00	M1 = 00	E2 = 00

The TOH block can perform A1/A2 corruption by inverting the A1/A2 bytes and also can forces B1 errors by inverting the B1 byte. A RDI can be injected by forcing the K2 byte to “00000110”. In SONET mode, all TOH bytes can be transparently sent from the FPGA as an option. Error and RDI insertion are controlled by software register bits as shown in the Register Map tables.

Scramble Sub-block

The scrambler scrambles the incoming 32-bit data using the standard SONET polynomial $1 + x^6 + x^7$. The scrambler can be disabled by a software register bit.

32:8 MUX

The MUX block is responsible for converting 32 bits of data at 77.76 MHz to 8 bits of data at 311.04 MHz. It will contain a small elastic store for clock domain transfer between the write clock from the FPGA to the divide-by-4 clock from the SERDES output clock (XCK311). It is recommended to use the clocking scheme shown to guaran-

frame pulse, is less than the minimum threshold set by RX_FIFO_MIN. In the memory map section OOS is referred to as SYNC2_[A2,B2]_OOS, SYNC4_OOS. OVFL is referred to as SYNC2_[A2,B2]_OVFL, SYNC4_OVFL.

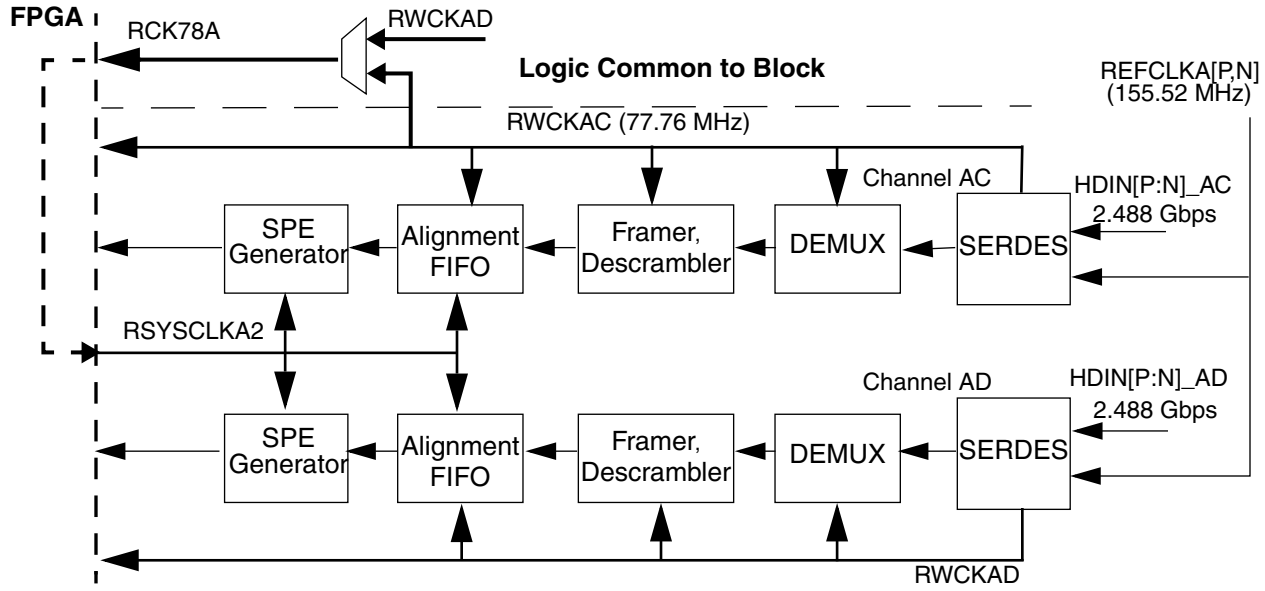
Receive Clocking for Multi-channel Alignment – ORSO42G5

There are a total of seven clocks for the receive path, from FPGA to the core. The two used in SONET mode are RSYSCLKA2 (for block A), and RSYSCLKB2 (for block B). The following diagrams show the recommended clock distribution approaches for SONET mode multi-channel alignment modes. Cell mode alignment is discussed in the section describing the Input Port Controller (IPC).)

SONET Mode Twin Alignment – ORSO42G5

Figure 22 describes the clocking scheme for twin alignment. In twin alignment, the valid channel pairs are AC,AD in block A and BC,BD in block B. The figure provides the clocking scheme for block A as an example. RSYSCLKA2 should be sourced from RCK78A, RWCKAC or RWCKAD. For the ORSO42G5, the use of RCK78A is recommended since it uses primary clock routing resources. This clocking approach provides the required 0 ppm clock frequency matching for each pair and provides flexibility in applications where the two pairs are received from asynchronous sources.

Figure 22. Receive Clocking Diagram for Twin Alignment in Block A – ORSO42G5

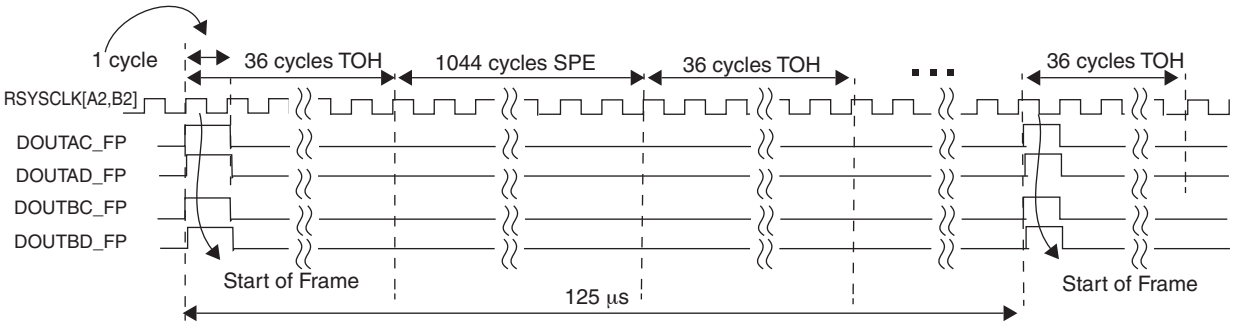


SONET Mode Quad Alignment – ORSO42G5

Figure 23 shows the clocking scheme for four-channel alignment. In this application, both clocks RSYSCLKA2 and RSYSCLKB2 should be sourced from a common clock. Either RCK78A or RCK78B can be used as a common clock source. The figure shows RCK78A being used as the clock source.

Figure 31 shows the quad alignment mode in the ORSO42G5.

Figure 31. Receive SONET Mode, Quad Alignment Mode – ORSO42G5



Clocks
RSYSCLKA2 and RSYSYSCLKB2 are sourced by RCK78A

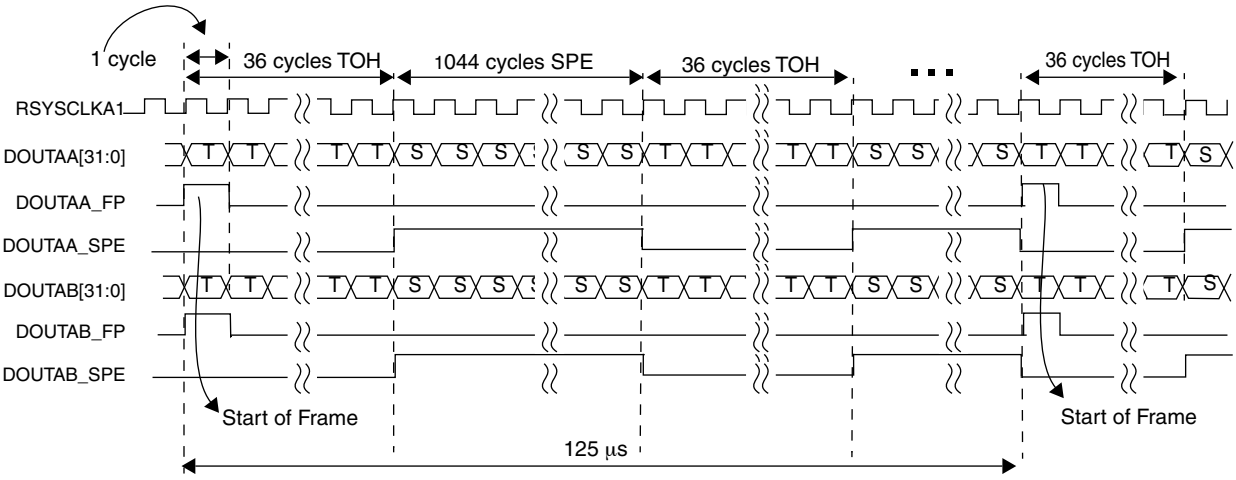
SONET Mode Receive Timing – ORSO82G5

This section contains timing diagrams for major interfaces of this block to the FPGA logic when SONET frames are to be transferred.

- When operating in SONET mode, the entire SONET frame is sent to the FPGA. In multi-channel alignment mode(s), data from all channels within an alignment group are aligned to the A1A2 framing bytes.
- Each SONET frame is 125µs. The frame starts with 36 clock cycles (77.76 MHz) of TOH followed by 1044 clock cycles of SPE, followed by 36 clock cycles of TOH, 1044 cycles of SPE.
- The DOUTxx_SPE signal indicates TOH or SPE in the data (low for TOH, high for SPE)
- Twin pairs are AA, AB (group A1), AC, AD (group A2), BA, BB (group B1) and BC, BD (group B2)

Figure 32 shows the SONET twin alignment mode timing for the ORSO82G5. The frame pulse and SPE indicators are show for each of the two channels (AA, AB) in twin alignment.

Figure 32. Receive Clocking Diagram for SONET Mode Twin Alignment in Block A – ORSO82G5



Clocks
RSYSCLKA1 is the read clock used for group A1
RSYSCLKA2 is the read clock used for group A2
RSYSCLKB1 is the read clock used for group B1
RSYSBLKB2 is the read clock used for group B2

Data
T Represents TOH
S Represents SPE
DOUTxx-SPE is high for SPE, low for TOH

TCK156[A:B]: This is a muxed output from the core to the FPGA across the core-FPGA interface of one of the 4 transmit SERDES clocks per block. There is one clock output per SERDES block. It is derived from REFCLK_[A:B] and runs at the reference clock frequency.This clock is available from the core in all modes and used by the core in cell mode.

TCK78[A:B]: This is a muxed output from the core to the FPGA across the core-FPGA interface of one of the 4 transmit SERDES clocks per block. There is one clock output per SERDES block. It is derived from REFCLK_[A:B] and runs at half the reference clock frequency. This clock is available from the core in all modes and used by the core in SONET and SERDES-only mode.

TCK39[A:B]: This is a muxed output from the core to the FPGA across the core-FPGA interface of one of the 4 transmit SERDES clocks per block. There is one clock output per SERDES block. It is derived from REFCLK_[A:B] and runs at a quarter of the reference clock frequency. This clock is available from the core in all modes.

TSYSCLK[AA,…BD]: These clocks are inputs to the SERDES block A and B respectively from the FPGA. These are used by each channel to control the timing of the Transmit Data Path in the SONET and SERDES-only modes. (They are not used in cell mode.) To guarantee correct transmit operation theses clocks must be frequency locked within 0 ppm to TCK78[A:B].

SYSCLK156 [A:B][1:2] and SYSCLK156 8: These clocks are inputs to the SERDES block A and B from the FPGA. and are used by the cell processing blocks within the embedded core. Clocks SYSCLK156 A[1:2] are used by channels in the SERDES block A and SYSCLK156 B[1:2] by channels in the SERDES block B for two-link cell mode operation. SYSCLK156 8 is used by both blocks for eight-link cell mode in the ORSO82G5.

Sample Initialization Sequences – ORSO42G5

The following paragraphs show sample control register write sequences for initialization and resynchronization for the major modes of the device. Hexadecimal values will be shown for the data to be written into the control registers. For these values bit 0 will be the MSb while bit 7 is the LSb. For the per-channel control registers, only the first register address is shown. The other per-channel control registers must also be initialized for the desired mode.

1. SERDES-Only Mode Initialization – ORSO42G5

- Set SERDES Only mode (per channel, channel AA selected for sample initialization)
  - 30823 and 30833 40
- Set SERDES PLL to Lock to Data signal (per channel, channel AA selected for sample initialization)
  - 30824 and 30834 80
- Toggle SOFT_RESET once all clocks have stabilized
  - 30A06 01
  - 30A06 00
- Provide a rising edge on the DINxx_START signal

2. SONET Mode Initialization – ORSO42G5

This sample initialization uses the alignment FIFO for two channel alignment and Auto_SOH mode

- Set Dual Channel Alignment (per channel, channels AC and AD)
  - 30822 and 30833 10
- Set SERDES PLL to Lock to Data signal (per channel, channels AC and AD)
  - 30824 and 30834 80
- Set Auto_SOH Mode (per channel, channels AC and AD)
  - 30826 and 30836 03

Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30826 - AC 30836 - AD 30926 - BC 30936 - BD	[0:5]	RSVD	00	Reserved	—
	[6]	AUTO_B1_xx		AUTO_B1_xx = 0, B1 is not inserted by the embedded core AUTO_B1_xx = 1, B1 is calculated and inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	Both
	[7]	AUTO_A1A2_xx		AUTO_A1A2_xx = 0, A1/A2 bytes are not inserted by the embedded core AUTO_A1A2_xx = 1, A1/A2 bytes inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	

Table 27. Per-Channel Status Register Descriptions – ORSO42G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
Channel Status Registers (Read Only) xx = [AC, AD, BC, BD]					
30828 - AC 30838 - AD 30928 - BC 30938 - BD	[0:4]	RSVD	00	Reserved	—
	[5]	CELL_ALIGN_ERR_xx		Cell Alignment Error, CELL_ALIGN_ERR = 1 indicates that the internal transmit frame processor did not detect a start of cell indicator when it was expecting a new cell. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[6]	TX_URUN_ERR_xx		Transmit Underrun Error, TX_URUN_ERR = 1 indicates an underrun error in the transmit Asynchronous FIFO. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[7]	TX_ORUN_ERR_xx		Transmit Overrun Error, TX_ORUN_ERR = 1 indicates an overrun error in the transmit Asynchronous FIFO. The TX FIFO is designed to not overflow since it sends backpressure signal to the FPGA when it cannot accept more cells. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
30829 - AC 30839 - AD 30929 - BC 30939 - BD	[0]	RSVD	00	Reserved	—
	[1]	OOF_xx		OOF_xx = 1 indicates OOF has been detected in this link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm	Both
	[2]	EX_SEQ_ERR_xx		Excessive Sequence Errors, EX_SEQ_ERR = 1 indicates that three consecutive cells containing sequence errors have been detected in this link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[3]	SEQ_ERR_xx		Sequence Error, SEQ_ERR = 1 indicates that a sequence error has been detected for a cell on this link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	]4]	CELL_BIP_ERR_xx		Cell mode BIP Error, CELL_BIP_ERR = 1 indicates that a BIP error has been detected in a cell on the link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[5]	B1_ERR_xx		Bit Interleaved Parity Error, B1_ERR = 1 indicates that a Section B1 error has been detected on the link.If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Both
	[6]	RX_FIFO_OVRUN_xx		Receive FIFO Overrun, RX_FIFO_OVRUN_xx = 1 indicates that the asynchronous RX FIFO has detected an overrun condition. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[7]	RDI_xx		Remote Defect Indication, RDI = 1 indicates that a RDI has been detected on the link. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm	Both

Table 28. Common Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A09	[0:7]	B1_ERR_CNT	00	Error counter that increments when a section B1 error is detected on a link. The link is selected using ERRCNT_CHSEL. This counter is cleared on read.	Both
30A0A	[0:7]	CELL_BIP_ERR_CNT	00	Cell BIP Error Counter, Error counter that increments when a Cell BIP error is detected on a link. The link being monitored is selected using ERRCNT_CHSEL. This counter is cleared on read.	Cell
30A0B	[0:2]	RSVD	00	Reserved	
	[3]	CELL_DRP_B2		Cell Drop, CELL_DRP_B2 = 1 indicates that a cell has been dropped from the link group BC and BD	Cell
	[4]	RSVD		Reserved	—
	[5]	CELL_DRP_A2		Cell Drop, CELL_DRP_A2 = 1 indicates that a cell has been dropped from the link group AC and AD	Cell
	[6:7]	RSVD		Reserved	—
30A0C	[0:1]	RSVD	00	Reserved	
	[2]	SYNC2_B2_OOS		SYNC2_B2_OOS = 1 indicates that channels cannot be aligned within the links BC and BD in SONET mode	SONET
	[3:4]	RSVD		Reserved	—
	[5]	SYNC2_A2_OOS		SYNC2_A2_OOS = 1 indicates that channels cannot be aligned within the AC and AD links in SONET mode	SONET
	[6:7]	SYNC2_A1_OOS		Reserved	—
30A0D	[0:1]	RSVD	00	Reserved	—
	[2]	SYNC2_B2_OVFL		SYNC2_B2_OVFL = 1 indicates that the alignment FIFO(s) in the links BC and BD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[3:4]	RSVD		Reserved	—
	[5]	SYNC2_A2_OVFL		SYNC2_A2_OVFL = 1 indicates that the alignment FIFO(s) in the links AC and AD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[6:7]	RSVD		Reserved	—
30A0E	[0:2]	RSVD	00	Reserved	
	[3]	BDL_ALIGN_ERR_B2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs BC and BD	Cell
	[4]	RSVD		Reserved	—
	[5]	BDL_ALIGN_ERR_A2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs AC and AD	Cell
	[6:7]	RSVD		Reserved	—

Table 34. Per-Channel Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30806 - AA 30816 - AB 30826 - AC 30836 - AD 30906 - BA 30916 - BB 30926 - BC 30936 - BD	[0:5]	RSVD	00	Reserved	—
	[6]	AUTO_B1_xx		AUTO_B1_xx = 0, B1 is not inserted by the embedded core AUTO_B1_xx = 1, B1 is calculated and inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	Both
	[7]	AUTO_A1A2_xx		AUTO_A1A2_xx = 0, A1/A2 bytes are not inserted by the embedded core AUTO_A1A2_xx = 1, A1/A2 bytes inserted by the embedded core AUTO_TOH_xx = 1 overrides this bit	

Table 35. Per-Channel Status Register Descriptions – ORSO82G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
Channel Status Registers (Read Only) xx = [AA,...,BD]					
30808 - AA 30818 - AB 30828 - AC 30838 - AD 30908 - BA 30918 - BB 30928 - BC 30938 - BD	[0:4]	RSVD	00	Reserved	—
	[5]	CELL_ALIGN_ERR_xx		Cell Alignment Error, CELL_ALIGN_ERR = 1 indicates that the internal transmit frame processor did not detect a start of cell indicator when it was expecting a new cell. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[6]	TX_URUN_ERR_xx		Transmit Underrun Error, TX_URUN_ERR = 1 indicates an underrun error in the transmit Asynchronous FIFO. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell
	[7]	TX_ORUN_ERR_xx		Transmit Overrun Error, TX_ORUN_ERR = 1 indicates an overrun error in the transmit Asynchronous FIFO. The TX FIFO is designed to not overflow since it sends backpressure signal to the FPGA when it cannot accept more cells. If the corresponding alarm enable bit has been set, a 1 on this bit will cause an alarm.	Cell

Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A03	[0]	NO_TX_RDI_EXSEQ	00	Not Transmission of RDI, If NO_TX_RDI_EXSEQ = 1, a transmit link will not send data if its corresponding receive link is not good due to excessive sequence errors. If this bit is set to 0, a transmit link will still send data even if its corresponding receive link has excessive sequence errors. This bit should always be set during simulation and in SONET mode.	Both
	[1]	AUTO_BUNDLE		Automatic (Link) Bundle, AUTO_BUNDLE = 1 allows a link within a link group to remain active even when another link within that group is defective. Cell data from all links within that group will continue to be sent to the FPGA. If this bit is set to 0, then all links within a link group must be good before cell data are read from the links by the IPC and passed to the FPGA.	Cell
	[2]	RSVD		Reserved	—
	[3]	REJOIN_A		Link Rejoin, REJOIN = 1 forces any link in a SERDES block to reassert a “RX link good” signal automatically when three consecutive sequence numbers are correct on that link.	Cell
	[4]	AUTO_REMOVE_A		Automatic (Link) Remove, AUTO_REMOVE = 1 indicates that any link in a SERDES block which sees three excessive sequence errors should deassert the “RX link good” signal which will cause the link to be inactive.	Cell
	[5]	RSVD		Reserved	—
	[6]	REJOIN_B		Link Rejoin, REJOIN = 1 forces any link in a SERDES block to reassert a “RX link good” signal automatically when three consecutive sequence numbers are correct on that link.	Cell
	[7]	AUTO_REMOVE_B		AUTO_REMOVE_B = 1 indicates that any link in SERDES block B which sees three excessive sequence errors should deassert the “RX link good” signal which will cause the link to be inactive.	Cell

Table 47. Pin Descriptions (Continued)

Symbol	I/O	Description
MPI_ACK	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_CLK	I	This is the PowerPC synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the Embedded System Bus. If MPI is used this will be the AMBA bus clock.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_TEA	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_RTRY	O	This pin requests the MPC860 to relinquish the bus and retry the cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
D[0:31]	I/O	Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	O	D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.[1]
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.[1]
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.[1]
TESTCFG (ORSO82G5 only)	I	During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user programmable I/O pin.[1]

1. The FPGA States of Operation section in the ORCA Series 4 FPGAs data sheet contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Package Information

Package Pinouts

Table 50 provides the number of user-programmable I/Os available for each available package.

Table 50. I/O Summary

Device	ORSO42G5	ORSO82G5
User programmable I/O	204	372
Available programmable differential pair pins	166	330
FPGA configuration pins	7	7
FPGA dedicated function pins	2	2
Core function pins	32	71
VDD15	49	63
VDD33	8	10
VDDIO	34	32
VSS	112	91
VDDGB	2	2
VDDIB	4	8
VDDOB	8	12
VDD_ANA	22	8
Core LV_REF pins	1	1
No connect	0	2
Total package pins	484	680

Table 51 provides the package pin and pin function for the ORSO42G5 and ORSO82G5 FPSC and packages. The bond pad name is identified in the PIO nomenclature used in the ispLEVER System software design editor. The Bank column provides information as to which output voltage level bank the given pin is in. The Group column provides information as to the group of pins the given pin is in. This is used to show which VREF pin is used to provide the reference voltage for single-ended limited-swing I/Os. If none of these buffer types (such as SSTL, GTL, HSTL) are used in a given group, then the VREF pin is available as an I/O pin.

When the number of FPGA bond pads exceeds the number of package pins, bond pads are unused. When the number of package pins exceeds the number of bond pads, package pins are left unconnected (no connects). When a package pin is to be left as a no connect for a specific die, it is indicated as a note in the device column for the FPGA. The tables provide no information on unused pads.

The differential pairs within each bank are physically arranged so that the ball locations for the pair are adjacent in either the horizontal, vertical or diagonal directions.

VREF pins, shown in the Pin Description columns in Table 51 are associated to the bank and group (e.g., VREF_TL_01 is the VREF for group one of the Top Left (TL) bank.

Table 51. ORSO42G5 484-pin PBGAM Pinout

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
E4	-	-	O	PRD_DATA	RD_DATA/TDO	-
C20	-	-	VDD15	VDD15	-	-
D3	-	-	I	PRESET_N	RESET_N	-
F5	-	-	I	PRD_CFG_N	RD_CFG_N	-
F4	-	-	I	PPRGRM_N	PRGRM_N	-
C2	0 (TL)	7	IO	PL2D	PLL_CK0C/HPPLL	L1C

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
M3	7 (CL)	6	IO	PL24D	PLCK1C	L11C
M4	7 (CL)	6	IO	PL24C	PLCK1T	L11T
N4	7 (CL)	6	IO	PL25C	A7/PPC_A21	-
M2	7 (CL)	6	IO	PL26D	A6/PPC_A20	L12C
M1	7 (CL)	6	IO	PL26C	A5/PPC_A19	L12T
N3	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	-
F11	-	-	VDD15	VDD15	-	-
N5	7 (CL)	8	IO	PL28D	A4/PPC_A18	-
M5	7 (CL)	-	VDDIO7	VDDIO7	-	-
N2	7 (CL)	8	IO	PL29D	A3/PPC_A17	L13C
N1	7 (CL)	8	IO	PL29C	A2/PPC_A16	L13T
G11	-	-	VSS	VSS	-	-
P2	7 (CL)	8	IO	PL30D	A1/PPC_A15	L14C
P1	7 (CL)	8	IO	PL30C	A0/PPC_A14	L14T
F12	-	-	VDD15	VDD15	-	-
P3	7 (CL)	8	IO	PL31D	DP0	L15C
P4	7 (CL)	8	IO	PL31C	DP1	L15T
R4	6 (BL)	1	IO	PL32D	D8	L16C
R3	6 (BL)	1	IO	PL32C	VREF_6_01	L16T
R2	6 (BL)	1	IO	PL33D	D9	L17C
R1	6 (BL)	1	IO	PL33C	D10	L17T
G12	-	-	VSS	VSS	-	-
T3	6 (BL)	2	IO	PL34D	-	-
P5	6 (BL)	-	VDDIO6	VDDIO6	-	-
T2	6 (BL)	2	IO	PL34B	-	L18C
T1	6 (BL)	2	IO	PL34A	-	L18T
U1	6 (BL)	3	IO	PL35B	D11	L19C
U2	6 (BL)	3	IO	PL35A	D12	L19T
R5	6 (BL)	-	VDDIO6	VDDIO6	-	-
V1	6 (BL)	3	IO	PL36B	VREF_6_03	L20C
V2	6 (BL)	3	IO	PL36A	D13	L20T
G13	-	-	VSS	VSS	-	-
W2	6 (BL)	4	IO	PL37B	-	L21C
W1	6 (BL)	4	IO	PL37A	VREF_6_04	L21T
Y1	6 (BL)	4	IO	PL39D	PLL_CK7C/HPPLL	L22C
Y2	6 (BL)	4	IO	PL39C	PLL_CK7T/HPPLL	L22T
U3	-	-	I	PTEMP	PTEMP	-
F13	-	-	VDD15	VDD15	-	-
V4	-	-	IO	LVDS_R	LVDS_R	-
V3	-	-	VDD33	VDD33	-	-
F17	-	-	VDD15	VDD15	-	-
W3	6 (BL)	5	IO	PB2A	DP2	-
AA2	6 (BL)	5	IO	PB2C	PLL_CK6T/PPLL	L23T
AB2	6 (BL)	5	IO	PB2D	PLL_CK6C/PPLL	L23C

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
K13	-	-	VSS	VSS	-	-
B21	1 (TC)	9	IO	PT31D	-	L55C
A21	1 (TC)	9	IO	PT31C	VREF_1_09	L55T
E13	1 (TC)	-	VDDIO1	VDDIO1	-	-
D14	1 (TC)	9	IO	PT30D	-	L56C
C14	1 (TC)	9	IO	PT30C	-	L56T
K14	-	-	VSS	VSS	-	-
B20	1 (TC)	9	IO	PT29D	-	L57C
A20	1 (TC)	9	IO	PT29C	-	L57T
N7	-	-	VDD15	VDD15	-	-
B19	1 (TC)	1	IO	PT28D	-	L58C
A19	1 (TC)	1	IO	PT28C	-	L58T
L8	-	-	VSS	VSS	-	-
D13	1 (TC)	1	IO	PT27D	VREF_1_01	L59C
C13	1 (TC)	1	IO	PT27C	-	L59T
E18	1 (TC)	-	VDDIO1	VDDIO1	-	-
A18	1 (TC)	1	IO	PT27B	-	L60C
B18	1 (TC)	1	IO	PT27A	-	L60T
A17	1 (TC)	2	IO	PT26D	-	L61C
B17	1 (TC)	2	IO	PT26C	VREF_1_02	L61T
L9	-	-	VSS	VSS	-	-
D12	1 (TC)	2	IO	PT25D	-	L62C
C12	1 (TC)	2	IO	PT25C	-	L62T
E19	1 (TC)	-	VDDIO1	VDDIO1	-	-
A16	1 (TC)	3	IO	PT24D	-	L63C
B16	1 (TC)	3	IO	PT24C	VREF_1_03	L63T
A15	1 (TC)	3	IO	PT23D	-	L64C
B15	1 (TC)	3	IO	PT23C	-	L64T
F16	1 (TC)	-	VDDIO1	VDDIO1	-	-
E11	1 (TC)	3	IO	PT22D	-	-
L10	-	-	VSS	VSS	-	-
D11	1 (TC)	4	IO	PT21D	-	L65C
C11	1 (TC)	4	IO	PT21C	-	L65T
A14	1 (TC)	4	IO	PT20D	-	L66C
B14	1 (TC)	4	IO	PT20C	-	L66T
A13	1 (TC)	4	IO	PT19D	-	L67C
B13	1 (TC)	4	IO	PT19C	VREF_1_04	L67T
G14	1 (TC)	-	VDDIO1	VDDIO1	-	-
L11	-	-	VSS	VSS	-	-
N15	-	-	VDD15	VDD15	-	-
D10	1 (TC)	5	IO	PT18D	PTCK1C	L68C
C10	1 (TC)	5	IO	PT18C	PTCK1T	L68T
A12	1 (TC)	5	IO	PT17D	PTCK0C	L69C
B12	1 (TC)	5	IO	PT17C	PTCK0T	L69T

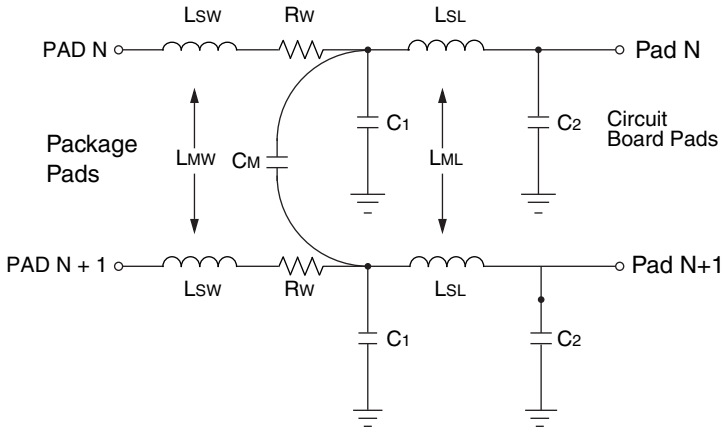
Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
M10	-	-	VSS	VSS	-	-
M11	-	-	VSS	VSS	-	-
M12	-	-	VSS	VSS	-	-
M13	-	-	VSS	VSS	-	-
M14	-	-	VSS	VSS	-	-
N8	-	-	VSS	VSS	-	-
N9	-	-	VSS	VSS	-	-
N10	-	-	VSS	VSS	-	-
N11	-	-	VSS	VSS	-	-
N12	-	-	VSS	VSS	-	-
N13	-	-	VSS	VSS	-	-
N14	-	-	VSS	VSS	-	-
P7	-	-	VSS	VSS	-	-
P8	-	-	VSS	VSS	-	-
P9	-	-	VSS	VSS	-	-
P10	-	-	VSS	VSS	-	-
P11	-	-	VSS	VSS	-	-
P12	-	-	VSS	VSS	-	-
P13	-	-	VSS	VSS	-	-
P14	-	-	VSS	VSS	-	-
R7	-	-	VSS	VSS	-	-
R8	-	-	VSS	VSS	-	-
R9	-	-	VSS	VSS	-	-
R10	-	-	VSS	VSS	-	-
R11	-	-	VSS	VSS	-	-
R12	-	-	VSS	VSS	-	-
R13	-	-	VSS	VSS	-	-
R14	-	-	VSS	VSS	-	-
AA1	-	-	VSS	VSS	-	-
AA19	-	-	VSS	VSS	-	-
AA20	-	-	VSS	VSS	-	-
AA21	-	-	VSS	VSS	-	-
AA22	-	-	VSS	VSS	-	-
AB1	-	-	VSS	VSS	-	-
AB19	-	-	VSS	VSS	-	-
AB20	-	-	VSS	VSS	-	-
AB21	-	-	VSS	VSS	-	-
AB22	-	-	VSS	VSS	-	-

Table 54. ORCA Typical Package Parasitics

L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
3.8	1.3	250	1.0	1.0	0.3	2.8-5	0.5 -1

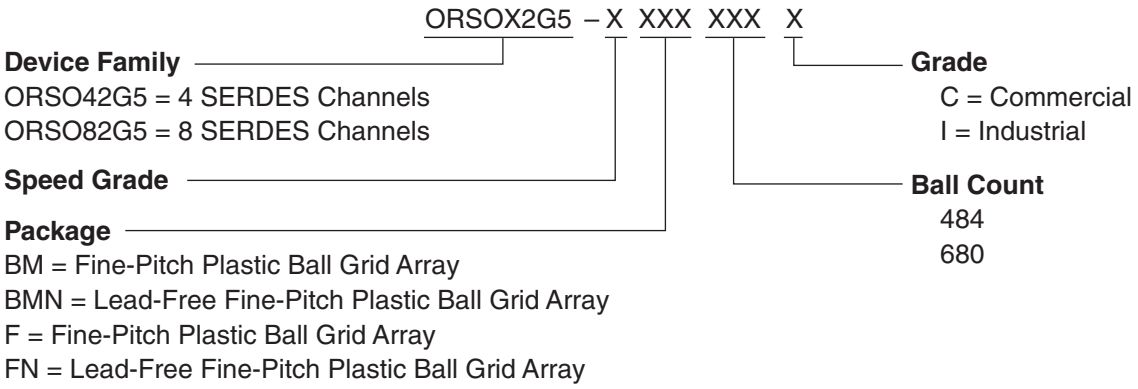
Figure 53. Package Parasitics



Package Outline Drawings

Package Outline Drawings for the 484-ball PBGAM (fpBGA) used for the ORSO42G5 and 680-ball PBGAM (fpBGA) used for the ORSO82G5 are available at the Package Diagrams section of the Lattice Semiconductor web site at www.latticesemi.com.

Part Number Description



Device Type Options

Device	Voltage
ORSO42G5	1.5V internal 3.3/2.5/1.8/1.5V I/O
ORSO82G5	1.5V internal 3.3/2.5/1.8/1.5V I/O

Ordering Information

Conventional Packaging

Commercial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORSO42G5	ORSO42G5-3BM484C	3	PBGAM	484	C
	ORSO42G5-2BM484C	2	PBGAM	484	C
	ORSO42G5-1BM484C	1	PBGAM	484	C
ORSO82G5	ORSO82G5-3F680C	3	PBGAM (No Heat Spreader)	680	C
	ORSO82G5-2F680C	2	PBGAM (No Heat Spreader)	680	C
	ORSO82G5-1F680C	1	PBGAM (No Heat Spreader)	680	C
	ORSO82G5-3BM680C[2]	3	PBGAM (With Heat Spreader)	680	C
	ORSO82G5-2BM680C[2]	2	PBGAM (With Heat Spreader)	680	C
	ORSO82G5-1BM680C[2]	1	PBGAM (With Heat Spreader)	680	C

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.
2. BM680 package was converted to F680 via PCN#09A-08.