Lattice Semiconductor Corporation - ORSO82G5-2FN680I Datasheet

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Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/orso82g5-2fn680i

Supported Data Formats

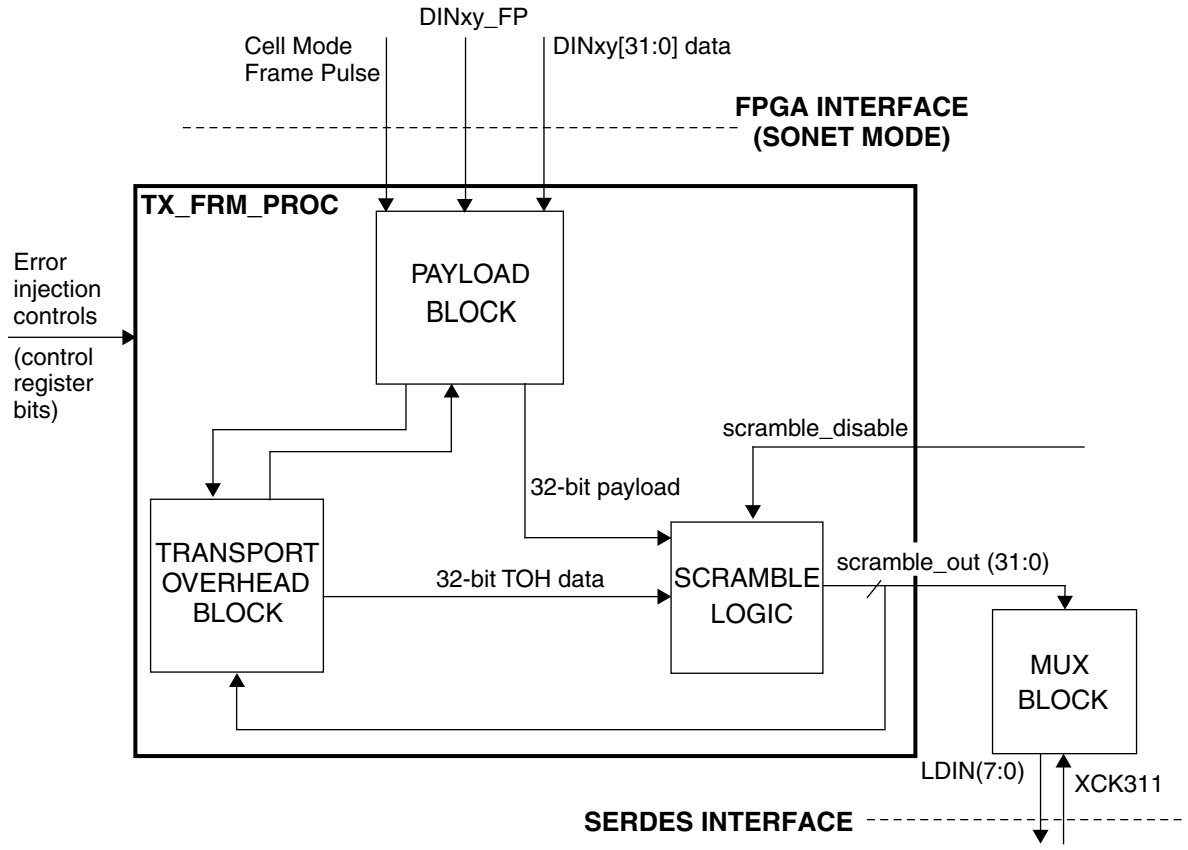
The ORSO42G5 and ORSO82G5 in the SONET mode support the following formats:

- Single OC-48 on each of the channels at a bit rate of 2.488 Gbps.
- OC-192 received in block OC-48 format on four channels at a combined rate of 9.952 Gbps.

The ORSO42G5 and ORSO82G5 SERDES will operate at the OC-12 rate of 622 MHz. For this rate, REFCLK is set to 77 MHz and the SERDES is used in half rate mode. However the embedded core SONET framing/processing logic is fixed at the OC-48 rate and therefore can not talk directly with standard STS-12 devices. In order to interoperate with standard STS-12 devices, the user must bypass the SONET functionality in the ORSO embedded core (SERDES-only mode) and implement all framing, TOH and scrambling/descrambling functionality in FPGA logic.

Figure 13 reveals the byte-ordering of the individual STS-48 streams. STS-192 is supported but it must be received in the block STS-48 format as shown in Figure 14. Each OC-48 stream is composed of byte-interleaved OC-1 data as described in GR-253 standard. Note that the SPE data is not touched by the core.

Figure 16. TX Frame Processor (TFP) Block Diagram



Payload Sub-block

The Payload sub block is activated by the cell mode frame pulse (cell mode) or DINxx_FP from FPGA (SONET mode). A pulse on this signal indicates the start of a frame.

In SONET mode, only two types of data bytes are in each frame:

- TOH bytes
- SPE data bytes

There are N x 3 (N = 48) bytes of TOH per row and there are a total of 9 rows in a SONET frame. The rest of the bytes in each row are SPE data bytes in SONET mode.

TOH Sub-block

This block is responsible formatting the 144 (48 x 3) bytes of TOH at the beginning of each row of the transport frame. All TOH bytes may be transmitted transparently from the FPGA logic using the transparent mode. Alternately, some or all TOH bytes may be inserted by the TOH block (AUTO_SOH and AUTO_TOH mode). The TOH data is transferred across the FPGA/core interface as 32-bit words, hence 36 clock cycles (12 x 3) are needed to transfer a TOH row. TOH insertion is controlled by software register bits as shown in the Register Map tables.

ment FIFO should be at exactly the same frequency (0 ppm difference), i.e., from a common clock source. Later in this data sheet, Figures 22, 23, 27, 28, and 29 show the recommended clocking scheme to adhere to this requirement. In addition, supervisory features such as BIP error check, OOF check, RDI monitoring and AIS-L insertion during OOF are also implemented. All the supervisory features are controlled through programmable register bits.

Framer

The frame and byte phase of the bits within the 32-bit word from the DEMUX is random. For each of the STS-48 channels, the framer outputs 4 bytes (32-bits) that are frame-aligned and a frame pulse that is one clock-wide. The transition from A1 bytes to A2 bytes should happen on a 32-bit boundary. If any two consecutive bytes of the 4-byte-aligned word match the A1-A2 pattern (0xF628 in standard SONET framing), the byte-aligned word will be byte rotated to achieve frame alignment.

Framer State Machine (FSM)

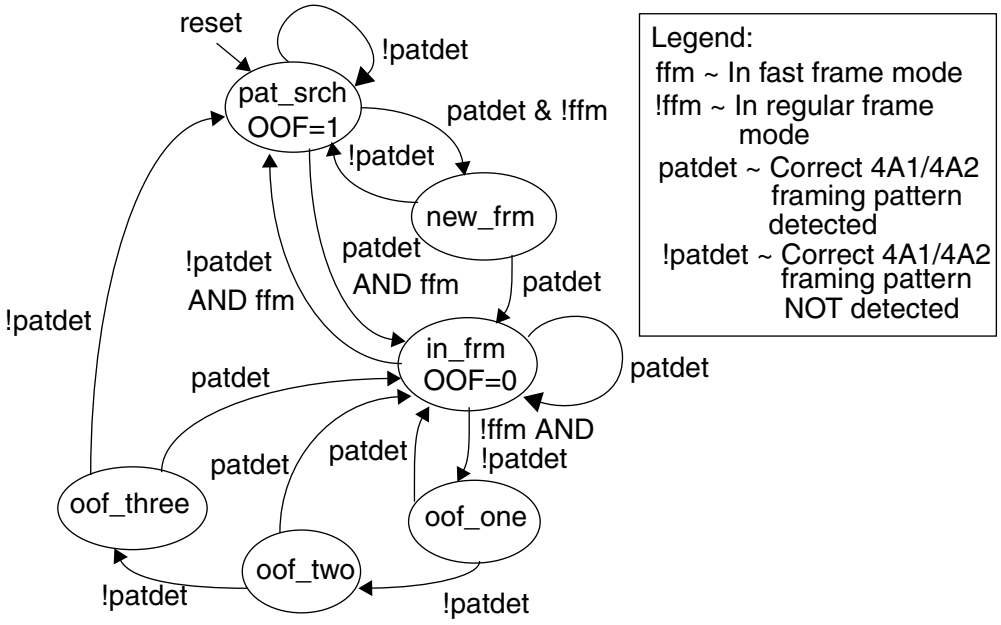
The framer FSM is responsible for detecting the in-frame and Out-Of-Frame status of the incoming data and sends out alarms (interrupts) on Out-Of-Frame (OOF). The framer is a pseudo-SONET framer in the sense that it does not support LOF or SEF detect-alarm signal as specified in the GR-253 standard.

The framer has a fast frame mode where a single good framing pattern can cause the framer state machine to go the “in_frm” state and a single bad frame can cause the state machine to declare “OOF” (See Fig. 19). The fast frame mode can be set by the software register bit, FFRM_EN_xx.

The FSM is a four byte framer and searches for the framing pattern based on the 32-bit words. Accordingly, the framing pattern is four A1 bytes (F6,F6,F6,F6) followed by four A2 bytes (28,28,28,28).

The framer FSM comes out of reset in the “OOF” state with the OOF alarm set. The framer goes in frame if it finds 2 consecutive frames with the desired framing bytes and goes out of frame if it finds 4 consecutive frames with at least one framing bit error in each frame. Frame timing is also synchronized based on the STS-48 row and column counters. This corresponds to SONET specification that it will take two consecutive valid framing patterns to frame to an incoming signal. Outside the “OOF” state, the OOF alarm output is low.

Figure 19. Transmit Clocking Diagram in SONET Mode



Section (B1) BIP-8 Calculator
The section BIP-8 B1 byte in a given STS-N frame contains the scrambled BIP value for all scrambled bytes of the previous frame. Except for the A1,A2 and J0 section overhead bytes, all bytes in a frame are scrambled. The Section (B1) BIP-8 is calculated as the even parity of all bits in the current STS-48 frame. This value is compared to the Section Overhead B1 byte of the next frame. B1 error counters are available that monitors the number of B1 errors on a per-channel basis. A B1 parity error flag is also generated as a software alarm bit.

Descrambler
The data from the framer is descrambled using the SONET/SDH standard generator polynomial $1 + x^6 + x^7$. The descrambling is performed in parallel on each 32-bit word per channel, synchronized to the frame pulse and can be disabled through the software register bit.

RDI (Remote Defect Indicator) Monitor
The line RDI (RDI-L) is monitored through bits 2-0 of the K2 byte. Within the 32-bit descrambled data, a pattern of "110" on bits 26-24 will indicate a RDI-L status. RDI-L must be detected in two consecutive frames before an RDI alarm register bit is set. If fast_frame_mode is enabled, then the RDI alarm register bit will be set if RDI-L is detected in one frame.

Receive FIFO
Clock domain transfers and multi-link de-skew are one of the most critical parts of this device. The main clock domain transfer for the datapath is handled by the receive FIFO. For each link, there are two FIFOs. A 24 x 33 FIFO is used in SONET mode.

The use of the FIFO is controlled by configuration bits.

- Data can be sent from the descrambler directly to the FPGA bypassing the alignment FIFO. Data from each channel will have an associated clock (RWCKxx at 77.76 MHz). Each channel will also provide a FP and SPE indicator along with the data. Descrambling can be inhibited through the DSCR_INH_xx control bit.
- Data can be sent directly from the 8:32 DEMUX block to the FPGA bypassing the alignment FIFO and SONET framer and descrambler. Data from each channel will have an associated clock. No SPE or FP indicator is provided with the data.

Receive FIFO in SONET mode
The receive FIFO used in SONET mode will allow for an inter-link skew of about 300 ns (24 x 32 = 768 bits, 400 ps per bit gives 307 ns). The FIFO is written at 77.76 MHz and read at 77.76 MHz. Once frame synchronization has occurred, the write control logic will cause data to be written to the memory. The write control block is required to insure that the word containing the first A1 byte is written to the same location (address 0) in the FIFO. The synchronization algorithm issues a sync pulse and sync error signals to the read control block based on the alignment option chosen. This sync pulse will coordinate the reading of the FIFOs.

The read control logic synchronizes the reading of the FIFO for the streams that are to be aligned. The block begins reading when the FIFO sync sub block signals that all of the applicable A1s with the appropriate margin have been written to the FIFO. All of the read blocks to be synchronized begin reading at the same time and same location in the memory (address 0). The block also takes the difference between the write and read address to indicate the relative skews between the links. If this difference exceeds a certain limit (programmable), then an alarm (alignment overflow) is provided to the register interface.

Multi-channel Alignment in SONET Mode – ORSO42G5
The alignment FIFO allows the transfer of all data to a common clock. The FIFO sync block allows the system to be configured to allow the frame alignment of multiple slightly varying data streams. This optional alignment ensures that matching SERDES streams will arrive at the FPGA end in perfect data sync. It is important to note that for all aligned channels in a group, the SERDES transmitters on the other side of the high-speed link must all be transmitting data at exactly the same frequency (0 ppm difference), i.e., using a common clock source.

The ORSO42G5 has a total of four channels (two per SERDES block). The incoming data of these channels can be synchronized in several ways, or they can be independent of one other. Two channels within a SERDES can be

SPE Generator

The SPE generator in the ORSO42G5 and ORSO82G5 is used to indicate the payload and overhead portions of a SONET frame. It is present in the SONET data path only. The SPE generator generates row, column and STS counters based on the frame pulse received from the (24 x 33) alignment FIFO or from the descrambler if alignment FIFOs are bypassed. It also retimes the 32-bit data in order to align it with the SPE indicator. The SPE generator will also detect negative or positive pointer justification (if justification is enabled) by looking at the ID bits in the H1 and H2 bytes and adjust the SPE indicator for the STS-1 frame being justified as follows:

- During positive pointer justification, the SPE will be low during H3 byte and the SPE byte following it.
- During negative pointer justification, the SPE will be high during H3 byte.
- During no justification, the SPE will be low during H3 byte.

This block only detects the incoming pointer bytes for SPE generation. This capability can be enabled by software control. By default, the SPE generator will ignore any pointer justification. This block has no capability of any pointer processing, pointer checking or pointer mover operation and ignores “new data” indications from the SONET specification.

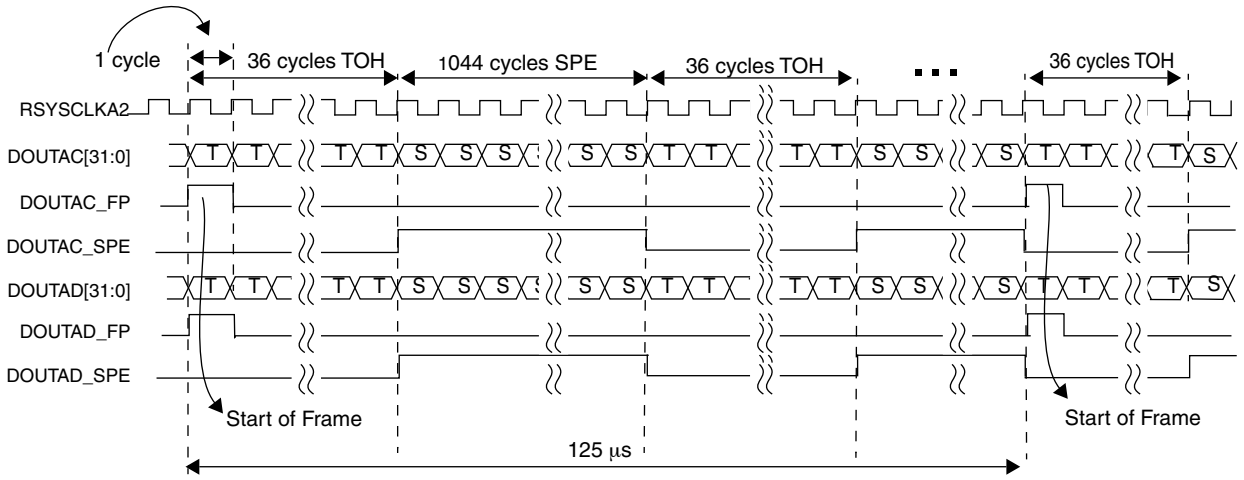
SONET Mode Receive Timing – ORSO42G5

This section contains timing diagrams for major interfaces of this block to the FPGA logic when SONET frames are to be transferred.

- When operating in SONET mode, the entire SONET frame is sent to the FPGA. In multi-channel alignment mode(s), data from all channels within an alignment group are aligned to the A1A2 framing bytes.
- Each SONET frame is 125μs. The frame starts with 36 clock cycles (77.76 MHz) of TOH followed by 1044 clock cycles of SPE, followed by 36 clock cycles of TOH, 1044 cycles of SPE.
- The DOUTxx_SPE signal indicates TOH or SPE in the data (low for TOH, high for SPE)
- Twin pairs are AC, AD (group A2) and BC, BD (group B2)

Figure 32 shows the SONET twin alignment mode timing for the ORSO42G5. The frame pulse and SPE indicators are show for each of the two channels (AC, AD) in twin alignment.

Figure 30. Receive Clocking Diagram for SONET Mode Twin Alignment in Block A – ORSO42G5

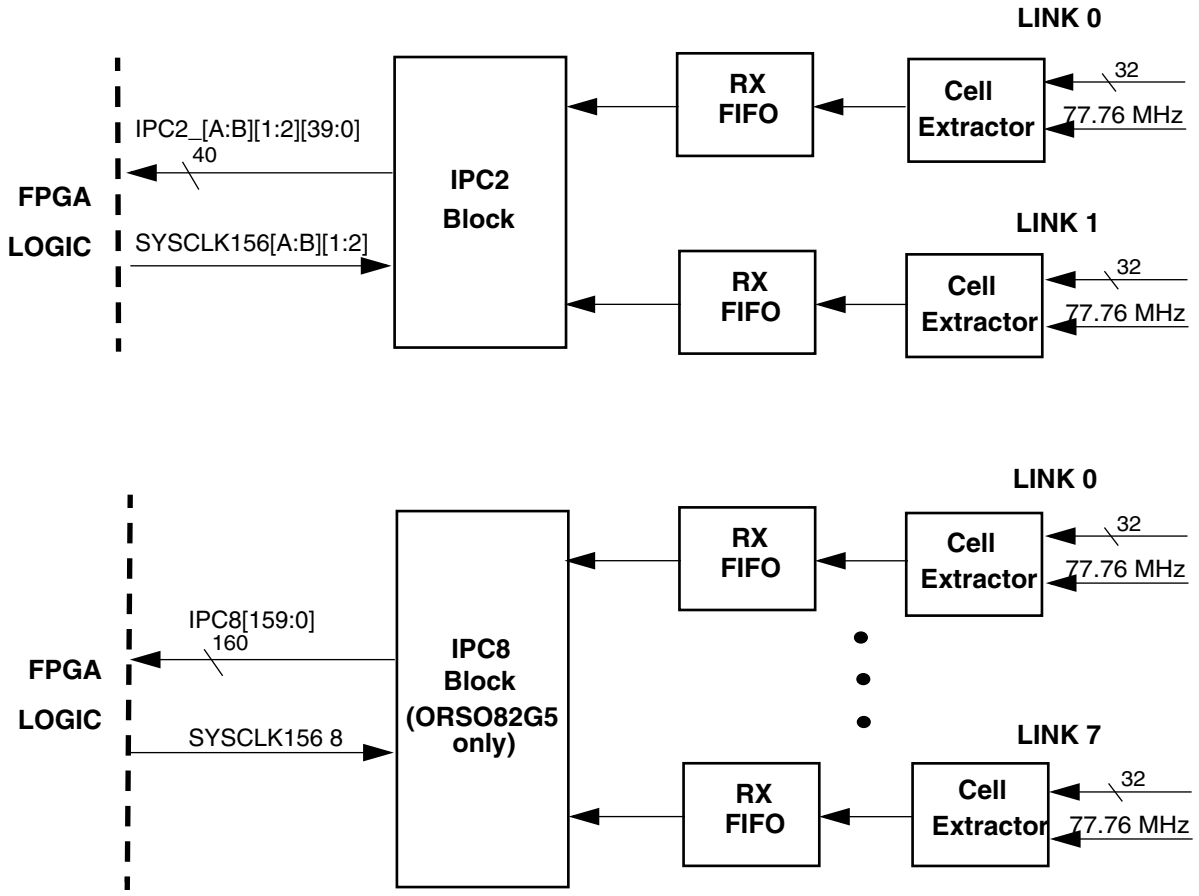


Clocks
RSYSCLKA2 is the read clock used for group A2
RSYSBLKB2 is the read clock used for group B2

Data
T Represents TOH
S Represents SPE
DOUTxx-SPE is high for SPE, low for TOH

- Insuring group bundles are properly aligned.
- Scheduling reads from the RX FIFOs. Cells are read one at a time from the configured links.
- Parsing the cell data into payload data (along with selected header information). Cells which have errors that make them unusable (such as BIP or sequence number errors) are thrown away. This dropping of errored cells can be disabled through register bits CELL_BIP_INH_xx and CELL_SEQ_INX_xx.

Figure 44. IPC2 and IPC8 Block Diagrams



There are 5 IPC blocks in the embedded core. There is an IPC2 block for every channel pair:

- IPC2_A1 combines links from channels AA,AB (ORSO82G5 only)
- IPC2_A2 combines links from channels AC,AD
- IPC2_B1 combines links from channels BA,BB (ORSO82G5 only)
- IPC2_B2 combines links from channels BC,BD

The IPC8 block combines cells from all eight aligned links and transmits them to the FPGA logic (ORSO82G5 only).

Before an IPC can begin reading data from the Rx FIFOs and assembling cells, it must first align all FIFOs in a port bundle. This is accomplished by handshaking signals between the framer and the IPC. The framer indicates to the IPC that framing has been acquired. The framer does not start filling the FIFOs, however, until the next A1/A2 SONET signal.

Table 24. SERDES Per Channel Configuration Registers (Read/Write) – ORSO42G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
SERDES Per Channel Transmit and Receive Channel Configuration Registers (Read/Write) xx = [AC, AD, BC, BD]					
30024 - AC 30034 - AD 30124 - BC 30134 - BD	[0]	RSVD	40	Reserved	—
	[1]	MASK_xx		Transmit and Receive Alarm Mask Bit, Channel xx. When MASK_xx = 1, the transmit and receive alarms of a channel are prevented from generating an alarm (i.e., they are masked or disabled). The MASK_xx bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK_xx = 1 on device reset.	Both
	[2]	SWRST_xx		Transmit and Receive Software Reset Bit, Channel xx. When SWRST_xx = 1, this bit provides the same function as the hardware reset, except that all configuration register settings are unaltered. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. SWRST = 0 on device reset.	Both
	[3:6]	RSVD		Reserved	—
	[7]	TESTEN_xx		Transmit and receive Test Enable Bit, Channel xx. When TESTEN_xx = 1, the transmit and receive sections of channel xx are place in test mode. The TESTMODE_xx bits (30006, 30106, etc.) must be set to specify the desired test. The GTESTEN_[A:B] bits override the individual TESTEN_xx settings.	Both
30026-AC 30036-AD 30126-BC 30136-BD	[0]	TESTMODE_xx	00	SERDES Test Mode Select, channel xx. TESTMODE_xx = 0 selects Near End Loopback (CML TX to CML RX internally) TESTMODE_xx = 1 selects Far End Loopback (CML RX to CML TX internally)	Factory Test
	[1:7]	RSVD		Reserved, Set to zero (default).	—

Table 26. Per-Channel Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30824 - AC 30834 - AD 30924 - BC 30934 - BD	[0]	LCKREFN_xx	00	0 = Lock receiver to reference clock (REFCLK) 1 = Lock receiver to HDINxx data	Both
	[1]	LOOPENB_xx		LOOPENB_xx =1 Enable high-speed internal loopback from TX to RX. Disable the HDOUT buffers.	Both
	[2]	DISABLE_TX_xx		Disable Transmitter, For DISABLE_TX = 1 the TX Link is disabled. The disabled link is ignored by the Output Port Controller (OPC) and internally generated idle cells are transmitted on the link.fIf the link is disabled during the transmission of a cell on the link, the entire cell is transmitted before the link is declared invalid.	Cell
	[3]	DISABLE_RX_xx		Disable Receiver, DISABLE_RX = 1 disables the RX link for cell processing by the Input Port Controller (IPC). The IPC will not read cells from a link if this bit is set for that link	Cell
	[4]	CELL_BIP_INH_xx		Cell BIP (Check) Inhibit, CELL_BIP_INH = 1 prevents cells from being dropped due to a Cell BIP error, in the RX path. If this bit is not set, then cells will be dropped automatically if a cell bip error is detected by the core. The CELLDROP signal across the core-FPGA interface will be active only if this bit is NOT set.	Cell
	[5]	CELL_SEQ_INH_xx		Cell Sequence (Checking) Inhibit, CELL_SEQ_INH = 1 prevents cells in the RX path from being dropped due to a sequence error. If this bit is not set, then cells will be dropped automatically if a sequence error is detected internally. The CELLDROP signal across the core-FPGA interface will be active only if this bit is NOT set.	Cell
	[6]	AUTO_TOH_xx		Automatic TOH Generation, AUTO_TOH_xx =1 enables the TX core to automatically generate TOH bytes. All the FORCE_* register bits are valid if this bit is set. This bit should be set to 1 in Cell Mode. It can be set to 1or 0 in SONET Mode. If this bit is not set, then user has to provide all the TOH bytes or use the AUTO_SOH mode.	SONET
	[7]	FMPU_RESYNC1_xx		Single channel alignment FIFO reset. Rising edge sensitive. Write a 0 and then a 1 to enable this bit. When enabled, the read pointer in the alignment FIFO is reset to the middle of the FIFO. This bit is valid only when FMPU_SYNMODE_xx = 00 (no multi channel alignment)	SONET
30825 - AC 30835 - AD 30925 - BC 30935 - BD	[0:7]	LINK_NUM_TX_xx	00	Transmit Link Number, This value is transmitted in the “F1” byte of the TOH. This value is used to verify that the links are connected properly and is only used in the AUTO_TOH mode.	Both

Table 28. Common Control Register Descriptions – ORSO42G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A09	[0:7]	B1_ERR_CNT	00	Error counter that increments when a section B1 error is detected on a link. The link is selected using ERRCNT_CHSEL. This counter is cleared on read.	Both
30A0A	[0:7]	CELL_BIP_ERR_CNT	00	Cell BIP Error Counter, Error counter that increments when a Cell BIP error is detected on a link. The link being monitored is selected using ERRCNT_CHSEL. This counter is cleared on read.	Cell
30A0B	[0:2]	RSVD	00	Reserved	
	[3]	CELL_DRP_B2		Cell Drop, CELL_DRP_B2 = 1 indicates that a cell has been dropped from the link group BC and BD	Cell
	[4]	RSVD		Reserved	—
	[5]	CELL_DRP_A2		Cell Drop, CELL_DRP_A2 = 1 indicates that a cell has been dropped from the link group AC and AD	Cell
	[6:7]	RSVD		Reserved	—
30A0C	[0:1]	RSVD	00	Reserved	
	[2]	SYNC2_B2_OOS		SYNC2_B2_OOS = 1 indicates that channels cannot be aligned within the links BC and BD in SONET mode	SONET
	[3:4]	RSVD		Reserved	—
	[5]	SYNC2_A2_OOS		SYNC2_A2_OOS = 1 indicates that channels cannot be aligned within the AC and AD links in SONET mode	SONET
	[6:7]	SYNC2_A1_OOS		Reserved	—
30A0D	[0:1]	RSVD	00	Reserved	—
	[2]	SYNC2_B2_OVFL		SYNC2_B2_OVFL = 1 indicates that the alignment FIFO(s) in the links BC and BD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[3:4]	RSVD		Reserved	—
	[5]	SYNC2_A2_OVFL		SYNC2_A2_OVFL = 1 indicates that the alignment FIFO(s) in the links AC and AD are near overflow (i.e., at the time of writing into address 0, the read address was less than RX_FIFO_MIN)	SONET
	[6:7]	RSVD		Reserved	—
30A0E	[0:2]	RSVD	00	Reserved	
	[3]	BDL_ALIGN_ERR_B2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs BC and BD	Cell
	[4]	RSVD		Reserved	—
	[5]	BDL_ALIGN_ERR_A2		Alignment Error, BDL_ALIGN_ERR = 1 indicates that an alignment error has occurred in the link group pairs AC and AD	Cell
	[6:7]	RSVD		Reserved	—

Table 34. Per-Channel Control Register Descriptions – ORSO82G5

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30800 - AA 30810 - AB 30820 - AC 30830 - AD 30900 - BA 30910 - BB 30920 - BC 30930 - BD	[0:4]	RSVD	00	Reserved	—
	[5]	CELL_ALIGN_ERR_EN_xx		'1' = Alarm enabled for CELL_ALIGN_ERR_xx	Cell
	[6]	TX_URUN_ERR_EN_xx		'1' = Alarm enabled for TX_URUN_ERR_xx	Cell
	[7]	TX_ORUN_ERR_EN_xx		'1' = Alarm enabled for TX_ORUN_ERR_xx	Cell
30801 - AA 30811 - AB 30821 - AC 30831 - AD 30901 - BA 30911 - BB 30921 - BC 30931 - BD	[0]	RSVD	00	Reserved	—
	[1]	OOF_EN_xx		'1' = Alarm enabled for OOF_xx	Both
	[2]	EX_SEQ_ERR_EN_xx		'1' = Alarm enabled for EX_SEQ_ERR _xx	Cell
	[3]	SEQ_ERR_EN_xx		'1' = Alarm enabled for SEQ_ERR _xx	Cell
	[4]	CELL_BIP_ERR_EN_xx		'1' = Alarm enabled for CELL_BIP_ERR_xx	Cell
	[5]	B1_ERR_EN_xx		'1' = Alarm enabled for B1_ERR_xx	Both
	[6]	RX_FIFO_OVRUN_EN_xx		'1' = Alarm enabled for RX_FIFO_OVRUN_xx	Cell
	[7]	RDI_EN_xx		'1' = Alarm enabled for RDI_xx	Both
30802 - AA 30812 - AB 30822 - AC 30832 - AD 30902 - BA 30912 - BB 30922 - BC 30932 - BD	[0]	ENABLE_JUST_xx	00	ENABLE_JUST_xx =1 causes the core to interpret pointer bytes for positive or negative justification	SONET
	[1]	FMPU_STR_EN_xx		FMPU_STR_EN_xx = 1 enables a channel for alignment within a multi-channel alignment group	SONET
	[2:3]	FMPU_SYNMODE_xx		"00" - No channel alignment "01" - Twin channel alignment "10" - 4 channel alignment "11 - By-8 alignment	SONET
	[4]	DSCR_INH_xx		Descrambling Inhibit, DSCR_INH = 1 inhibits descrambling (in the Rx direction) and scrambling (in the Tx direction). When inhibiting the scrambler and descrambler the AUTO_B1_xx calculated and checked B1 value will always be incorrect.	Both
	[5]	FFRM_EN_xx		Fast Frame Enable, FFRM_EN=1 enables the fast frame mode.	Both
	[6]	AIS_ON_xx		Alarm Indication Signal (control), AIS_ON =1 forces AIS-L insertion.	Both
	[7]	AIS_ON_OOF_xx		Alarm Indication Signal on Out of Frame, AIS_ON_OOF =1 forces AIS-L insertion during OOF =1.	Both

Table 35. Per-Channel Status Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
3080B - AA 3081B - AB 3082B -AC 3083B - AD 3090B - BA 3091B - BB 3092B - BC 3093B - BD	[0]	RSVD	00	Reserved	—
	[1]	STAT_OOF_xx		STAT_OOF_xx = 1 same as OOF_xx except that a 1 on this bit can NOT cause an interrupt	Both
	[2]	STAT_EX_SEQ_ERR_xx		STAT_EX_SEQ_ERR_xx = 1 same as EX_SEQ_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[3]	STAT_SEQ_ERR_xx		STAT_SEQ_ERR_xx = 1 same as SEQ_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[4]	STAT_CELL_BIP_ERR_xx		STAT_CELL_BIP_ERR_xx = 1 same as CELL_BIP_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[5]	STAT_B1_ERR_xx		STAT_B1_ERR_xx = 1 same as B1_ERR_xx except that a 1 on this bit can NOT cause an interrupt	Both
	[6]	STAT_RX_FIFO_OVRUN_xx		STAT_RX_FIFO_OVRUN_xx = 1 same as RX_FIFO_OVRUN_xx except that a 1 on this bit can NOT cause an interrupt	Cell
	[7]	STAT_RDI_xx		STAT_RDI_xx = 1 same as RDI_xx except that a 1 on this bit can NOT cause an interrupt	Both
3080C - AA 3081C - AB 3082C - AC 3083C - AD 3090C - BA 3091C - BB 3092C - BC 3093C - BD	[0:7]	LINK_NUM_RX_xx	00	Link number received that is stored in the F1 byte position of the SONET TOH	Both
3080E - AA 3081E - AB 3082E - AC 3083E AD 3090E - BA 3091E - BB 3092E- BC 3093E - BD	[0:5]	RSVD	00	Reserved	—
	[6]	CH248_SYNC_xx		CH248_SYNC_xx = 1 indicates that A1A2 bytes have been detected by link xx for multi-channel alignment	SONET
	[7]	RX_LINK_GOOD_xx		RX_LINK_GOOD_xx = 1 indicates that frame has been acquired and the link has been stable. Goes high at an A1A2 boundary but can go low at any point in a frame due to excessive errors	Cell

Table 36. Common Control Register Descriptions – ORSO82G5 (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description	Mode
30A08	[0]	ALARM_STATUS_BD	00	Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BD. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[1]	ALARM_STATUS_BC		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BC. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[2]	ALARM_STATUS_BB		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BB. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[3]	ALARM_STATUS_BA		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel BA. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[4]	ALARM_STATUS_AD		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AD. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[5]	ALARM_STATUS_AC		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AC. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
	[6]	ALARM_STATUS_AB		OR of all alarm status bits for channel AB. A 1 on this bit will set the alarm pin on the system bus interrupt cause register (on the FPGA side)	Both
	[7]	ALARM_STATUS_AA		Alarm Status Indicator, This bit is an OR of all alarm status bits for the channel AA. A 1 on this bit will also set the alarm pin on the system bus interrupt cause register (on the FPGA side).	Both
30A09	[0:7]	B1_ERR_CNT	00	Error counter that increments when a section B1 error is detected on a link. The link is selected using ERRCNT_CHSEL. This counter is cleared on read.	Both
30A0A	[0:7]	CELL_BIP_ERR_CNT	00	Cell BIP Error Counter, Error counter that increments when a Cell BIP error is detected on a link. The link being monitored is selected using ERRCNT_CHSEL. This counter is cleared on read.	Cell

High Speed Data Transmitter

Table 40 specifies serial data output buffer parameters measured on devices with typical and worst case process parameters and over the full range of operation conditions.

Table 40. Serial Output Timing and Levels (CML I/O)

Parameter	Min.	Typ.	Max.	Units
Rise Time (20% - 80%)	50	80	110	ps
Fall Time (80% - 20%)	50	80	110	ps
Common Mode	V_{DDOB} – 0.30	V_{DDOB} – 0.25	V_{DDOB} – 0.15	V
Differential Swing (Full Amplitude)[1]	750	900	1000	mV_{p-p}
Differential Swing (Half Amplitude)[1]	375	450	500	mV_{p-p}
Output Load (External)	—	86	—	Ω

1. Differential swings measured at the end of 3 inches of FR-4 and 12 inches of coax cable.

Transmitter output jitter is a critical parameter to systems with high speed data links. Table 41 and Table 42 specify the transmitter output jitter for typical and worst case devices over the full range of operating conditions.

Table 41. Channel Output Jitter (2.7 Gbps)

Parameter	Device	Min.	Typ.[1]	Max.[1]	Units
Deterministic	ORSO42G5	—	0.12	0.16	Ulp-p
	ORSO82G5	—	0.12	0.16	Ulp-p
Random[2]	ORSO42G5	—	0.05	0.18	Ulp-p
	ORSO82G5	—	0.05	0.08	Ulp-p
Total[3]	ORSO42G5	—	0.17	0.34	Ulp-p
	ORSO82G5	—	0.17	0.24	Ulp-p

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Wavecrest SIA-3000 instrument used to measure one-sigma (RMS) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10^{-12}.
3. Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10^{-12}. See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

Table 42. Channel Output Jitter (2.5 Gbps)

Parameter	Device	Min.	Typ.[1]	Max.[1]	Units
Deterministic	ORSO42G5	—	0.11	0.13	Ulp-p
	ORSO82G5	—	0.11	0.13	Ulp-p
Random[2]	ORSO42G5	—	0.05	0.14	Ulp-p
	ORSO82G5	—	0.05	0.07	Ulp-p
Total[3]	ORSO42G5	—	0.16	0.27	Ulp-p
	ORSO82G5	—	0.16	0.20	Ulp-p

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Wavecrest SIA-3000 instrument used to measure one-sigma (RMS) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10^{-12}.
3. Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10^{-12}. See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

Input Eye-Mask Characterization

Figure 51 provides an eye-mask characterization of the SERDES receiver input. The eye-mask is specified below for two different eye-mask heights. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance. Almost all detrimental characteristics of transmit signal and the interconnection link design result in eye-closure. This, combined with the eye-opening limitations of the line receiver, can provide a good indication of a link's ability to transfer data error-free.

The Clock and Data Recovery (CDR) portion of the ORSO42G5 and ORSO82G5 SERDES receiver has the ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth (about 3 MHz). The eye-mask specifications of Table 45 are for jitter frequencies above the PLL bandwidth of the CDR, which is a worst case condition. When jitter occurs at frequencies below the PLL bandwidth, the receiver jitter tolerance is significantly better. For this case error-free data detection can occur even with a completely closed eye-mask.

Figure 51. Receive Data Eye-Diagram Template (Differential)

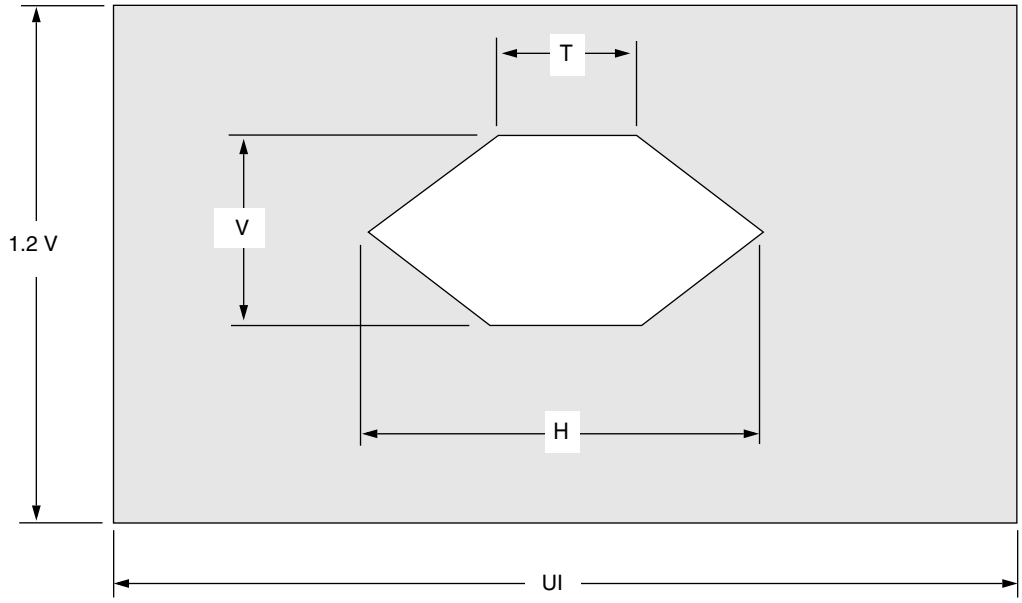


Table 45. Receiver Eye-Mask Specifications[1]

Parameter	Conditions	Value	Unit
Input Data			
Eye Opening Width (H)@ 2.7Gbps	V=175 mV diff[1]	0.55	UIP-P
Eye Opening Width (T)@ 2.7Gbps	V=175 mV diff[1]	0.15	UIP-P
Eye Opening Width (H)@ 2.7Gbps	V=600 mV diff[1]	0.35	UIP-P
Eye Opening Width (T)@ 2.7Gbps	V=600 mV diff[1]	0.10	UIP-P
Eye Opening Width (H)@ 2.5Gbps	V=175 mV diff[1]	0.42	UIP-P
Eye Opening Width (T)@ 2.5Gbps	V=175 mV diff[1]	0.15	UIP-P
Eye Opening Width (H)@ 2.5Gbps	V=600 mV diff[1]	0.33	UIP-P
Eye Opening Width (T)@ 2.5Gbps	V=600 mV diff[1]	0.10	UIP-P

1. With PRBS 2^7-1 data pattern, 10 MHz sinusoidal jitter, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply.

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
Y15	5 (BC)	7	IO	PB31C	VREF_5_07	L50T
W15	5 (BC)	7	IO	PB31D	-	L50C
V13	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB18	5 (BC)	8	IO	PB33C	-	L51T
AA18	5 (BC)	8	IO	PB33D	VREF_5_08	L51C
J11	-	-	VSS	VSS	-	-
V14	5 (BC)	8	IO	PB34D	-	-
V16	5 (BC)	9	IO	PB35B	-	-
Y16	5 (BC)	9	IO	PB36C	-	L52T
W16	5 (BC)	9	IO	PB36D	-	L52C
V15	-	-	VDD33	VDD33	-	-
J12	-	-	VSS	VSS	-	-
H15	-	-	VDD15	VDD15	-	-
J13	-	-	VSS	VSS	-	-
J6	-	-	VDD15	VDD15	-	-
J14	-	-	VSS	VSS	-	-
Y17	-	-	VDD33	VDD33	-	-
K8	-	-	VSS	VSS	-	-
J15	-	-	VDD15	VDD15	-	-
K7	-	-	VDD15	VDD15	-	-
Y18	-	-	VDD33	VDD33	-	-
K9	-	-	VSS	VSS	-	-
W21	-	-	VSS	VSS	-	-
W22	-	-	VDDGB_B	VDDGB_B	-	-
F18	-	-	VDD_ANA	VDD_ANA	-	-
V21	-	-	O	REXT_B	-	-
V22	-	-	O	REXTN_B	-	-
U21	-	-	I	REFCLKN_B	-	HSN_1
U22	-	-	I	REFCLKP_B	-	HSP_1
E20	-	-	VSS	VSS	-	-
G17	-	-	VDD_ANA	VDD_ANA	-	-
G18	-	-	VDD_ANA	VDD_ANA	-	-
J16	-	-	VDD_ANA	VDD_ANA	-	-
J17	-	-	VDD_ANA	VDD_ANA	-	-
T20	-	-	VDDIB	VDDIB_BC	-	-
J18	-	-	VDD_ANA	VDD_ANA	-	-
T21	-	-	I	HDINN_BC	-	HSN_2
F19	-	-	VSS	VSS	-	-
T22	-	-	I	HDINP_BC	-	HSP_2
J19	-	-	VDD_ANA	VDD_ANA	-	-
F20	-	-	VSS	VSS	-	-
K16	-	-	VDD_ANA	VDD_ANA	-	-
R20	-	-	VDDOB	VDDOB_BC	-	-
R21	-	-	O	HDOUTN_BC	-	HSN_3

Table 51. ORSO42G5 484-pin PBGAM Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
P15	-	-	VDD15	VDD15	-	-
R6	-	-	VDD15	VDD15	-	-
R15	-	-	VDD15	VDD15	-	-
T4	-	-	VDD15	VDD15	-	-
W19	-	-	VDD15	VDD15	-	-
Y3	-	-	VDD15	VDD15	-	-
Y19	-	-	VDD15	VDD15	-	-
Y20	-	-	VDD15	VDD15	-	-
T15	-	-	VDD15	VDD15	-	-
T16	-	-	VDD15	VDD15	-	-
U4	-	-	VDD15	VDD15	-	-
T12	-	-	VDD15	VDD15	-	-
T13	-	-	VDD15	VDD15	-	-
T14	-	-	VDD15	VDD15	-	-
T6	-	-	VDD15	VDD15	-	-
T7	-	-	VDD15	VDD15	-	-
T10	-	-	VDD15	VDD15	-	-
T11	-	-	VDD15	VDD15	-	-
G5	0 (TL)	-	VDDIO0	VDDIO0	-	-
H5	0 (TL)	-	VDDIO0	VDDIO0	-	-
J5	0 (TL)	-	VDDIO0	VDDIO0	-	-
V17	5 (BC)	-	VDDIO5	VDDIO5	-	-
W17	5 (BC)	-	VDDIO5	VDDIO5	-	-
W18	5 (BC)	-	VDDIO5	VDDIO5	-	-
M6	7 (CL)	-	VDDIO7	VDDIO7	-	-
N6	7 (CL)	-	VDDIO7	VDDIO7	-	-
U5	-	-	VDD15	VDD15	-	-
U17	-	-	VDD15	VDD15	-	-
V5	-	-	VDD15	VDD15	-	-
V18	-	-	VDD15	VDD15	-	-
R18	-	-	VSS	VSS	-	-
R19	-	-	VSS	VSS	-	-
T19	-	-	VSS	VSS	-	-
U19	-	-	VSS	VSS	-	-
U20	-	-	VSS	VSS	-	-
V19	-	-	VSS	VSS	-	-
V20	-	-	VSS	VSS	-	-
W20	-	-	VSS	VSS	-	-
Y21	-	-	VSS	VSS	-	-
Y22	-	-	VSS	VSS	-	-
L13	-	-	VSS	VSS	-	-
L14	-	-	VSS	VSS	-	-
M8	-	-	VSS	VSS	-	-
M9	-	-	VSS	VSS	-	-

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
B29	1 (TC)	8	IO	PT33D	—	L1C_A0
C29	1 (TC)	8	IO	PT33C	VREF_1_08	L1T_A0
B15	1 (TC)	—	VDDIO1	VDDIO1	—	—
E27	1 (TC)	8	IO	PT32D	—	L2C_A0
E26	1 (TC)	8	IO	PT32C	—	L2T_A0
AP34	—	—	Vss	Vss	—	—
A30	1 (TC)	8	IO	PT32B	—	—
A29	1 (TC)	9	IO	PT31D	—	L3C_D3
E25	1 (TC)	9	IO	PT31C	VREF_1_09	L3T_D3
B17	1 (TC)	—	VDDIO1	VDDIO1	—	—
E24	1 (TC)	9	IO	PT31A	—	—
B28	1 (TC)	9	IO	PT30D	—	L4C_A0
C28	1 (TC)	9	IO	PT30C	—	L4T_A0
B2	—	—	Vss	Vss	—	—
D28	1 (TC)	9	IO	PT30A	—	—
C27	1 (TC)	9	IO	PT29D	—	L5C_A0
D27	1 (TC)	9	IO	PT29C	—	L5T_A0
E23	1 (TC)	9	IO	PT29B	—	L6C_A0
E22	1 (TC)	9	IO	PT29A	—	L6T_A0
D26	1 (TC)	1	IO	PT28D	—	L7C_A0
D25	1 (TC)	1	IO	PT28C	—	L7T_A0
B33	—	—	Vss	Vss	—	—
D24	1 (TC)	1	IO	PT28B	—	L8C_A0
D23	1 (TC)	1	IO	PT28A	—	L8T_A0
C26	1 (TC)	1	IO	PT27D	VREF_1_01	L9C_A0
C25	1 (TC)	1	IO	PT27C	—	L9T_A0
D11	1 (TC)	—	VDDIO1	VDDIO1	—	—
E21	1 (TC)	1	IO	PT27B	—	L10C_A0
E20	1 (TC)	1	IO	PT27A	—	L10T_A0
D22	1 (TC)	2	IO	PT26D	—	L11C_A0
D21	1 (TC)	2	IO	PT26C	VREF_1_02	L11T_A0
E34	—	—	Vss	Vss	—	—
A28	1 (TC)	2	IO	PT26B	—	—
B26	1 (TC)	2	IO	PT25D	—	L12C_A0
B25	1 (TC)	2	IO	PT25C	—	L12T_A0
D13	1 (TC)	—	VDDIO1	VDDIO1	—	—
B27	1 (TC)	2	IO	PT25B	—	—
A27	1 (TC)	3	IO	PT24D	—	L13C_A0
A26	1 (TC)	3	IO	PT24C	VREF_1_03	L13T_A0
N13	—	—	Vss	Vss	—	—
C24	1 (TC)	3	IO	PT24B	—	—
C22	1 (TC)	3	IO	PT23D	—	L14C_A0
C23	1 (TC)	3	IO	PT23C	—	L14T_A0
D15	1 (TC)	—	VDDIO1	VDDIO1	—	—

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
D7	0 (TL)	—	VDDIO0	VDDIO0	—	—
C14	0 (TL)	1	IO	PT13B	—	L2C_A0
B14	0 (TL)	1	IO	PT13A	VREF_0_01	L2T_A0
A14	0 (TL)	1	IO	PT12D	M0	L3C_A0
A13	0 (TL)	1	IO	PT12C	M1	L3T_A0
AA20	—	—	Vss	Vss	—	—
E12	0 (TL)	2	IO	PT12B	MPI_CLK	L4C_A0
E13	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L4T_A0
C13	0 (TL)	2	IO	PT11D	M2	L5C_A0
C12	0 (TL)	2	IO	PT11C	M3	L5T_A0
B12	0 (TL)	2	IO	PT11B	VREF_0_02	L6C_A0
A12	0 (TL)	2	IO	PT11A	MPI_TEA_N	L6T_A0
D12	0 (TL)	3	IO	PT10D	—	L7C_D0
C11	0 (TL)	3	IO	PT10C	—	L7T_D0
B11	0 (TL)	3	IO	PT10B	—	—
A11	0 (TL)	3	IO	PT9D	VREF_0_03	L8C_A0
A10	0 (TL)	3	IO	PT9C	—	L8T_A0
AA21	—	—	Vss	Vss	—	—
B10	0 (TL)	3	IO	PT9B	—	—
E11	0 (TL)	3	IO	PT8D	D0	L9C_D0
D10	0 (TL)	3	IO	PT8C	TMS	L9T_D0
C10	0 (TL)	3	IO	PT8B	—	—
A9	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L10C_A0
B9	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L10T_A0
AA22	—	—	Vss	Vss	—	—
E10	0 (TL)	4	IO	PT7B	—	—
A8	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L11C_A0
B8	0 (TL)	4	IO	PT6C	D3	L11T_A0
D9	0 (TL)	4	IO	PT6B	VREF_0_04	L12C_D0
C8	0 (TL)	4	IO	PT6A	—	L12T_D0
E9	0 (TL)	5	IO	PT5D	D1	L13C_D0
D8	0 (TL)	5	IO	PT5C	D2	L13T_D0
AB13	—	—	Vss	Vss	—	—
A7	0 (TL)	5	IO	PT5B	—	L14C_A0
A6	0 (TL)	5	IO	PT5A	VREF_0_05	L14T_A0
C7	0 (TL)	5	IO	PT4D	TDI	L15C_D0
B6	0 (TL)	5	IO	PT4C	TCK	L15T_D0
E8	0 (TL)	5	IO	PT4B	—	L16C_A0
E7	0 (TL)	5	IO	PT4A	—	L16T_A0
A5	0 (TL)	6	IO	PT3D	—	L17C_A0
B5	0 (TL)	6	IO	PT3C	VREF_0_06	L17T_A0
AB14	—	—	Vss	Vss	—	—
C6	0 (TL)	6	IO	PT3B	—	L18C_A0
D6	0 (TL)	6	IO	PT3A	—	L18T_A0

Table 52. ORSO82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L19C_A0
B4	0 (TL)	6	IO	PT2C	PLL_CK1T/PPLL	L19T_A0
A4	0 (TL)	6	IO	PT2B	—	L20C_A0
A3	0 (TL)	6	IO	PT2A	—	L20T_A0
D5	—	—	O	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	—
E6	—	—	IO	PCCLK	CCLK	—
D4	—	—	IO	PDONE	DONE	—
E5	—	—	VDD33	VDD33	—	—
AB15	—	—	Vss	Vss	—	—
AL33	—	—	VDD15	VDD15	—	—
AL34	—	—	VDD15	VDD15	—	—
AM34	—	—	VDD15	VDD15	—	—
AN34	—	—	VDD15	VDD15	—	—
B34	—	—	VDD15	VDD15	—	—
C33	—	—	VDD15	VDD15	—	—
C34	—	—	VDD15	VDD15	—	—
D33	—	—	VDD15	VDD15	—	—
D34	—	—	VDD15	VDD15	—	—
E32	—	—	VDD15	VDD15	—	—
E33	—	—	VDD15	VDD15	—	—
F32	—	—	VDD15	VDD15	—	—
F34	—	—	VDD15	VDD15	—	—
N16	—	—	VDD15	VDD15	—	—
N17	—	—	VDD15	VDD15	—	—
N18	—	—	VDD15	VDD15	—	—
N19	—	—	VDD15	VDD15	—	—
P16	—	—	VDD15	VDD15	—	—
P17	—	—	VDD15	VDD15	—	—
P18	—	—	VDD15	VDD15	—	—
P19	—	—	VDD15	VDD15	—	—
R16	—	—	VDD15	VDD15	—	—
R17	—	—	VDD15	VDD15	—	—
R18	—	—	VDD15	VDD15	—	—
R19	—	—	VDD15	VDD15	—	—
T13	—	—	VDD15	VDD15	—	—
T14	—	—	VDD15	VDD15	—	—
T15	—	—	VDD15	VDD15	—	—
T20	—	—	VDD15	VDD15	—	—
T21	—	—	VDD15	VDD15	—	—
T22	—	—	VDD15	VDD15	—	—
U13	—	—	VDD15	VDD15	—	—
U14	—	—	VDD15	VDD15	—	—
U15	—	—	VDD15	VDD15	—	—
U20	—	—	VDD15	VDD15	—	—

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: ΘJA, ψJC, and ΘJC. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

ΘJA

This is the thermal resistance from junction to ambient (theta-JA):

$$\Theta_{JA} = \frac{T_J - T_A}{Q} \quad (1)$$

where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, ΘJA is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that ΘJA is expressed in units of °C/W.

ψJC

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance and it is defined by:

$$\psi_{JC} = \frac{T_J - T_C}{Q} \quad (2)$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the ΘJA measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψJC is also expressed in units of °C/W.

ΘJC

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\Theta_{JC} = \frac{T_J - T_C}{Q} \quad (3)$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates ΘJC from ψJC. ΘJC is a true thermal resistance and is expressed in units of °C/W.

ΘJB

This is the thermal resistance from junction to board. It is defined by:

$$\Theta_{JB} = \frac{T_J - T_B}{Q} \quad (4)$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads.