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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21j17a-mu

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- Up to four compare channels with optional complementary output
 - Generation of synchronized pulse width modulation (PWM) pattern across port pins
 - Deterministic fault protection, fast decay and configurable dead-time between complementary output
 - Dithering that increase resolution with up to 5 bit and reduce quantization error
- 32-bit Real Time Counter (RTC) with clock/calendar function
- Watchdog Timer (WDT)
- CRC-32 generator
- One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
 - Embedded host and device function
 - Eight endpoints
- Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
 - USART with full-duplex and single-wire half-duplex configuration
 - I2C up to 3.4MHz
 - SPI
 - LIN slave
- One two-channel Inter-IC Sound (I²S) interface
- One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 20 channels
 - Differential and single-ended input
 - 1/2x to 16x programmable gain stage
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
- 10-bit, 350ksps Digital-to-Analog Converter (DAC)
- Two Analog Comparators (AC) with window compare function
- Peripheral Touch Controller (PTC)
 - 256-Channel capacitive touch and proximity sensing
- I/O
 - Up to 52 programmable I/O pins
- Drop in compatible with SAM D20
- Packages
 - 64-pin TQFP, QFN, UFBGA
 - 48-pin TQFP, QFN, WLCSP
 - 32-pin TQFP, QFN, WLCSP
- Operating Voltage
 - 1.62V – 3.63V

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Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21E16A-AU	64K	8K	TQFP32	Tray
ATSAMD21E16A-AUT				Tape & Reel
ATSAMD21E16A-AF				Tray
ATSAMD21E16A-AFT				Tape & Reel
ATSAMD21E16A-MU			QFN32	Tray
ATSAMD21E16A-MUT				Tape & Reel
ATSAMD21E16A-MF				Tray
ATSAMD21E16A-MFT				Tape & Reel
ATSAMD21E17A-AU	128K	16K	TQFP32	Tray
ATSAMD21E17A-AUT				Tape & Reel
ATSAMD21E17A-AF				Tray
ATSAMD21E17A-AFT				Tape & Reel
ATSAMD21E17A-MU			QFN32	Tray
ATSAMD21E17A-MUT				Tape & Reel
ATSAMD21E17A-MF				Tray
ATSAMD21E17A-MFT				Tape & Reel
ATSAMD21E18A-AU	256K	32K	TQFP32	Tray
ATSAMD21E18A-AUT				Tape & Reel
ATSAMD21E18A-AF				Tray
ATSAMD21E18A-AFT				Tape & Reel
ATSAMD21E18A-MU			QFN32	Tray
ATSAMD21E18A-MUT				Tape & Reel
ATSAMD21E18A-MF				Tray
ATSAMD21E18A-MFT				Tape & Reel

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Table 3-2. Device Variant B

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21E15B-AU	32K	4K	TQFP32	Tray
ATSAMD21E15B-AUT				Tape & Reel
ATSAMD21E15B-AF				Tray
ATSAMD21E15B-AFT				Tape & Reel
ATSAMD21E15B-MU			QFN32	Tray
ATSAMD21E15B-MUT				Tape & Reel
ATSAMD21E15B-MF				Tray
ATSAMD21E15B-MFT				Tape & Reel
ATSAMD21E15B-UUT			WLCSP35 (GJR)	Tape & Reel
ATSAMD21E16B-AU	64K	8K	TQFP32	Tray
ATSAMD21E16B-AUT				Tape & Reel
ATSAMD21E16B-AF				Tray
ATSAMD21E16B-AFT				Tape & Reel
ATSAMD21E16B-MU			QFN32	Tray
ATSAMD21E16B-MUT				Tape & Reel
ATSAMD21E16B-MF				Tray
ATSAMD21E16B-MFT				Tape & Reel
ATSAMD21E16B-UUT	64K	8K	WLCSP35 (GJR)	Tape & Reel

Table 3-3. Device Variant C

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21E15C-UUT	32K	4K	WLCSP35 (GJS)	Tape & Reel
ATSAMD21E16C-UUT	64K	8K	WLCSP35 (GJS)	Tape & Reel

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Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21J18A-AU	256K	32K	TQFP64	Tray
ATSAMD21J18A-AUT				Tape & Reel
ATSAMD21J18A-AF				Tray
ATSAMD21J18A-AFT				Tape & Reel
ATSAMD21J18A-MU			QFN64	Tray
ATSAMD21J18A-MUT				Tape & Reel
ATSAMD21J18A-MF				Tray
ATSAMD21J18A-MFT				Tape & Reel
ATSAMD21J18A-CU			UFBGA64	Tray
ATSAMD21J18A-CUT				Tape & Reel

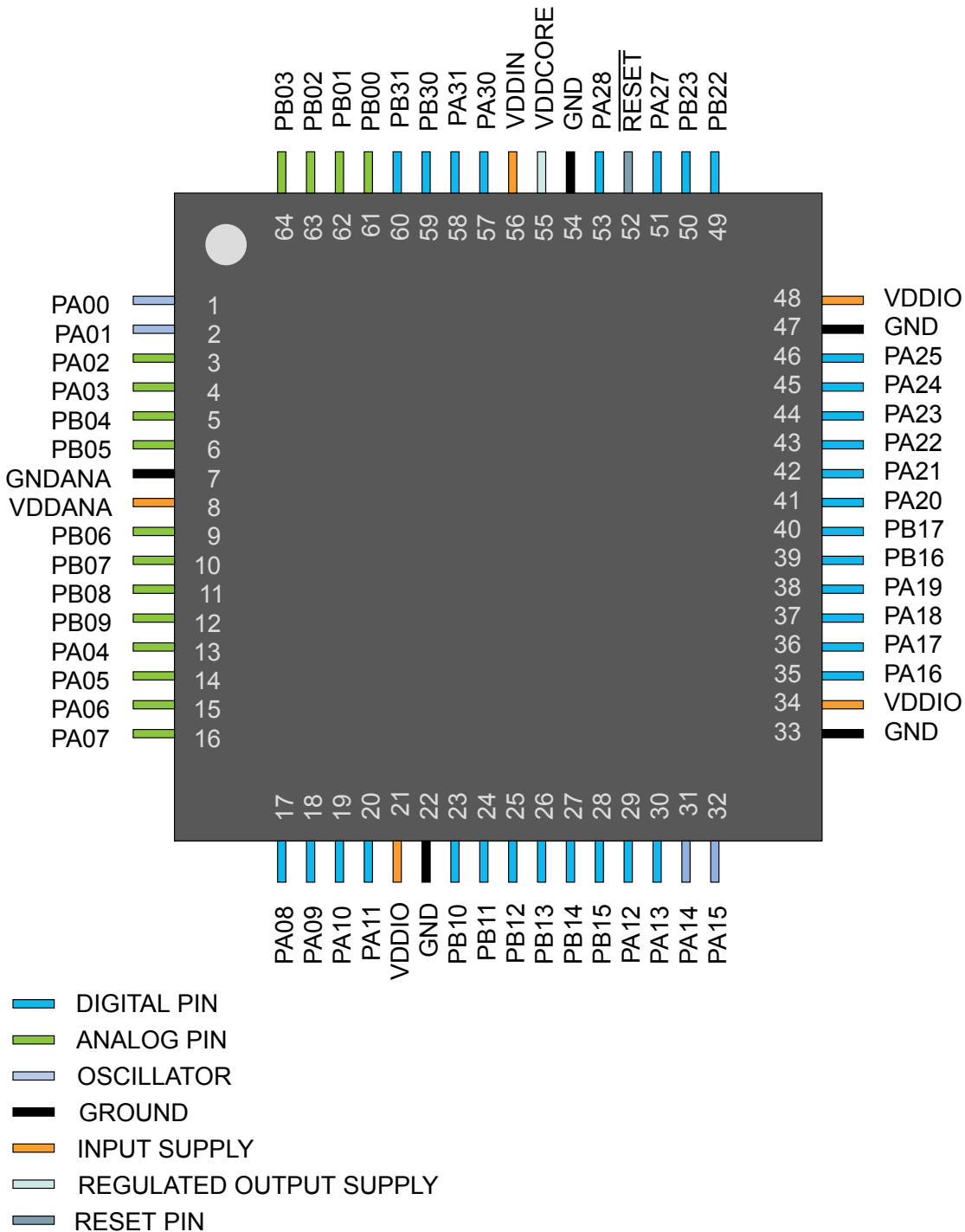
Table 3-7. Device Variant B

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21J15B-AU	32K	4K	TQFP64	Tray
ATSAMD21J15B-AUT				Tape & Reel
ATSAMD21J15B-AF				Tray
ATSAMD21J15B-AFT				Tape & Reel
ATSAMD21J15B-MU			QFN64	Tray
ATSAMD21J15B-MUT				Tape & Reel
ATSAMD21J15B-MF				Tray
ATSAMD21J15B-MFT				Tape & Reel
ATSAMD21J16B-AU	64K	8K	TQFP64	Tray
ATSAMD21J16B-AUT				Tape & Reel
ATSAMD21J16B-AF				Tray
ATSAMD21J16B-AFT				Tape & Reel
ATSAMD21J16B-MU			QFN64	Tray
ATSAMD21J16B-MUT				Tape & Reel
ATSAMD21J16B-MF				Tray
ATSAMD21J16B-MFT				Tape & Reel
ATSAMD21J16B-CU			UFBGA64	Tray
ATSAMD21J16B-CUT				Tape & Reel

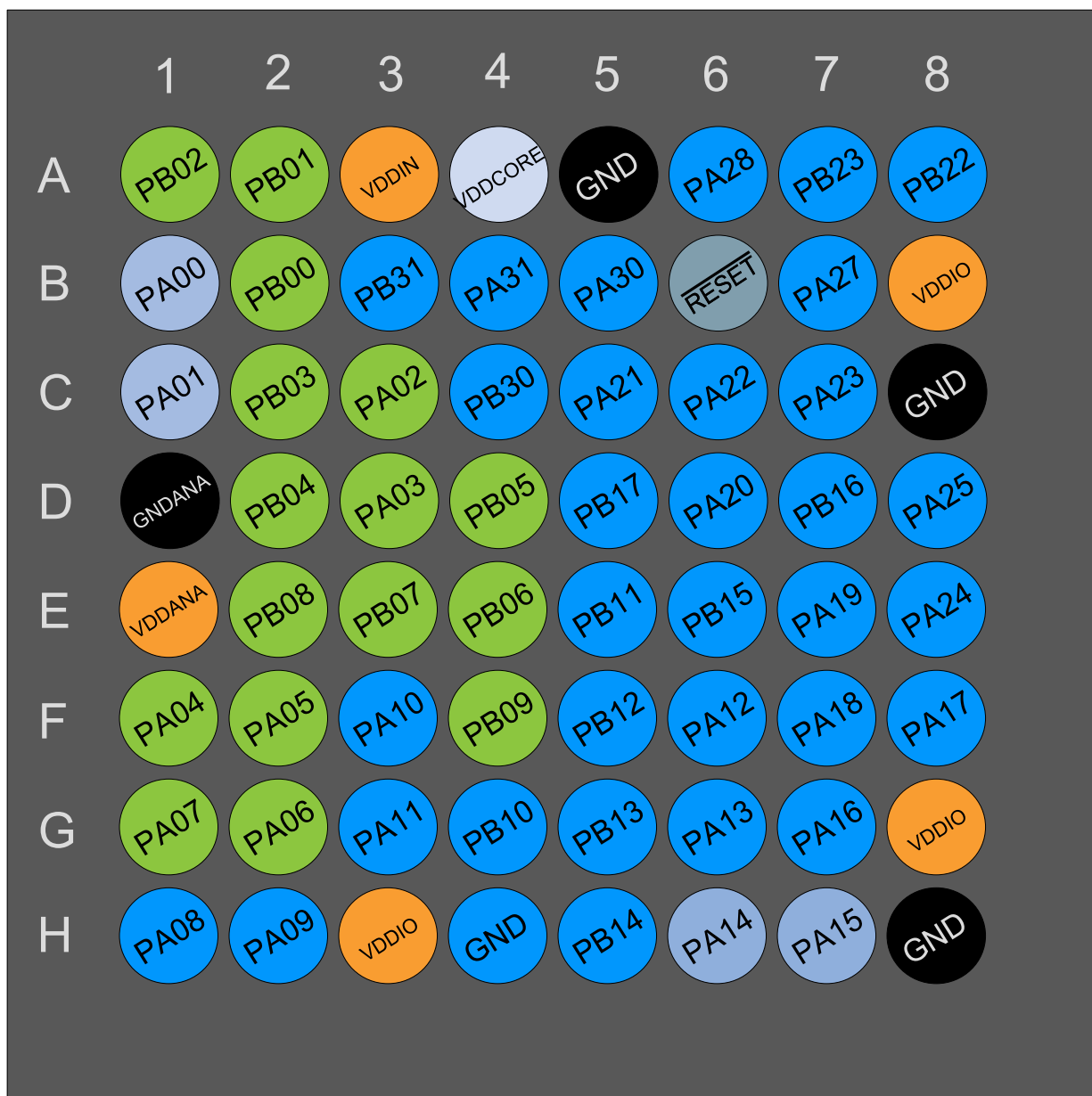
5. Pinout

5.1 SAM D21J

5.1.1 QFN64 / TQFP64



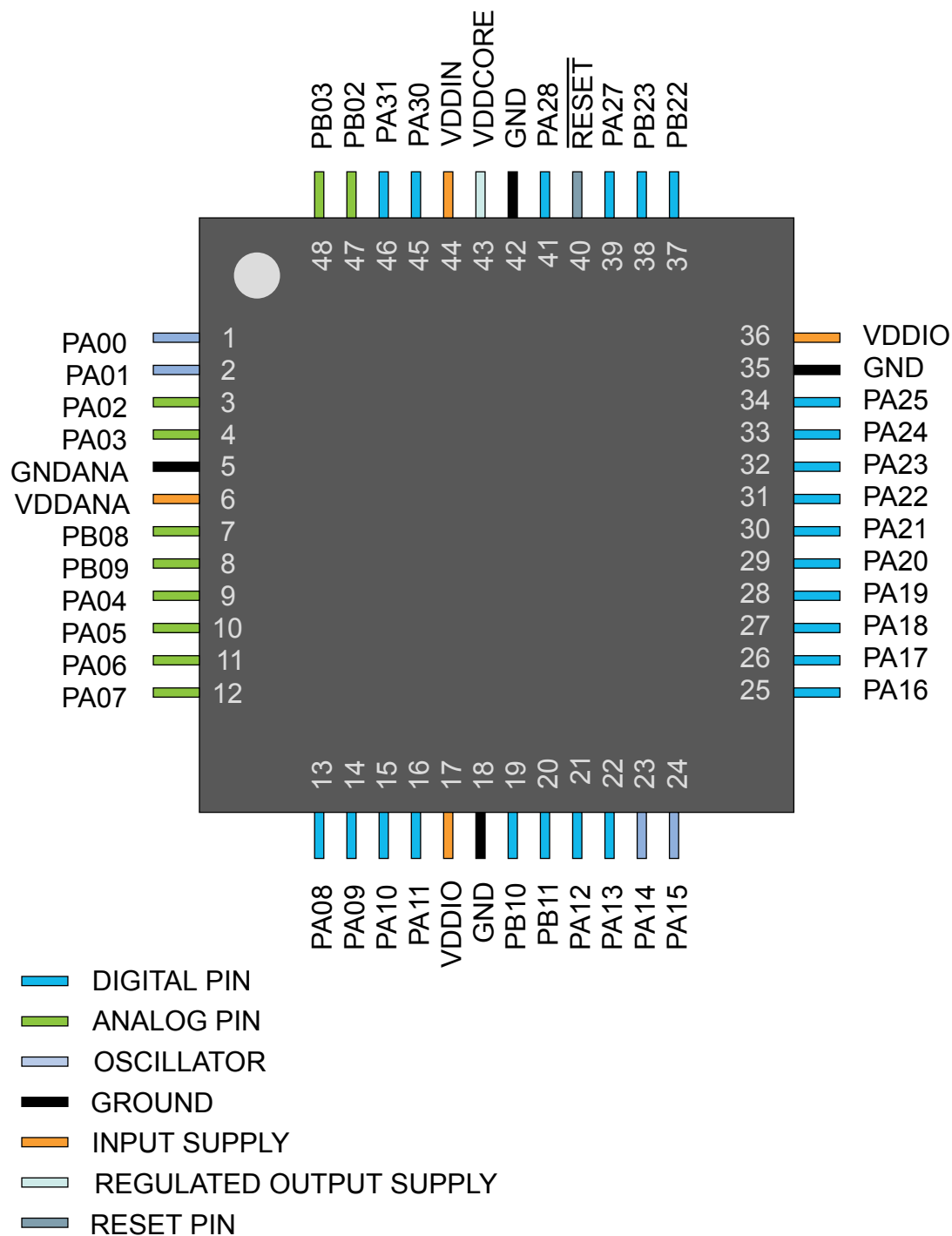
5.1.2 UFBGA64



- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

5.2 SAM D21G

5.2.1 QFN48 / TQFP48



- The System Timer is a 24-bit timer that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- Nested Vectored Interrupt Controller (NVIC)
 - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to [Nested Vector Interrupt Controller](#) and the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Control Block (SCB)
 - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (www.arm.com).
- Micro Trace Buffer (MTB)
 - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section [Micro Trace Buffer](#) and the CoreSight MTB-M0+ Technical Reference Manual for details (www.arm.com).

7.1.3 Cortex-M0+ Address Map

Table 7-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000 (see also Product Mapping)	Micro Trace Buffer (MTB)

7.1.4 I/O Interface

7.1.4.1 Overview

Because accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, the Cortex-M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O accesses to be sustained for as long as needed. Refer to *CPU Local Bus* for more information.

7.1.4.2 Description

Direct access to PORT registers.

7.2 Nested Vector Interrupt Controller

7.2.1 Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM D21 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (www.arm.com).

7.2.2 Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear

Peripheral Source	NVIC Line
AC – Analog Comparator	24
DAC – Digital-to-Analog Converter	25
PTC – Peripheral Touch Controller	26
I2S - Inter IC Sound	27

7.3 Micro Trace Buffer

7.3.1 Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

7.3.2 Overview

When enabled, the MTB records changes in program flow, reported by the Cortex-M0+ processor over the execution trace interface shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. This information is stored as trace packets in the SRAM by the MTB. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB simultaneously stores trace information into the SRAM, and gives the processor access to the SRAM. The MTB ensures that trace write accesses have priority over processor accesses.

The execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects the processor PC value changes non-sequentially. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has 4 programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit,
- MASTER: Contains the main trace enable bit and other trace control fields,
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits,
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

7.4 High-Speed Bus System

7.4.1 Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2 Configuration

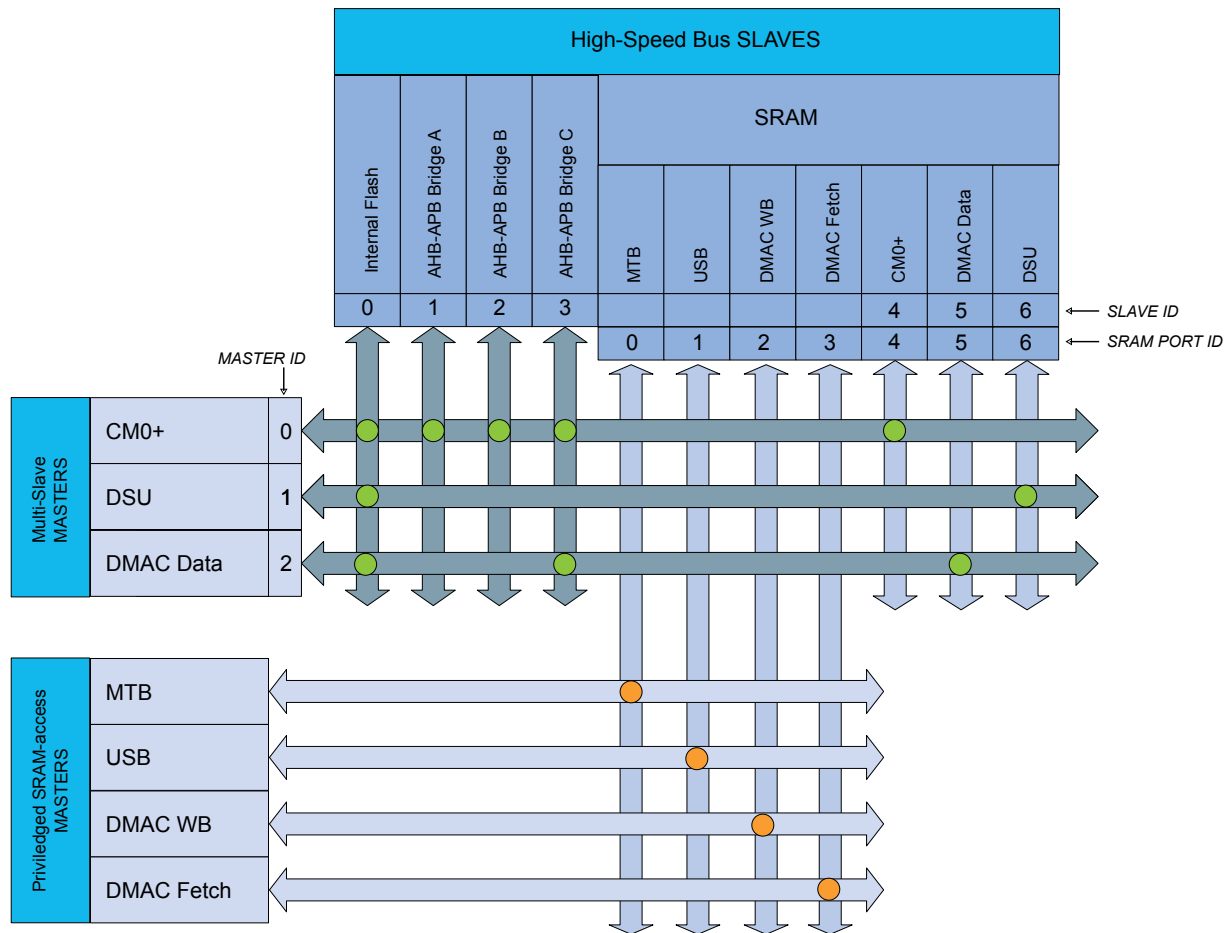


Table 7-4. Bus Matrix Masters

Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1

Table 7-5. Bus Matrix Slaves

Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
AHB-APB Bridge A	1
AHB-APB Bridge B	2
AHB-APB Bridge C	3
SRAM Port 4 - CM0+ Access	4
SRAM Port 5 - DMAC Data Access	5
SRAM Port 6 - DSU Access	6

Table 7-6. SRAM Port Connection

SRAM Port Connection	Port ID	Connection Type
MTB - Micro Trace Buffer	0	Direct
USB - Universal Serial Bus	1	Direct
DMAC - Direct Memory Access Controller - Write-Back Access	2	Direct
DMAC - Direct Memory Access Controller - Fetch Access	3	Direct
CM0+ - Cortex M0+ Processor	4	Bus Matrix
DMAC - Direct Memory Access Controller - Data Access	5	Bus Matrix
DSU - Device Service Unit	6	Bus Matrix

7.4.3 SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, the different masters can be configured to have a given priority for different type of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration is shown in Table. Quality of Service.

Table 7-7. Quality of Service

Value	Name	Description
00	DISABLE	Background (no sensitive operation)
01	LOW	Sensitive Bandwidth
10	MEDIUM	Sensitive Latency
11	HIGH	Critical Latency

If a master is configured with QoS level 0x00 or 0x01 there will be minimum one cycle latency for the RAM access.

The priority order for concurrent accesses are decided by two factors. First the QoS level for the master and then a static priority given by table nn-mm (table: SRAM port connection) where the lowest port ID has the highest static priority.

The MTB has fixed QoS level 3 and the DSU has fixed QoS level 1.

The CPU QoS level can be written/read at address 0x41007110, bits [1:0]. Its reset value is 0x0.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

7.5 AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals.

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

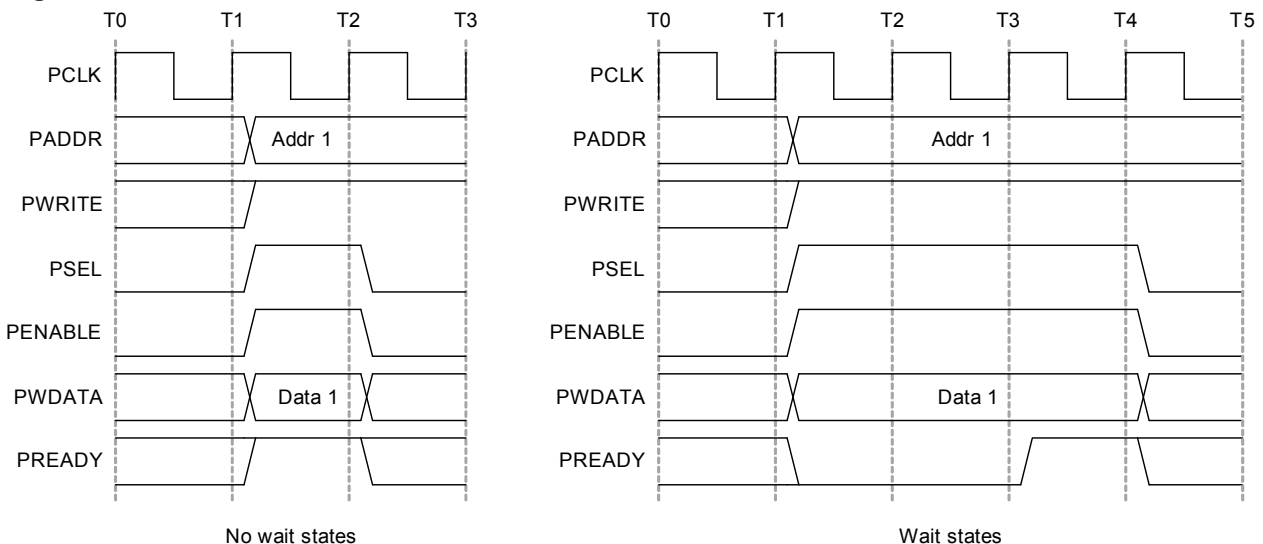
- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPxBx_AHB) must be enabled. See *PM – Power Manager* for details.

Figure 7-1. APB Write Access.



7.6.2 Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

7.6.2.1 PAC0 Register Description

Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

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Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – DSU

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET

Offset: 0x04

Reset: 0x000002

Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 11, 12, 13, 14, 15 – TC3, TC4, TC5, TC4, TC7

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 8, 9, 10 – TCCn

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – EVSYS

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 0:1, 2:3, 4:5, 6:7, 8:9, 10:11 – SERCOMn

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x00800000

8.2 Package Drawings

8.2.1 64 pin TQFP

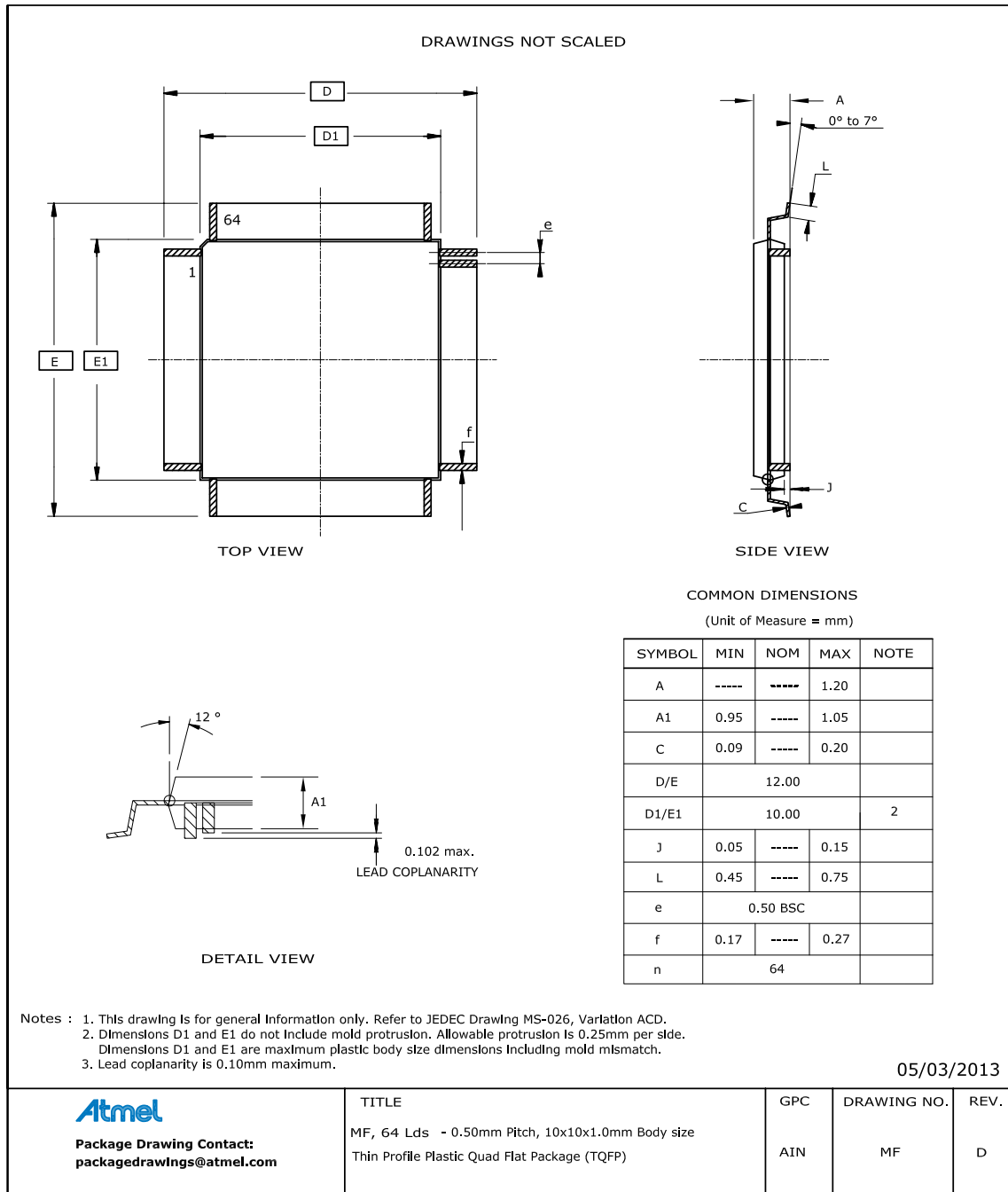


Table 8-2. Device and Package Maximum Weight

300	mg
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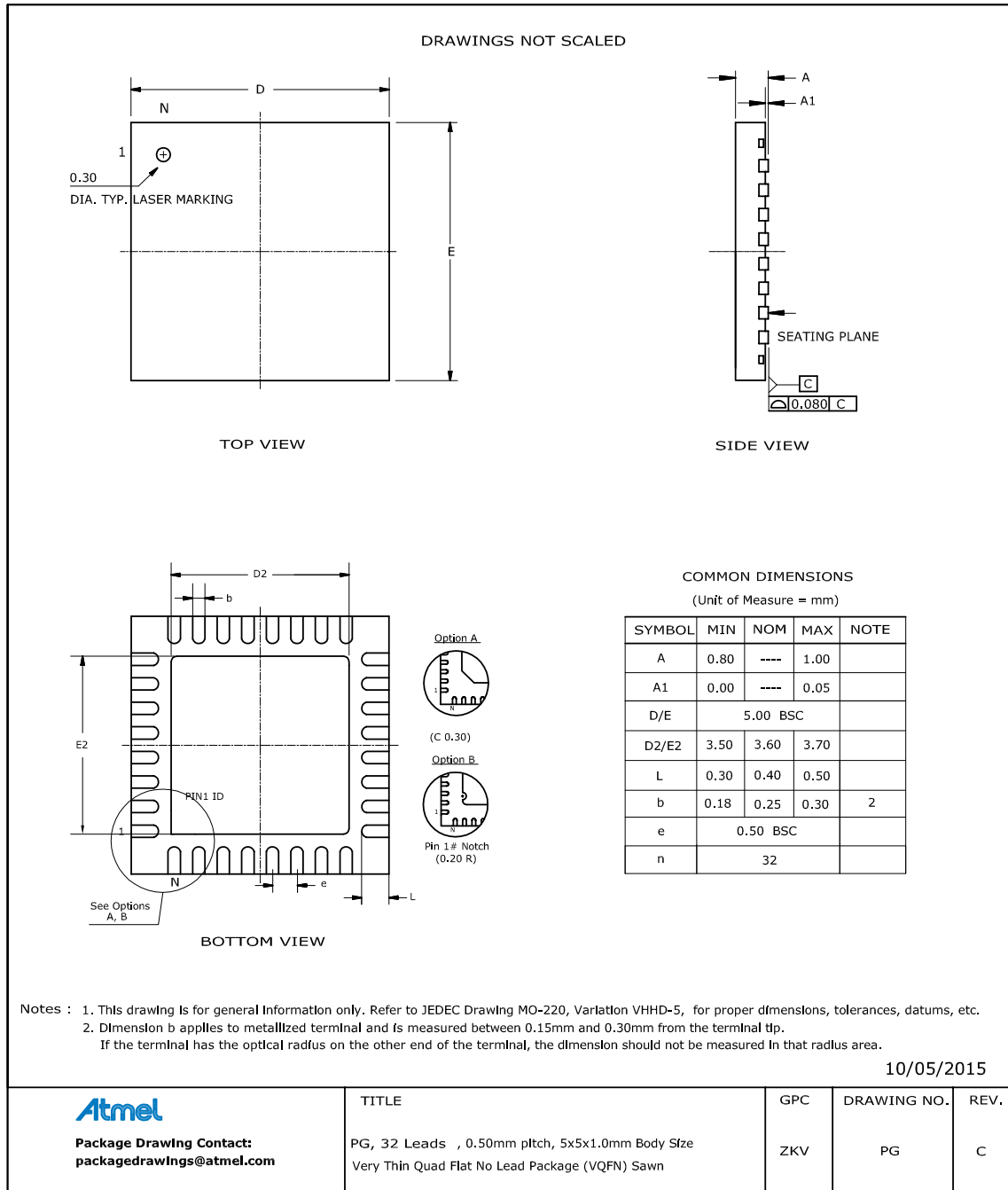
Table 8-3. Package Characteristics

Moisture Sensitivity Level	MSL3
----------------------------	------

Table 8-22. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.8 32 pin QFN



Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 8-23. Device and Package Maximum Weight

90	mg
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Table 8-24. Package Characteristics

Moisture Sensitivity Level	MSL3
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Table 8-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.9 35 ball WLCSP (Device Variant B)

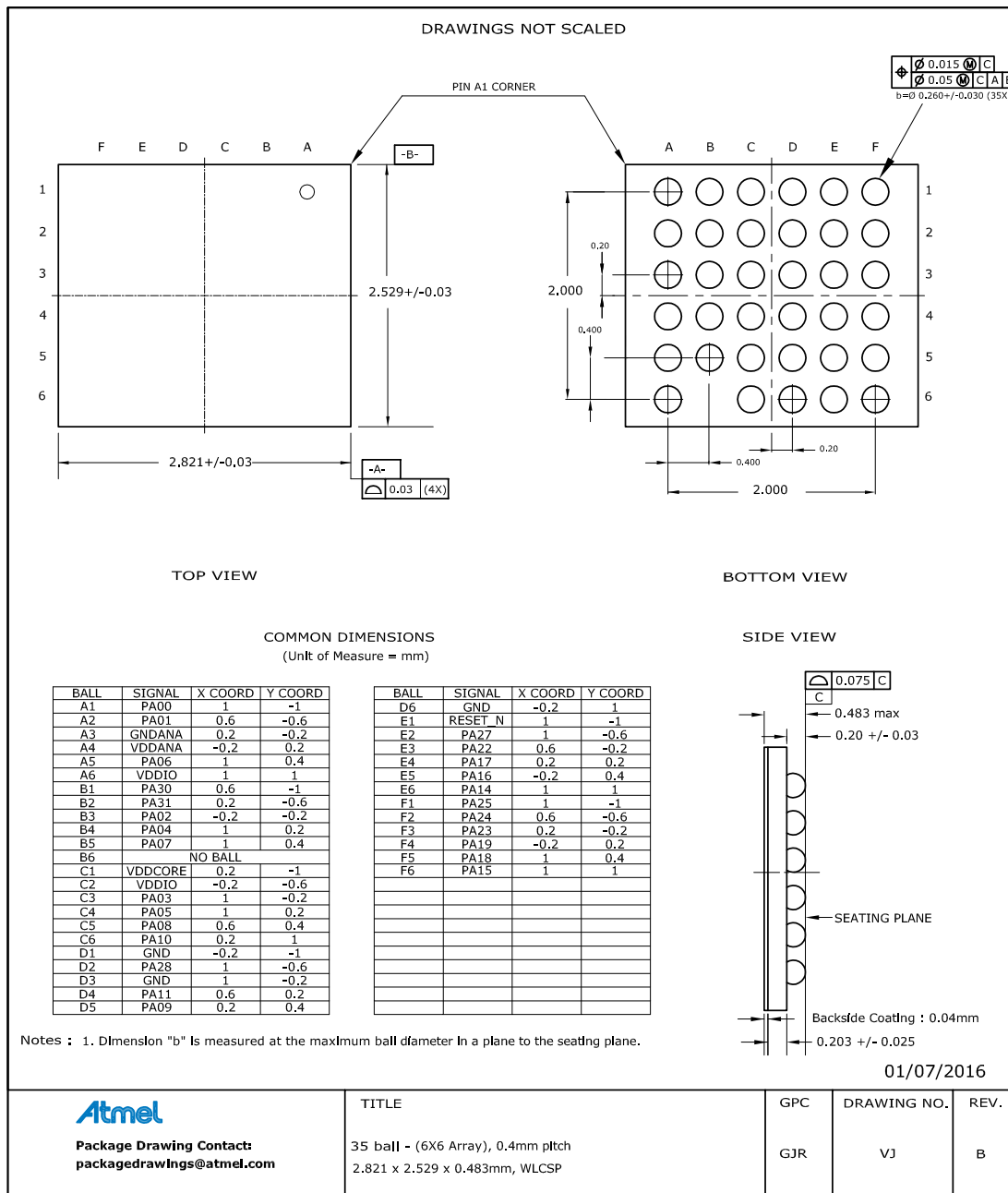


Table 8-26. Device and Package Maximum Weight

6.2	mg
-----	----

Table 8-27. Package Characteristics

Moisture Sensitivity Level	MSL1
----------------------------	------

Table 8-28. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.2.10 35 ball WLCSP (Device Variant C)

