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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atsamd21j18a-mut">https://www.e-xfl.com/product-detail/microchip-technology/atsamd21j18a-mut</a>

## 32-bit ARM-Based Microcontrollers

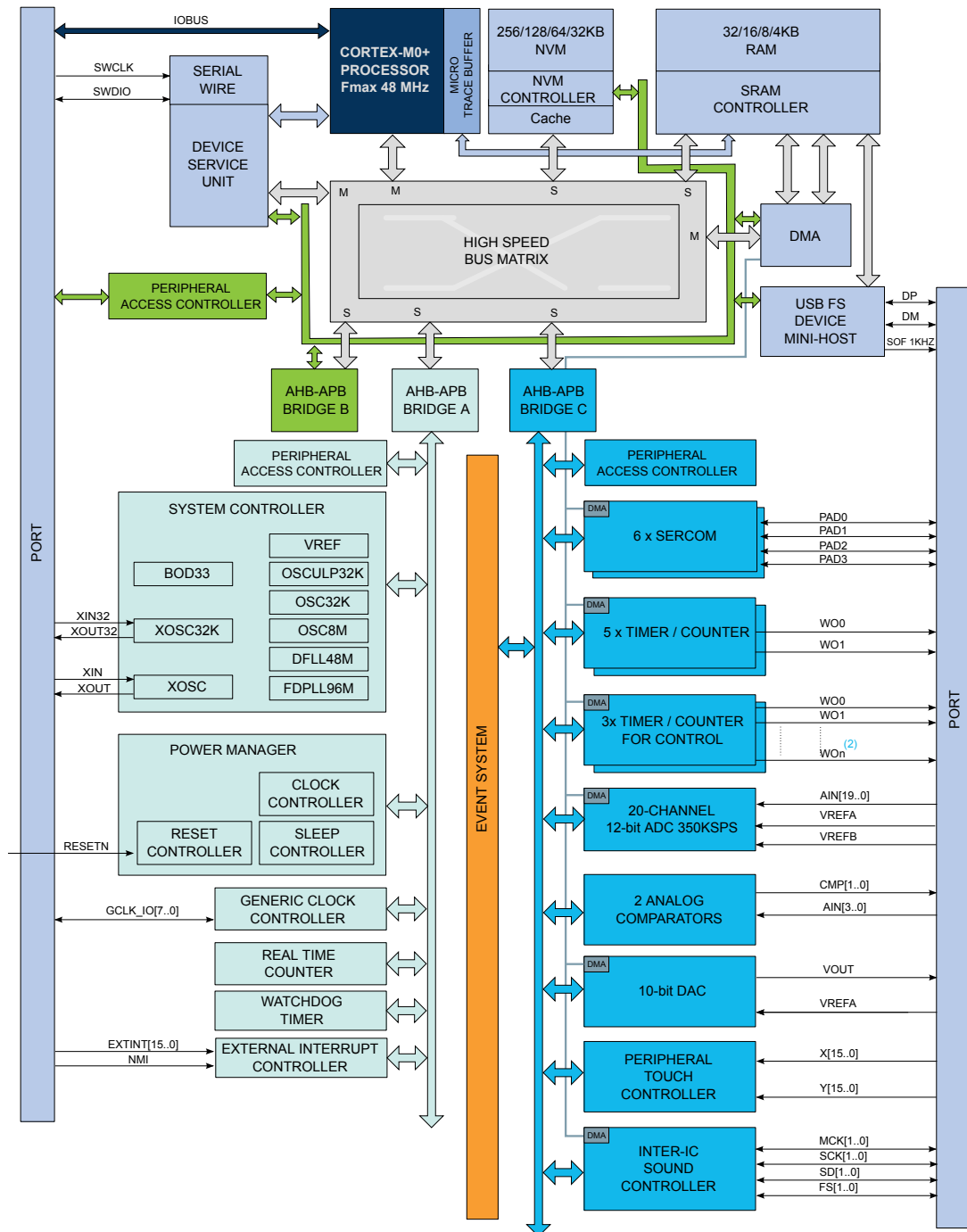
**Table 3-2. Device Variant B**

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21E15B-AU	32K	4K	TQFP32	Tray
ATSAMD21E15B-AUT				Tape & Reel
ATSAMD21E15B-AF				Tray
ATSAMD21E15B-AFT				Tape & Reel
ATSAMD21E15B-MU			QFN32	Tray
ATSAMD21E15B-MUT				Tape & Reel
ATSAMD21E15B-MF				Tray
ATSAMD21E15B-MFT				Tape & Reel
ATSAMD21E15B-UUT			WLCSP35 (GJR)	Tape & Reel
ATSAMD21E16B-AU	64K	8K	TQFP32	Tray
ATSAMD21E16B-AUT				Tape & Reel
ATSAMD21E16B-AF				Tray
ATSAMD21E16B-AFT				Tape & Reel
ATSAMD21E16B-MU			QFN32	Tray
ATSAMD21E16B-MUT				Tape & Reel
ATSAMD21E16B-MF				Tray
ATSAMD21E16B-MFT				Tape & Reel
ATSAMD21E16B-UUT	64K	8K	WLCSP35 (GJR)	Tape & Reel

**Table 3-3. Device Variant C**

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21E15C-UUT	32K	4K	WLCSP35 (GJS)	Tape & Reel
ATSAMD21E16C-UUT	64K	8K	WLCSP35 (GJS)	Tape & Reel

#### 4. Block Diagram

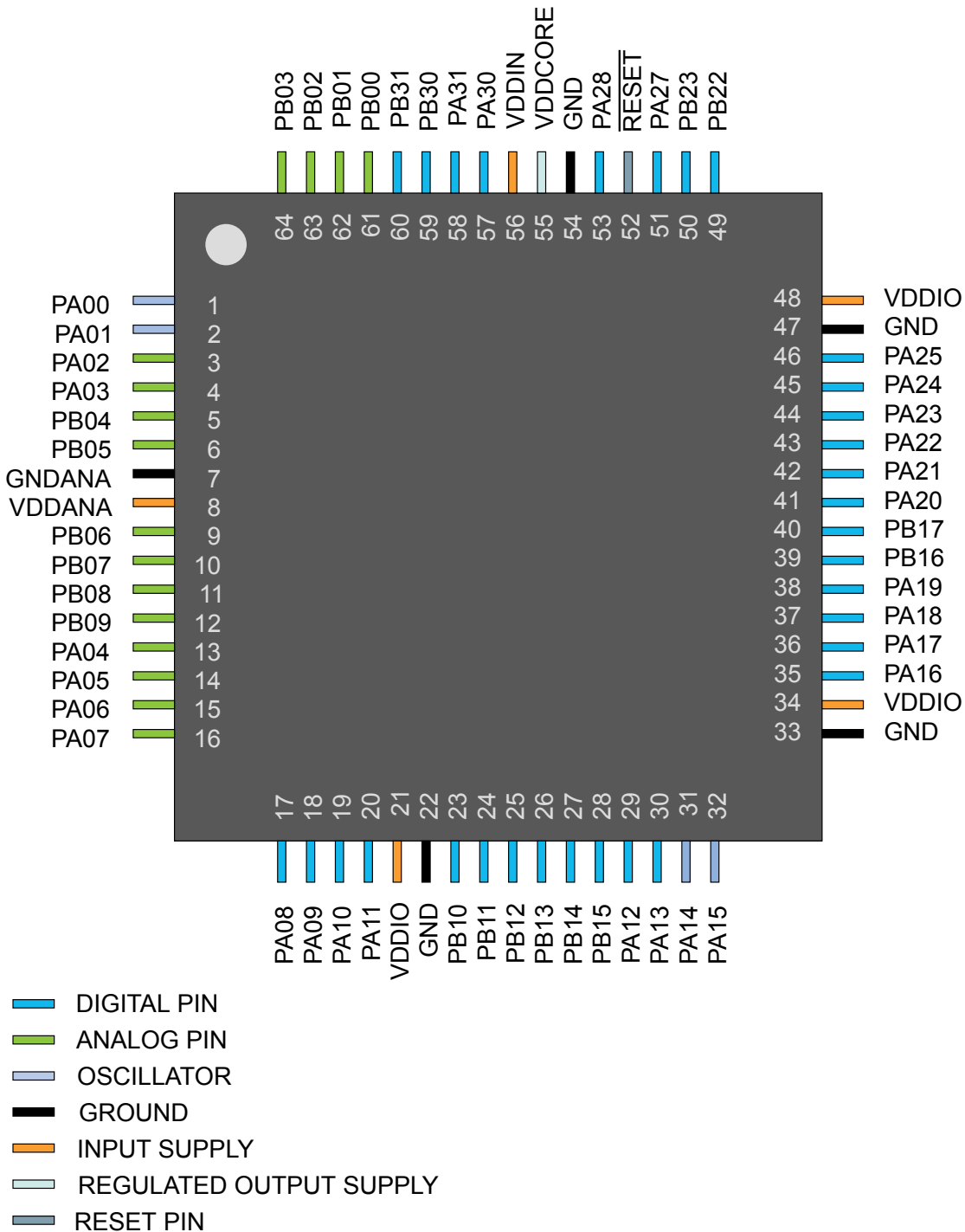


1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to the Configuration Summary for details.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines. Refer to the TCC Configuration for details.

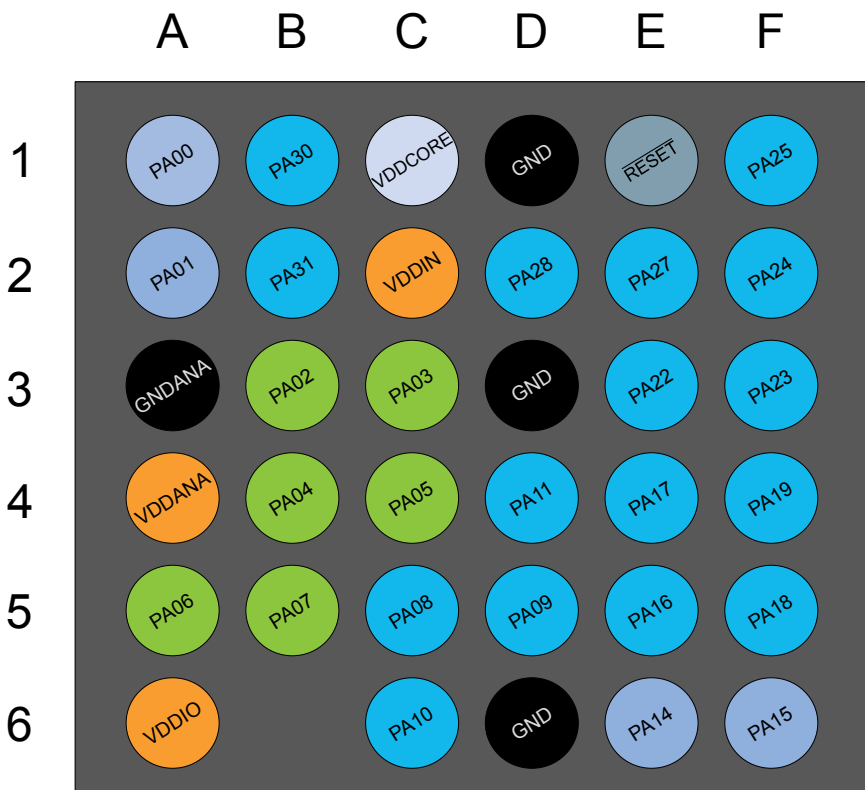
## 5. Pinout

### 5.1 SAM D21J

#### 5.1.1 QFN64 / TQFP64



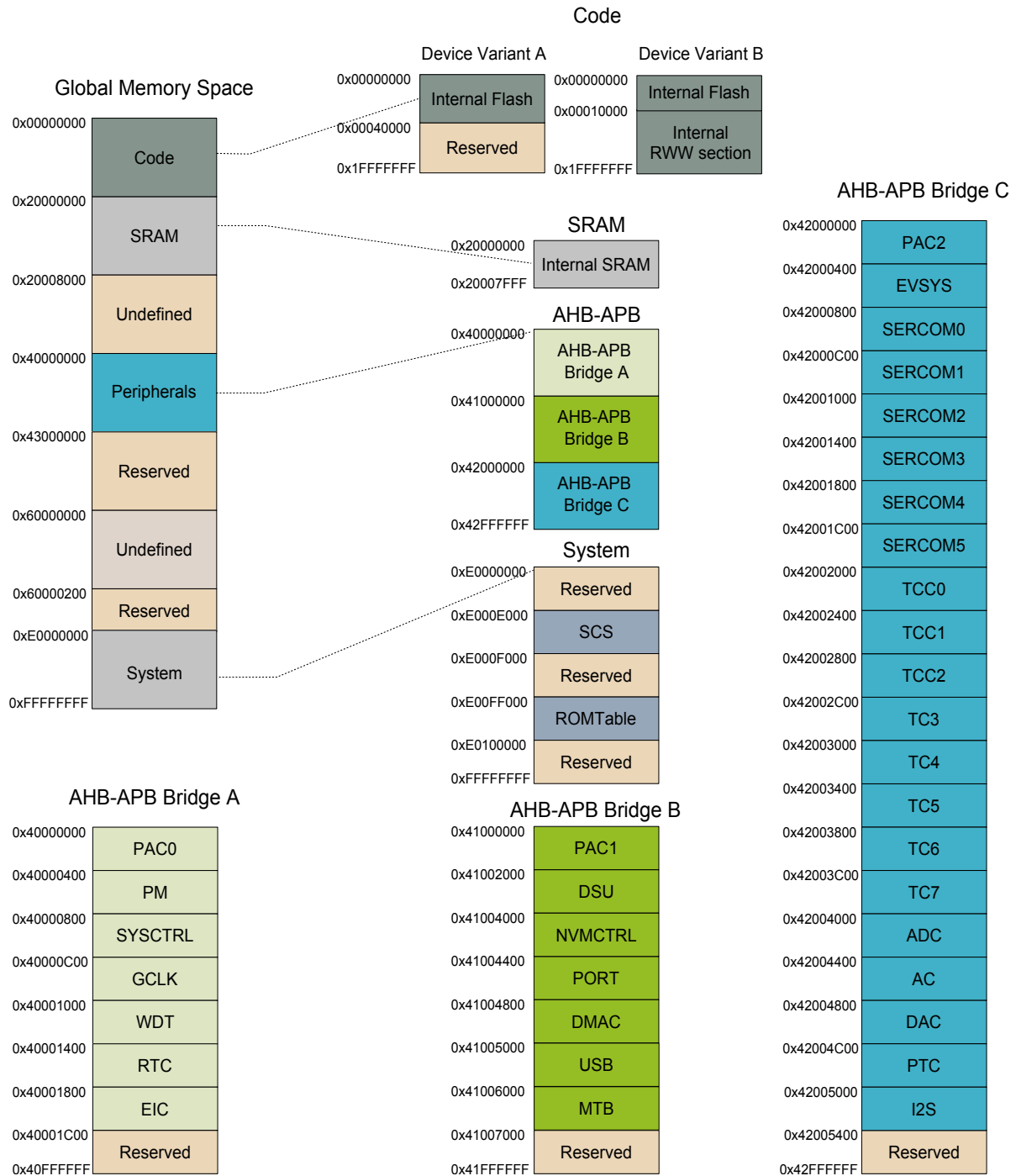
## 5.3.2 WLCSP35



- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

## 6. Product Mapping

Figure 6-1. SAM D21 Product Mapping



This figure represents the full configuration of the SAM D21 with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the [Configuration Summary](#) for details.

## 7. Processor And Architecture

### 7.1 Cortex M0+ Processor

The SAM D21 implements the ARM® Cortex®-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The ARM Cortex-M0+ implemented is revision r0p1. For more information refer to <http://www.arm.com>.

#### 7.1.1 Cortex M0+ Configuration

**Table 7-1. Cortex M0+ Configuration**

Features	Configurable option	Device configuration
Interrupts	External interrupts 0-32	28
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent <sup>(1)</sup>
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

**Note:**

1. All software run in privileged mode only.

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores.

#### 7.1.2 Cortex-M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details ([www.arm.com](http://www.arm.com)).
- System Timer (SysTick)

- The System Timer is a 24-bit timer that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details ([www.arm.com](http://www.arm.com)).
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to [Nested Vector Interrupt Controller](#) and the Cortex-M0+ Technical Reference Manual for details ([www.arm.com](http://www.arm.com)).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details ([www.arm.com](http://www.arm.com)).
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section [Micro Trace Buffer](#) and the CoreSight MTB-M0+ Technical Reference Manual for details ([www.arm.com](http://www.arm.com)).

## 7.1.3 Cortex-M0+ Address Map

**Table 7-2. Cortex-M0+ Address Map**

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000 (see also Product Mapping)	Micro Trace Buffer (MTB)

## 7.1.4 I/O Interface

### 7.1.4.1 Overview

Because accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, the Cortex-M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O accesses to be sustained for as long as needed. Refer to *CPU Local Bus* for more information.

### 7.1.4.2 Description

Direct access to PORT registers.

## 7.2 Nested Vector Interrupt Controller

### 7.2.1 Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM D21 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual ([www.arm.com](http://www.arm.com)).

### 7.2.2 Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear



(INTFLAG) register. The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR). For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

**Table 7-3. Interrupt Line Mapping**

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager	0
SYSCTRL – System Control	1
WDT – Watchdog Timer	2
RTC – Real Time Counter	3
EIC – External Interrupt Controller	4
NVMCTRL – Non-Volatile Memory Controller	5
DMAC - Direct Memory Access Controller	6
USB - Universal Serial Bus	7
EVSYS – Event System	8
SERCOM0 – Serial Communication Interface 0	9
SERCOM1 – Serial Communication Interface 1	10
SERCOM2 – Serial Communication Interface 2	11
SERCOM3 – Serial Communication Interface 3	12
SERCOM4 – Serial Communication Interface 4	13
SERCOM5 – Serial Communication Interface 5	14
TCC0 – Timer Counter for Control 0	15
TCC1 – Timer Counter for Control 1	16
TCC2 – Timer Counter for Control 2	17
TC3 – Timer Counter 3	18
TC4 – Timer Counter 4	19
TC5 – Timer Counter 5	20
TC6 – Timer Counter 6	21
TC7 – Timer Counter 7	22
ADC – Analog-to-Digital Converter	23

The MTB has fixed QoS level 3 and the DSU has fixed QoS level 1.

The CPU QoS level can be written/read at address 0x41007110, bits [1:0]. Its reset value is 0x0.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

## 7.5 AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals.

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

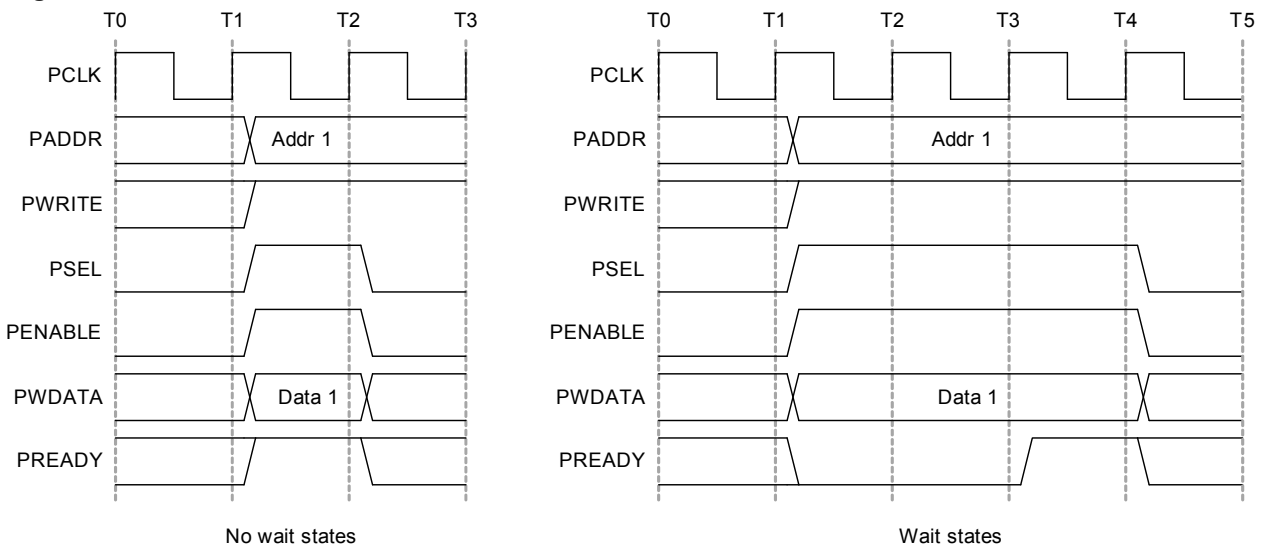
- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK\_HPxBx\_AHB) must be enabled. See *PM – Power Manager* for details.

**Figure 7-1. APB Write Access.**



## 7.6.2 Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

### 7.6.2.1 PAC0 Register Description

#### Write Protect Clear

**Name:** WPCLR

**Offset:** 0x00

**Reset:** 0x000000

**Property:** –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

#### Bit 6 – EIC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

#### Bit 5 – RTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## Bit 1 – PM

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## 7.6.2.2 PAC1 Register Description

### Write Protect Clear

**Name:** WPCLR

**Offset:** 0x00

**Reset:** 0x000002

**Property:** –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
		MTB	USB		PORT	NVMCTRL	DSU	
Access		R/W	R/W		R/W	R/W	R/W	
Reset		0	0		0	0	1	

## Bit 6 – MTB

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## Bit 5 – USB

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

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**Reset:** 0x00800000

**Property:** –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
				I2S	PTC	DAC	AC	ADC
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC7	TC4	TC5	TC4	TC3	TCC2	TCC1	TCC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
							EVSYS	
Access							R/W	
Reset							0	

### Bit 20 – I2S

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

### Bit 19 – PTC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

### Bit 18 – DAC:

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

### Bit 17 – AC

Writing a zero to these bits has no effect.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## Bit 16 – ADC

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## Bits 11, 12, 13, 14, 15 – TC3, TC4, TC5, TC6, TC7

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## Bits 8, 9, 10 – TCCn

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## Bits 2, 3, 4, 5, 6, 7 – SERCOMn

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## Bit 1 – EVSYS

Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

## 8. Packaging Information

### 8.1 Thermal Considerations

#### Related Links

[Junction Temperature](#)

#### 8.1.1 Thermal Resistance Data

The following Table summarizes the thermal resistance data depending on the package.

**Table 8-1. Thermal Resistance Data**

Package Type	$\theta_{JA}$	$\theta_{JC}$
32-pin TQFP	64.7°C/W	23.1°C/W
48-pin TQFP	63.6°C/W	12.2°C/W
64-pin TQFP	60.9°C/W	12.2°C/W
32-pin QFN	40.9°C/W	15.2°C/W
48-pin QFN	32.0°C/W	10.9°C/W
64-pin QFN	32.5°C/W	10.7°C/W
35-ball WLCSP	41.8°C/W	2.26°C/W

#### 8.1.2 Junction Temperature

The average chip-junction temperature,  $T_J$ , in °C can be obtained from the following:

1.  $T_J = T_A + (P_D \times \theta_{JA})$
2.  $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- $\theta_{JA}$  = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- $\theta_{JC}$  = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$  = Thermal resistance (°C/W) specification of the external cooling device
- $P_D$  = Device power consumption (W)
- $T_A$  = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature  $T_J$  in °C.

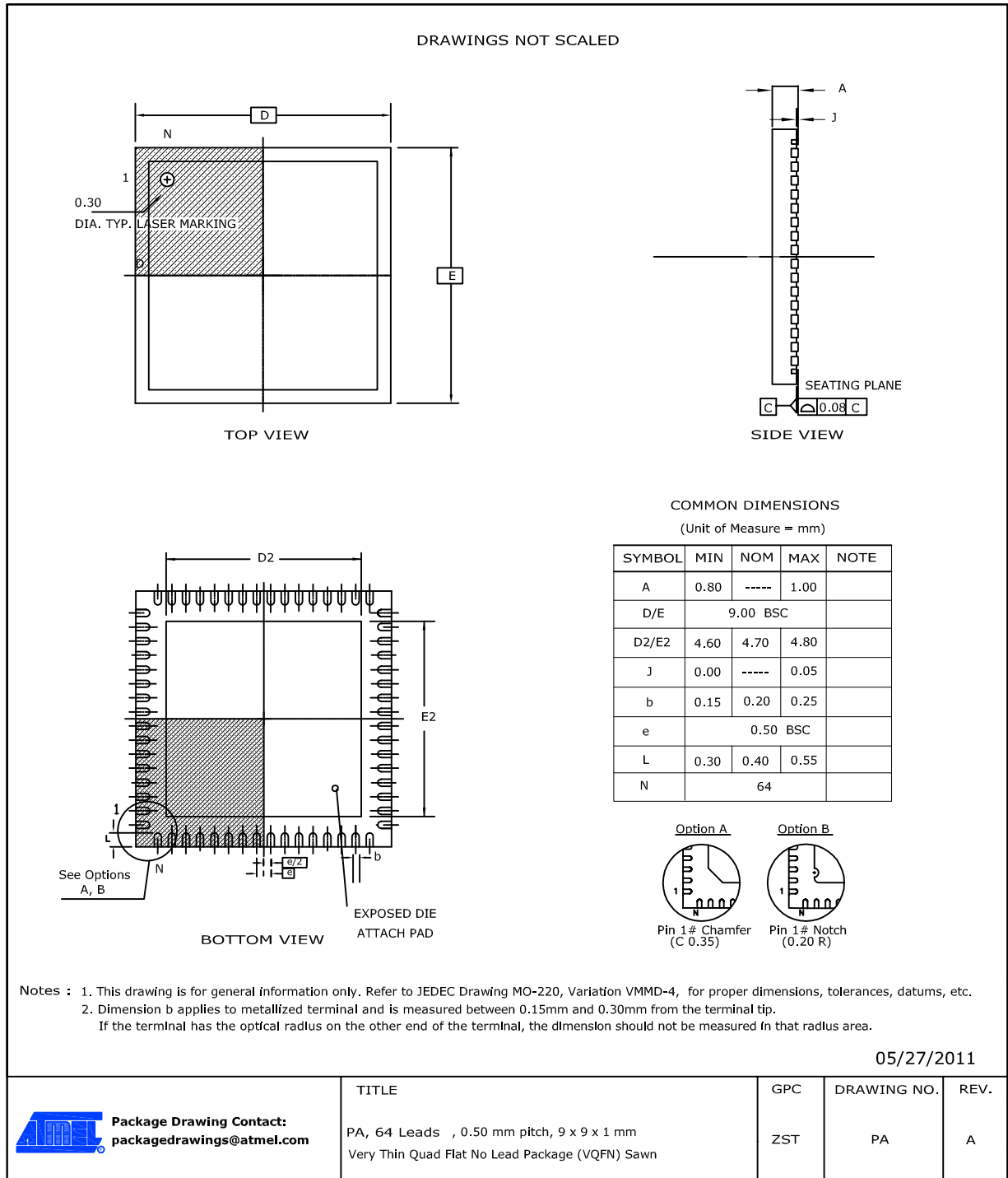
#### Related Links

[Thermal Considerations](#)

**Table 8-4. Package Reference**

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

## 8.2.2 64 pin QFN



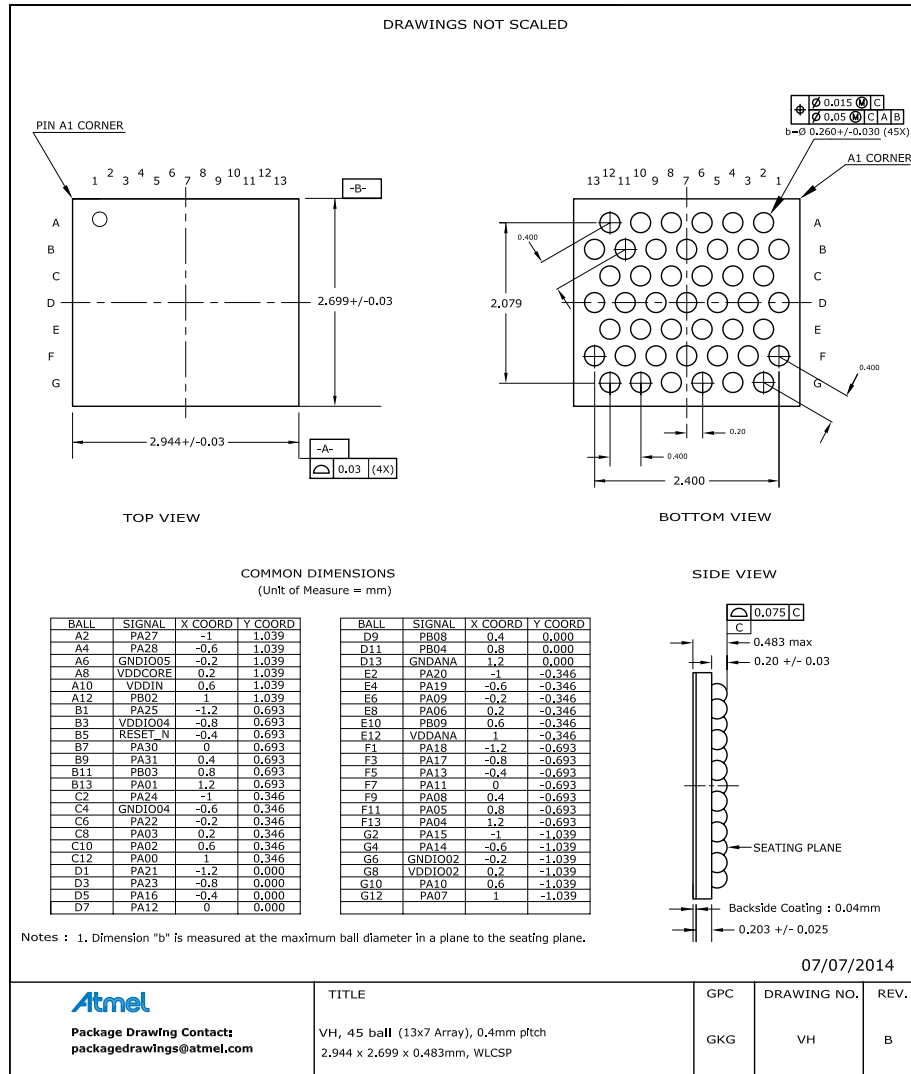
**Note:** The exposed die attach pad is not connected electrically inside the device.



**Table 8-16. Package Reference**

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

## 8.2.6 45-ball WLCSP



**Table 8-17. Device and Package Maximum Weight**

7.3	mg
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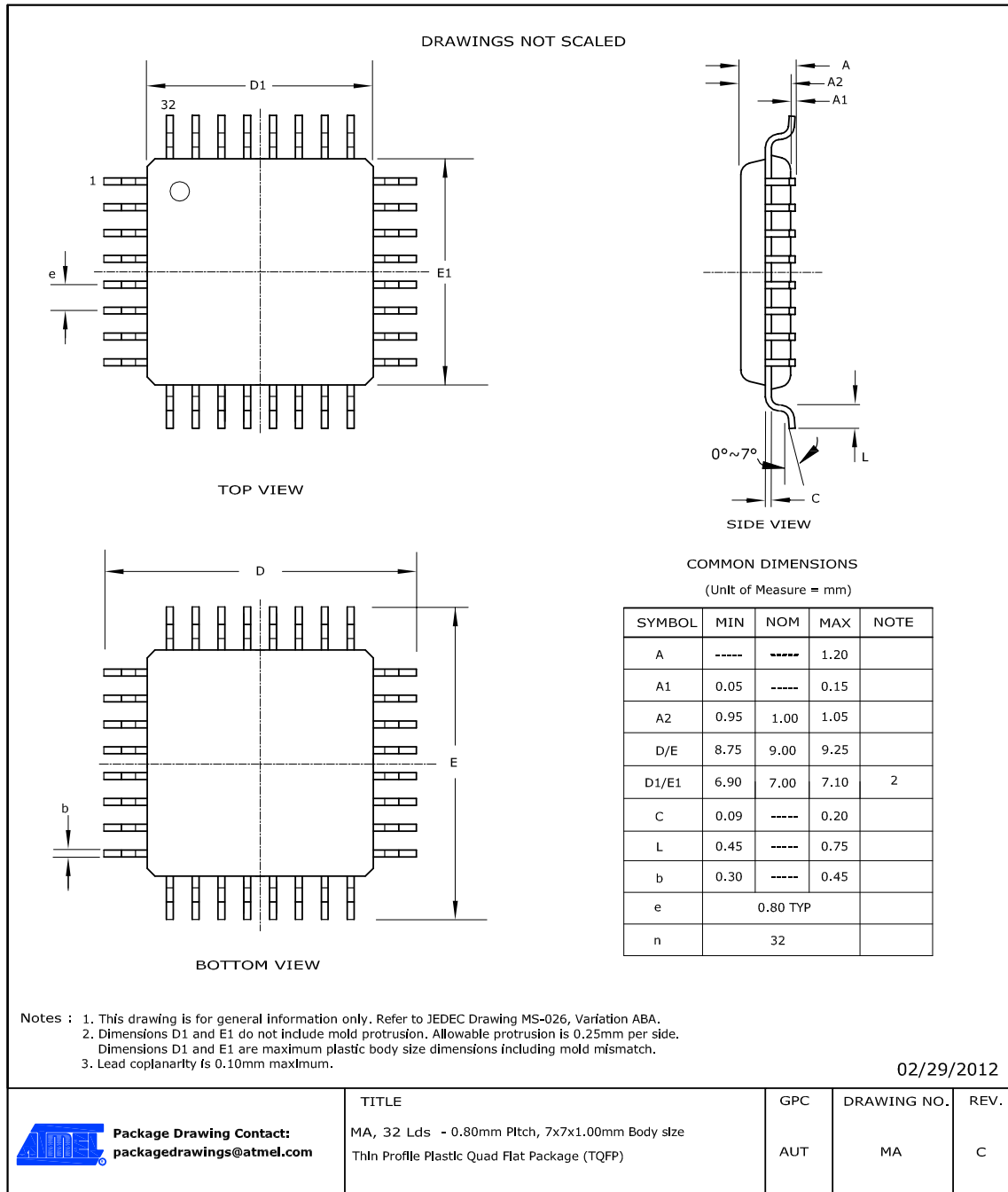
**Table 8-18. Package Characteristics**

Moisture Sensitivity Level	MSL1
----------------------------	------

**Table 8-19. Package Reference**

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

## 8.2.7 32 pin TQFP



**Table 8-20. Device and Package Maximum Weight**

100	mg
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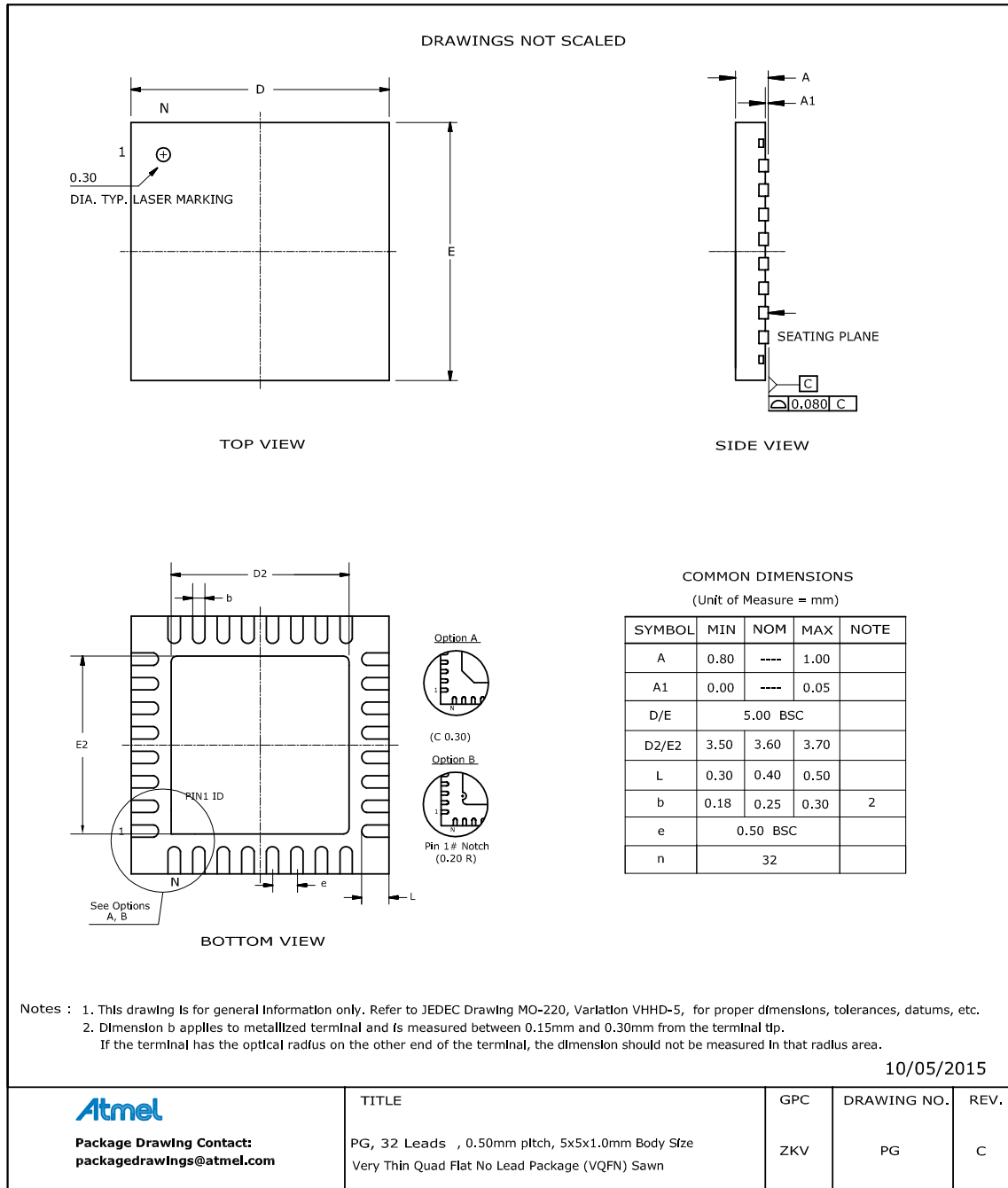
**Table 8-21. Package Characteristics**

Moisture Sensitivity Level	MSL3
----------------------------	------

**Table 8-22. Package Reference**

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

## 8.2.8 32 pin QFN



**Note:** The exposed die attach pad is connected inside the device to GND and GNDANA.

**Table 8-23. Device and Package Maximum Weight**

90	mg
----	----

**Table 8-29. Device and Package Maximum Weight**

6.22	mg
------	----

**Table 8-30. Package Characteristics**

Moisture Sensitivity Level	MSL1
----------------------------	------

**Table 8-31. Package Reference**

JEDEC Drawing Reference	N/A
JESD97 Classification	e1

## 8.3 Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

**Table 8-32.**

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.

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