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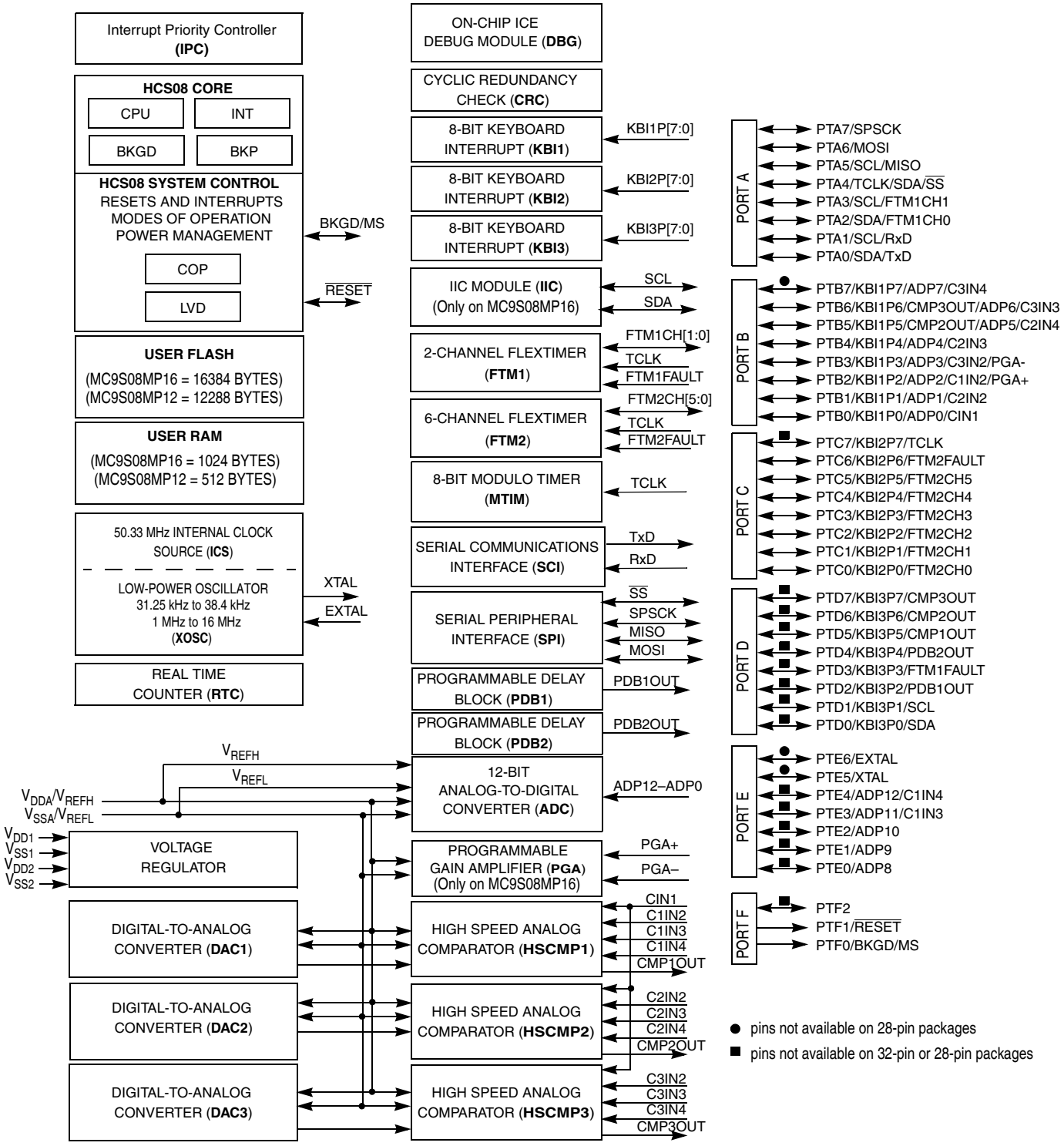
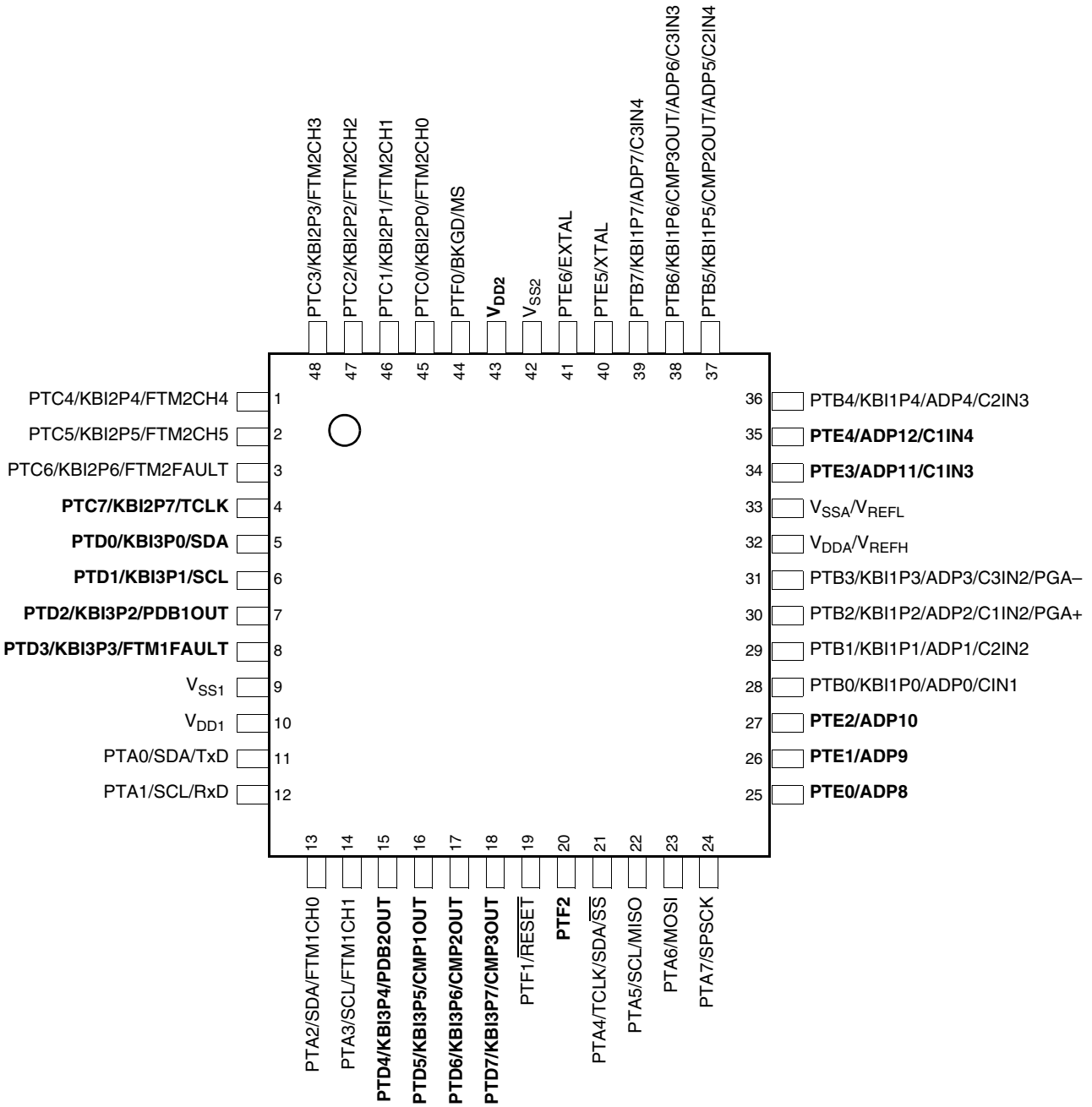


Notes: When PTF1 is configured as RESET, pin becomes bi-directional with output being open-drain drive containing an internal pull-up device.
When PTF0 is configured as BKGD, pin becomes bi-directional.
V_{DD2} pad is tied internally on 32-pin and 28-pin packages,
V_{SS2} pad is tied internally on 28-pin packages

Figure 1. MC9S08MP16 Series Block Diagram

1 Pin Assignments

This section shows the pin assignments for the MC9S08MP16 Series devices.



Note: Pins in **bold** are lost in the next lower pin count package.

Figure 2. MC9S08MP16 Series in 48-LQFP

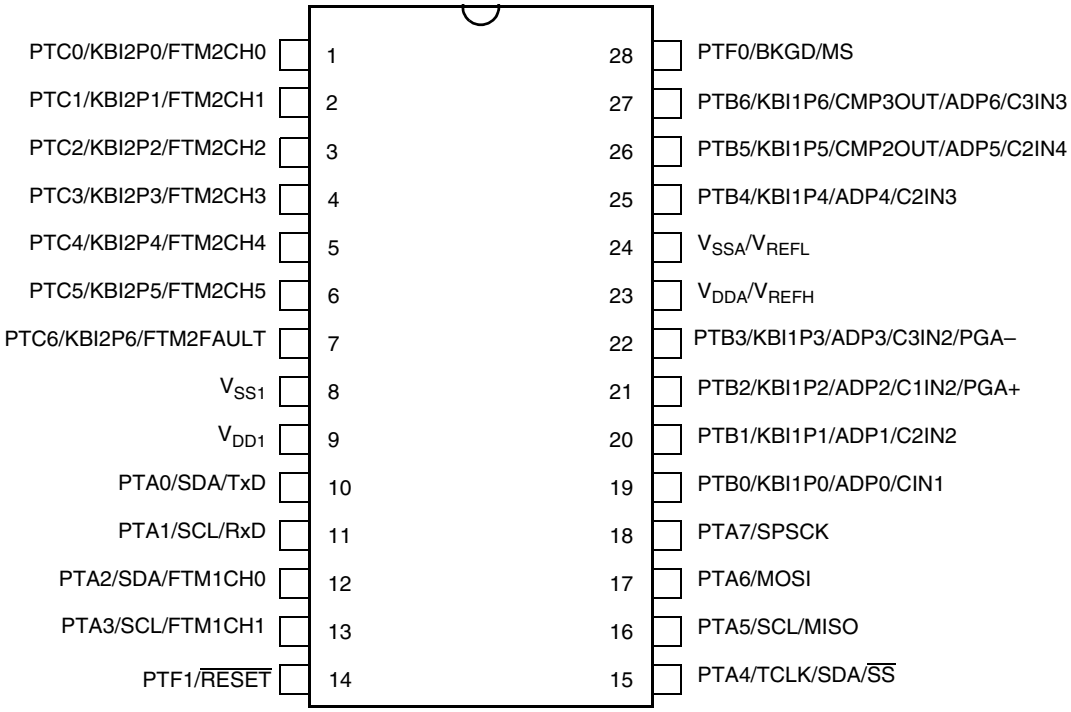


Figure 4. MC9S08MP16 Series in 28-Pin SOIC Package

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number			<-- Lowest **Priority** --> Highest				
48	**32 LQFP**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
35	—	—	PTE4		ADP12[6]	C1IN4[6]	
36	23	25	PTB4	KBI1P4		ADP4[6]	C2IN3[6]
37	24	26	PTB5	KBI1P5	CMP2OUT[2]	ADP5[6]	C2IN4[6]
38	25	27	PTB6	KBI1P6	CMP3OUT[3]	ADP6[6]	C3IN3[6]
39	26	—	PTB7	KBI1P7		ADP7[6]	C3IN4[6]
40	27	—	PTE5	XTAL			
41	28	—	PTE6	EXTAL			
42	29	—					V_{SS2}
43	—	—					V_{DD2}
44	30	28	PTF0	BKGD	MS		
45	31	1	PTC0	KBI2P0	FTM2CH0		
46	32	2	PTC1	KBI2P1	FTM2CH1		
47	1	3	PTC2	KBI2P2	FTM2CH2		
48	2	4	PTC3	KBI2P3	FTM2CH3		

1 TCLK pin can be repositioned using TCLKPS in SOPT2. Default reset location is PTC7.

2 HSCMP2 output CMP2OUT can be repositioned using the CMP2OPS in the SOPT2 register. Default reset location is PTD6.

3 HSCMP3 output CMP3OUT can be repositioned using the CMP3OPS in the SOPT2 register. Default reset location is PTD7.

4 Pin is open drain with an internal pullup that is always enabled. Pin does not contain a clamp diode to V_{DD} and should not be driven above V_{DD}. The voltage measured on the internally pulled up $\overline{\text{RESET}}$ will not be pulled to V_{DD}. The internal gates connected to this pin are pulled to V_{DD}.

5 IIC pins SDA and SCL can be repositioned using IICPS in SOPT2. Default reset locations are PTD0 and PTD1.

6 If ADC, HSCMP, or PGA is enabling a shared analog input pin, each has access to the pin.

2 Electrical Characteristics

2.1 Introduction

This section contains electrical and timing specifications for the MC9S08MP16 Series of microcontrollers available at the time of publication.

2.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters that are guaranteed during production testing on each individual device.
C	Those parameters that are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters that are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters that are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

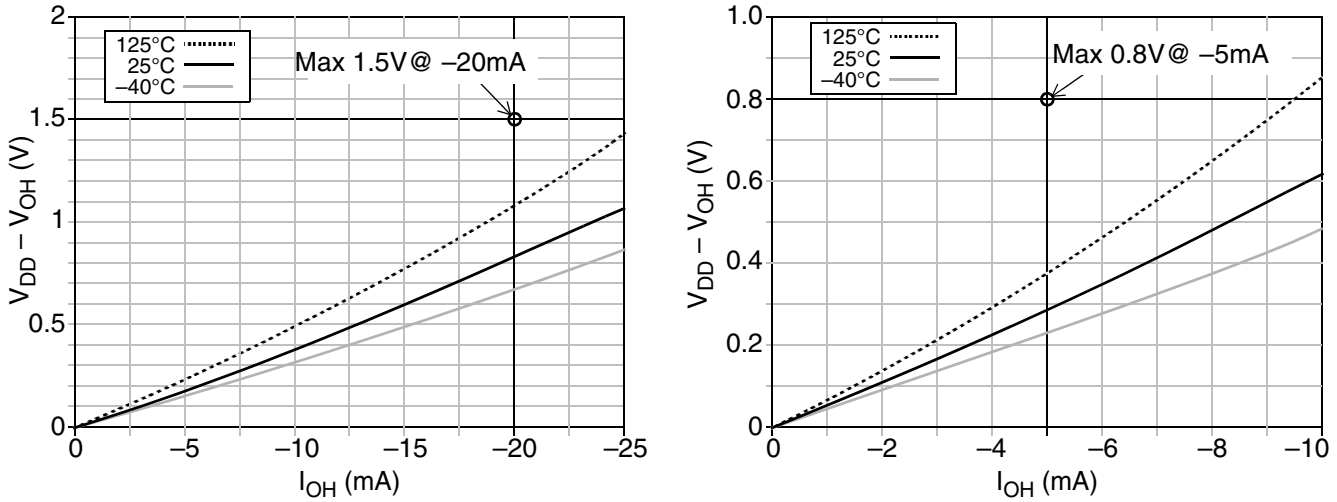
Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTF1/$\overline{\text{RESET}}$ are internally clamped to V_{SS} and V_{DD}.

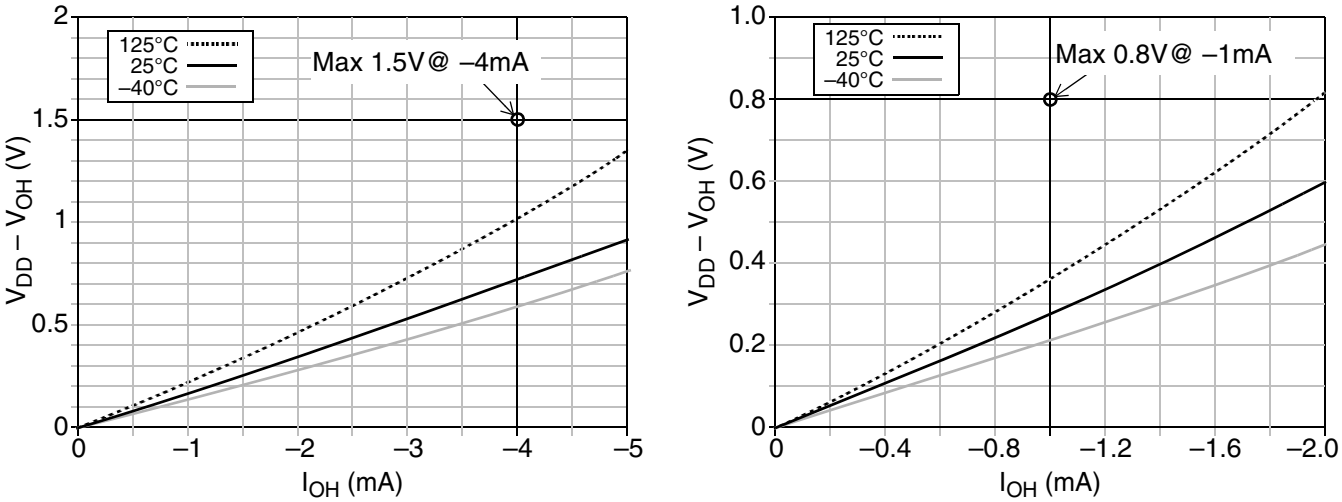
3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).



a) V_{DD} = 5V, High Drive

b) V_{DD} = 3V, High Drive

Figure 7. Typical $V_{DD} – V_{OH}$ vs I_{OH}, High Drive Strength



a) V_{DD} = 5V, Low Drive

b) V_{DD} = 3V, Low Drive

Figure 8. Typical $V_{DD} – V_{OH}$ vs I_{OH}, Low Drive Strength

2.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max[2]	Unit
1	C	Run supply current[3] measured at (CPU clock = 4 MHz, f_{Bus} = 2 MHz)	RI_{DD}	5	2.16	3	mA
	C			3	1.8	2.5	
2	P	Run supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	5	5.26	7.5	mA
	C			3	4.92	7	

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max[2]	Unit
3	C	Run supply current[4] measured at (CPU clock = 32 MHz, f_{Bus} = 16 MHz)	RI_{DD}	5	9.4	10	mA
	C			3	9	10	
4	P	Run supply current[5] measured at (CPU clock = 51.34 MHz, f_{Bus} = 25.67 MHz)	RI_{DD}	5	14.3	30	mA
	C			3	13.9	20	
5	P	Run supply current measured at (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	RI_{DD}	5	16	30	mA
	—			3	—	—	
6	C	Wait mode supply current measured at (CPU clock = 8 MHz, f_{Bus} = 4 MHz) (FEI mode, all modules off)	WI_{DD}	5	2.7	—	mA
7		Stop3 mode supply current					
	C	–40°C	$S3I_{DD}$	5	0.96	—	µA
	P	25°C			1.3	—	
	C	85°C			7.5	25	
	P[6]	105°C			37	90	
	P	125°C			65	150	
	C	–40°C		3	0.85	—	µA
	P	25°C			1.2	—	
	C	85°C			6.5	20	
	P[6]	105°C			32.7	80	
	P	125°C			58	130	
8		Stop2 mode supply current					
	C	–40°C	$S2I_{DD}$	5	0.94	—	µA
	P	25°C			1.25	—	
	C	85°C			7	25	
	P[6]	105°C			30	65	
	P	125°C			64	120	
	C	–40°C		3	0.83	—	µA
	P	25°C			1.1	—	
	C	85°C			6.3	20	
	P[6]	105°C			25	55	
	P	125°C			57	100	
9	C	RTC adder to stop2 or stop3[7]	$S23I_{DDRTC}$	5	300	500	nA
				3	300	500	nA

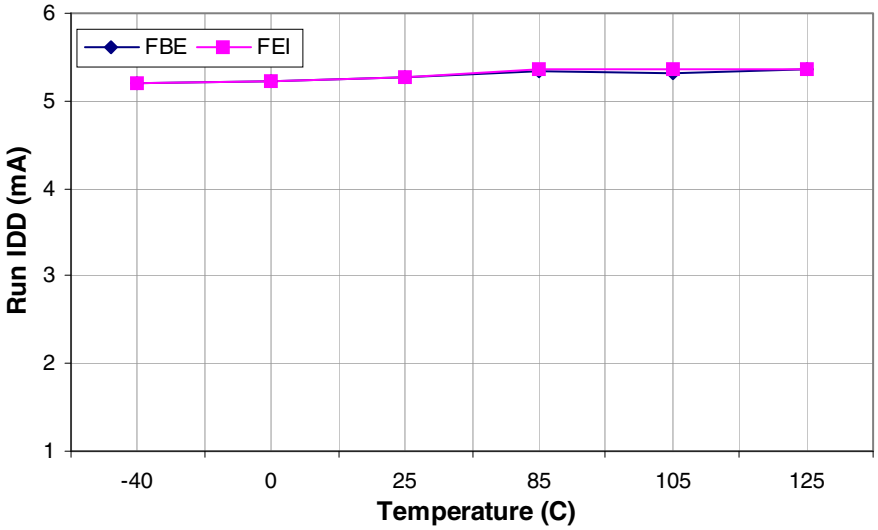


Figure 10. Typical Run I_{DD} vs. Temperature (V_{DD} = 5V, f_{bus} = 8MHz)

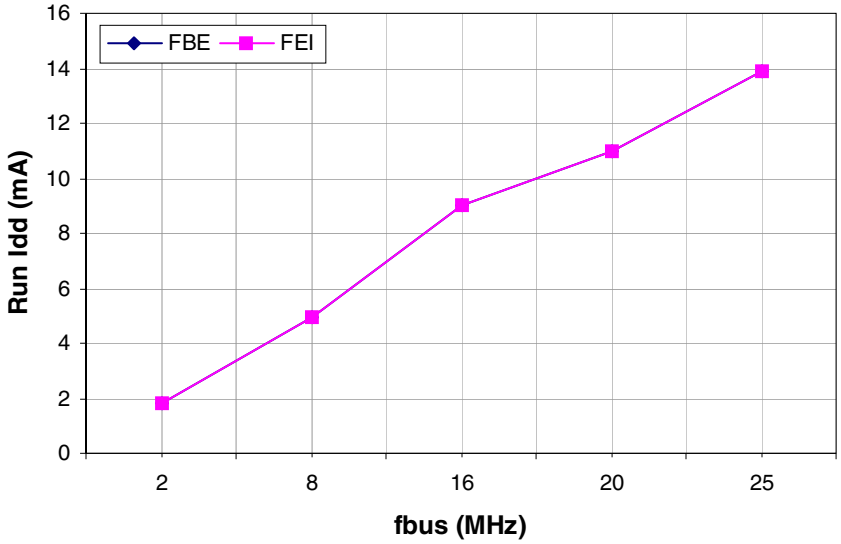


Figure 11. Typical Run I_{DD} vs. Bus Frequency (V_{DD} = 3V)

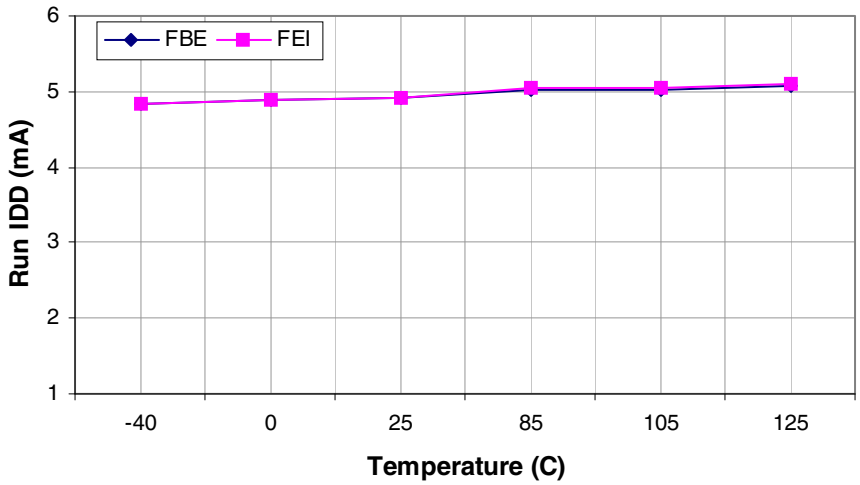


Figure 12. Typical Run I_{DD} vs. Temperature (V_{DD} = 3V, f_{bus} = 8MHz)

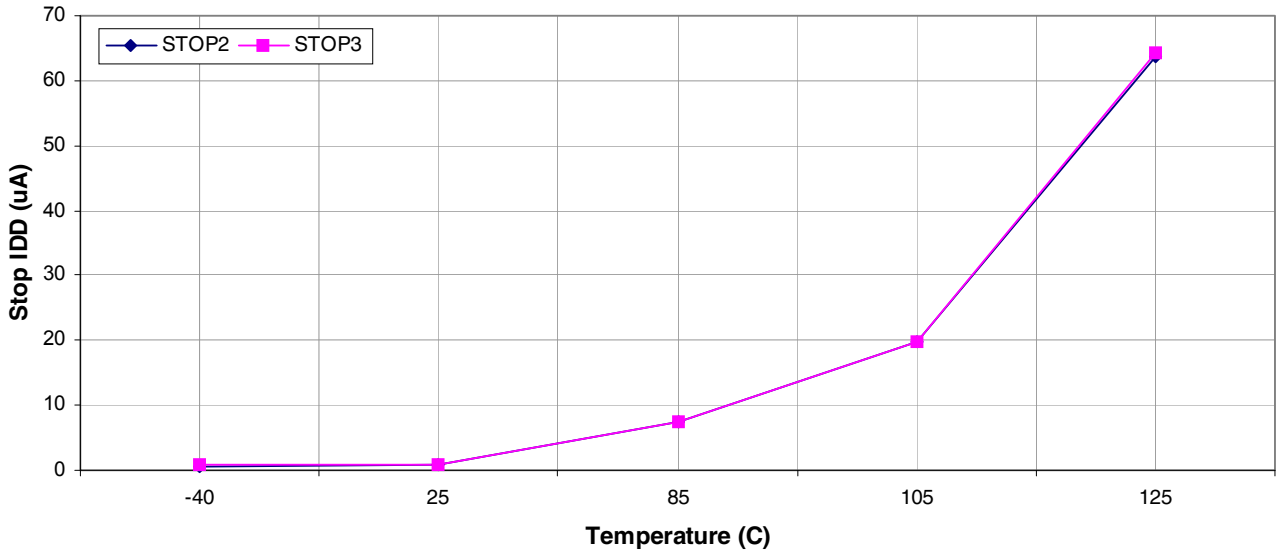


Figure 13. Typical Stop I_{DD} vs. Temperature (V_{DD} = 5V)

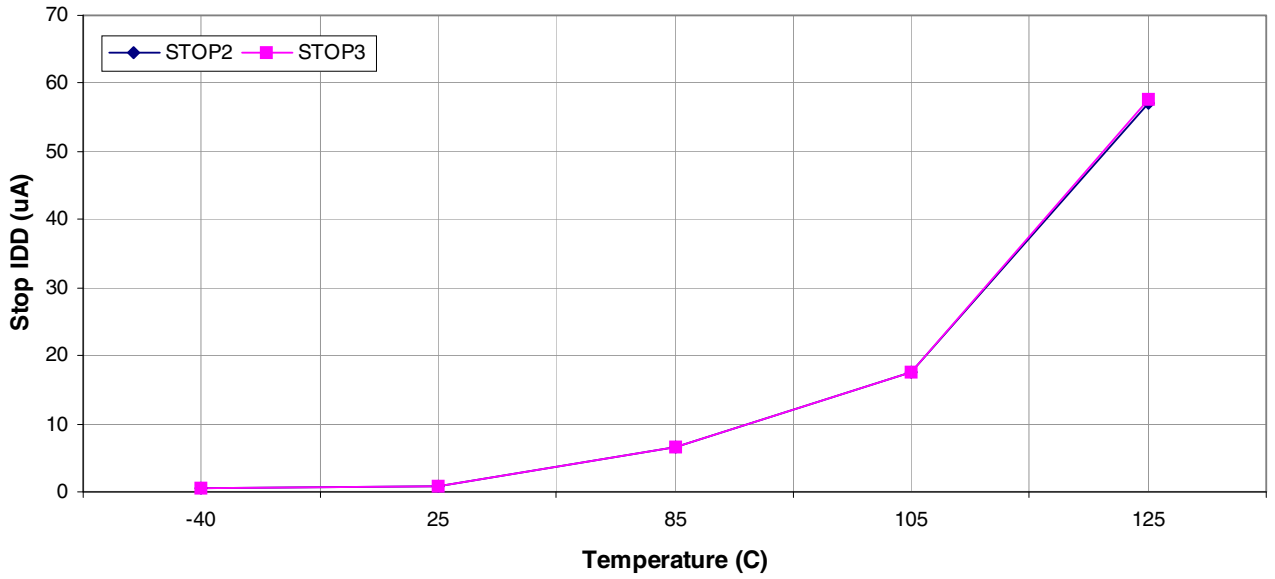


Figure 14. Typical Stop I_{DD} vs. Temperature (V_{DD} = 3V)

2.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1) FEE[2] or FBE[3] mode	f_{hi}	1	—	16	MHz
		High range (RANGE = 1, HGO = 1) FBELP mode	f_{hi-hgo}	1	—	16	MHz
		High range (RANGE = 1, HGO = 0) FBELP mode	f_{hi-lp}	1	—	8	MHz
2	—	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor					
		Low range (32 kHz to 100 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)		—	1	—	
4	—	Series resistor					
		Low range, low gain (RANGE = 0, HGO = 0)	R_S	—	0	—	kΩ
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	
		High range, low gain (RANGE = 1, HGO = 0)		—	0	—	
		High range, high gain (RANGE = 1, HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	

Table 10. ICS Frequency Specifications (continued)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
4	P	DCO output frequency range — trimmed [2]	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz
	C		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency [2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	± 0.8	± 2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C		Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
10	C	FLL acquisition time [3]		$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [4]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

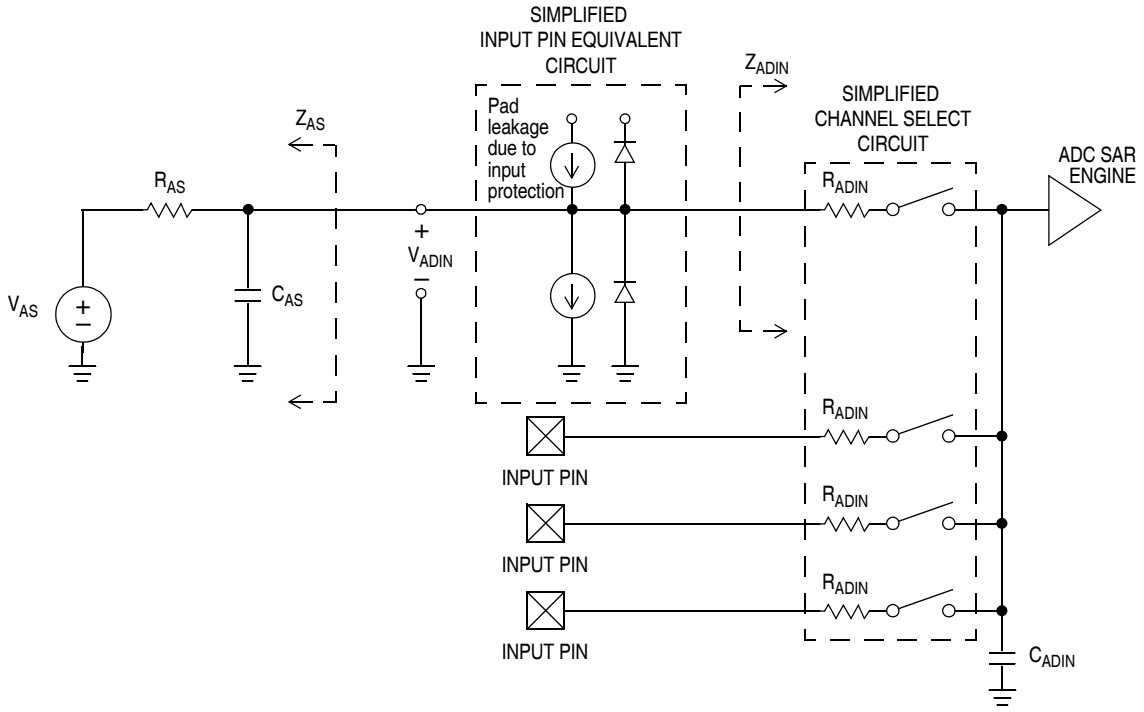


Figure 16. ADC Input Impedance Equivalency Diagram

Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC=1 ADLSMP=1 ADCO=1		I_{DDA}	—	133	—	μA	
T	Supply Current ADLPC=1 ADLSMP=0 ADCO=1		I_{DDA}	—	218	—	μA	
T	Supply Current ADLPC=0 ADLSMP=1 ADCO=1		I_{DDA}	—	327	—	μA	
T	Supply Current ADLPC=0 ADLSMP=0 ADCO=1		I_{DDA}	—	0.582	—	mA	
P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low Power (ADLPC=1)		1.25	2	3.3		

2.11 Digital to Analog (DAC) Characteristics

- The accuracy at worst case: +/- 1.5% maximum
- The settling time must be less than 100 ns
- When changing the output voltage level, the voltage glitch cannot be completely eliminated

Table 13. 5-bit DAC Characteristics

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
2	D	Supply current adder (enabled)	I_{DDAC}	—	—	20	μA
3	D	DAC reference inputs	Vin	V_{SSA}	—	V_{DDA}	V
5	D	DAC step size	V_{step}	$0.75 \times V_{in}/32$	$V_{in}/32$	$1.25 \times V_{in}/32$	V
6	D	DAC voltage range	V_{dacout}	$V_{in}/32$	—	V_{in}	V

2.12 High Speed Comparator (HSCMP) Characteristics

Table 14. High Speed Comparator Electrical Specifications

Num	C	Characteristic[1]	Symbol	Min	Typical	Max	Unit
1	D	Supply current, High Speed Mode (EN=1, PMODE=1)	I_{DDAHS}	—	200		μA
2	D	Supply current, Low Speed Mode (EN=1, PMODE=0)	I_{DDALS}	—	10		μA
3	—	Analog input voltage	V_{AIN}	V_{SSA}	—	V_{DDA}	V
4	P	Analog input offset voltage	V_{AIO}	—	5	40	mV
5	C	Analog Comparator hysteresis	V_H	3.0	9	20.0	mV
6	T	Propagation Delay, High Speed Mode (EN=1, PMODE=1)	t_{DHS}[2]	—	70	120	ns
7	T	Propagation Delay, Low Speed Mode (EN=1, PMODE=0)	t_{DLS}[2]	—	400	600	ns
8	D	Analog comparator initialization delay	t_{AINIT}	—	400	—	ns

1 All timing assumes slew rate control disabled and high drive strength enabled.

2 Delay from analog input to the CMPxOUT output pin. Measured with an input waveform that switches 30 mV above and below the reference.

2.13 Programmable Gain Amplifier (PGA) Characteristics

Table 15. Programmable Gain Amplifier Electrical Specifications

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	T	Supply current adder • normal mode (LP=0) • low power mode (LP=1)	I_{DDON}	 — —	 450 250	 550 300	uA
2	T	Supply current adder (stand-by)	I_{DDAOFF}	—	1	10	nA
3	T	Absolute analog input level	V_{IL}	V_{SSA}	$V_{DDA}/2$	V_{DDA}	V

Table 16. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
7	D	Keyboard interrupt pulse width Asynchronous path[4] Synchronous path[5]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 40 75	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 11 35	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to be recognized as a keyboard interrupt request in stop mode.

5 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

6 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 125°C.

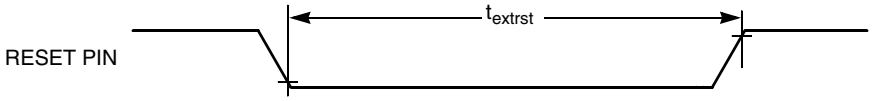


Figure 17. Reset Timing

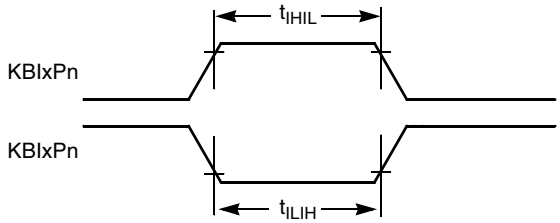


Figure 18. KBIxPn Timing

2.14.2 FTM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the FTM timer counter. These synchronizers operate from the current ICSOUT clock. The ICSOUT clock period = 0.5 × t_{cyc} = 1/(f_{Bus} × 2).

Table 17. FTM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	f_{ICSOUT}/4[1]	Hz
2	D	External clock period	t_{TCLK}	2	—	t_{cyc}
3	D	External clock high time	t_{clkh}	0.75	—	t_{cyc}

2.14.4 SPI

Table 19 and Figure 22 through Figure 25 describe the timing requirements for the SPI system.

Table 19. SPI Electrical Characteristics

Num[1]	C	Rating[2]	Symbol	Min	Max	Unit
1	D	Cycle time Master Slave	 t_{SCK} t_{SCK}	 2 4	 4096 —	 t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	 t_{Lead} t_{Lead}	 — 1/2	 1/2 —	 t_{SCK} t_{SCK}
3	D	Enable lag time Master Slave	 t_{Lag} t_{Lag}	 — 1/2	 1/2 —	 t_{SCK} t_{SCK}
4	D	Clock (SPSCK) high time Master and Slave	t_{SCKH}	1/2 t_{SCK} – 25	—	ns
5	D	Clock (SPSCK) low time Master and Slave	t_{SCKL}	1/2 t_{SCK} – 25	—	ns
6	D	Data setup time (inputs) Master Slave	 $t_{SI(M)}$ $t_{SI(S)}$	 30 30	 — —	 ns ns
7	D	Data hold time (inputs) Master Slave	 $t_{HI(M)}$ $t_{HI(S)}$	 30 30	 — —	 ns ns
8	D	Access time, slave[3]	t_A	0	40	ns
9	D	Disable time, slave[4]	t_{dis}	—	40	ns
10	D	Data setup time (outputs) Master Slave	 t_{SO} t_{SO}	 — —	 25 25	 ns ns
11	D	Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 –10 –10	 — —	 ns ns
12	D	Operating frequency Master (SPIFE=0) Slave (SPIFE=0) Master (SPIFE=1) Slave (SPIFE=1)	f_{op}	f_{Bus}/4096 dc f_{Bus}/4096 dc	8[5] f_{Bus}/4 5[6] 5[6]	MHz MHz MHz

1 Refer to Figure 22 through Figure 25.

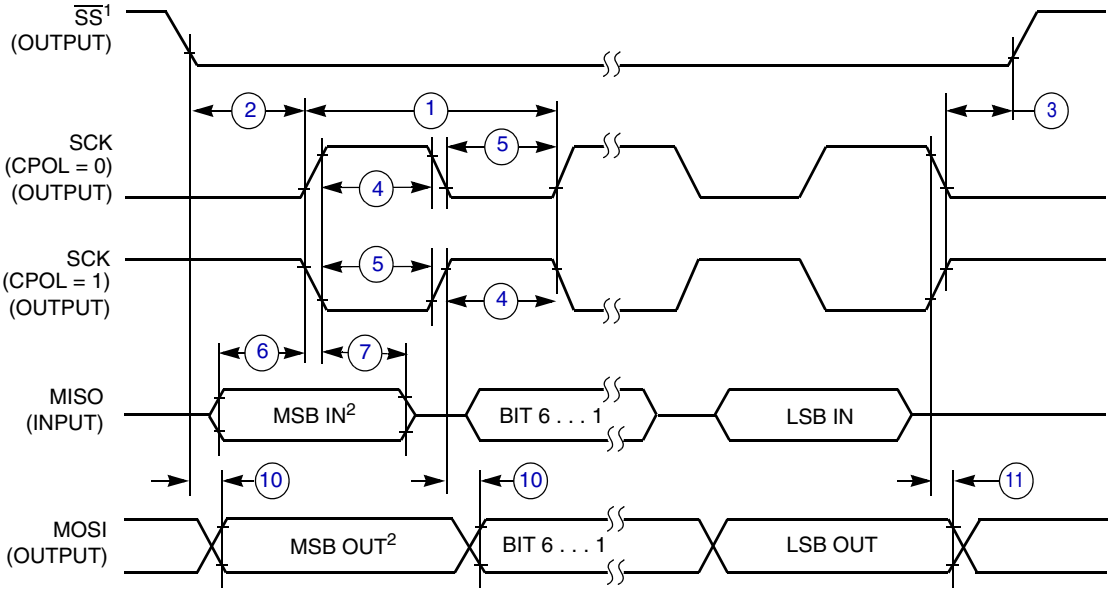
2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.

4 Hold time to high-impedance state.

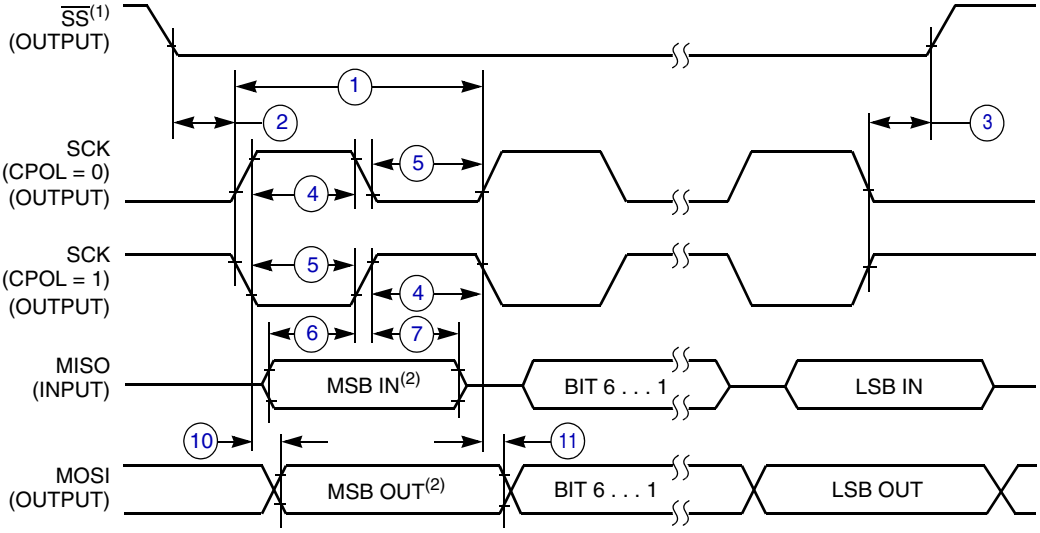
5 Maximum baud rate must be limited to 8 MHz.

6 Maximum baud rate must be limited to 5 MHz due to input filter characteristics.



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 23. SPI Master Timing (CPHA = 1)

2.15 Flash Memory Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 20. Flash Memory Characteristics

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage for program/erase -40°C to 125°C	$V_{prog/erase}$	2.7		5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7		5.5	V
3	—	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
5	C	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	D	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
8	D	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Byte program current[3]	R_{IDDBP}	—	4	—	mA
10	C	Page erase current[3]	R_{IDDPE}	—	6	—	mA
11	C	Program/erase endurance[4] T_L to T_H = –40°C to + 125°C T = 25°C		10,000	— 100,000	— —	cycles
12	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 5.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for Flash** is based upon the intrinsic bit cell performance. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

2.16 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.16.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a

custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 21. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5V TA = +25°C package type 48 LQFP	0.15 – 50 MHz	4 MHz crystal 2 MHz bus	3	dBμV
			50 – 150 MHz		8	
			150 – 500 MHz		–4	
			500 – 1000 MHz		–8	
			IEC Level[2]		N	—
			SAE Level[3]		1	—

1 Data based on qualification test results. The reported emission level is the value of the maximum emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2 IEC level maximums: N ≤ 12 dBμV, L ≤ 24 dBμV, I ≤ 36 dBμV

3 SAE level maximums: 1 ≤ 10 dBμV, 2 ≤ 20 dBμV, 3 ≤ 30 dBμV, 4 ≤ 40 dBμV

3 Ordering Information

This section contains ordering information for MC9S08MP16 and MC9S08MP12 devices.

Table 22. Device and Package Options

Device Number[1]	Temp Range	Memory		Available Packages[2]		
		Flash	RAM	48-Pin	32-Pin	28-Pin
Consumer and Industrial Qualification						
MC9S08MP16	V	16K	1024	48 LQFP	32 LQFP	28 SOIC
MC9S08MP12	V	12K	512	—	—	28 SOIC
Automotive Qualification						
S9S08MP16	C, V, M	16K	1024	48 LQFP	—	—

1 See the *MC9S08MP16RM Reference Manual* (MC9S08MP16RM) for a complete description of modules included on each device.

2 See Table 23 for package information.

Table 24 summarizes changes contained in this document.

Table 24. Revision History

Rev	Date	Description of Changes
1	10/15/2009	Initial public revision
2	08/09/2011	Updated Table 10. Changed the value of row 8 column “C” from to C to P.

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Document Number: MC9S08MP16
Rev. 2
08/2011

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