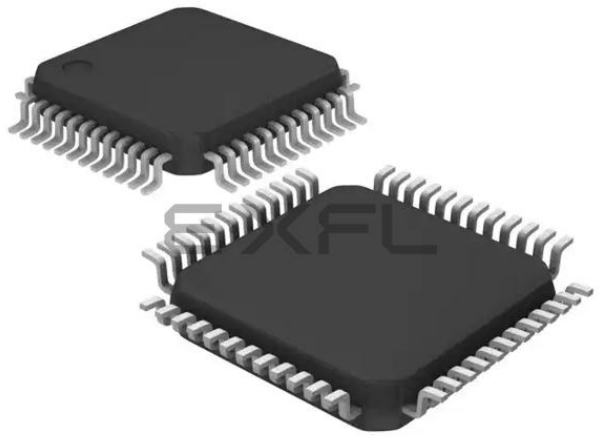

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Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	51.34MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 13x12b; D/A 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08mp16vlf

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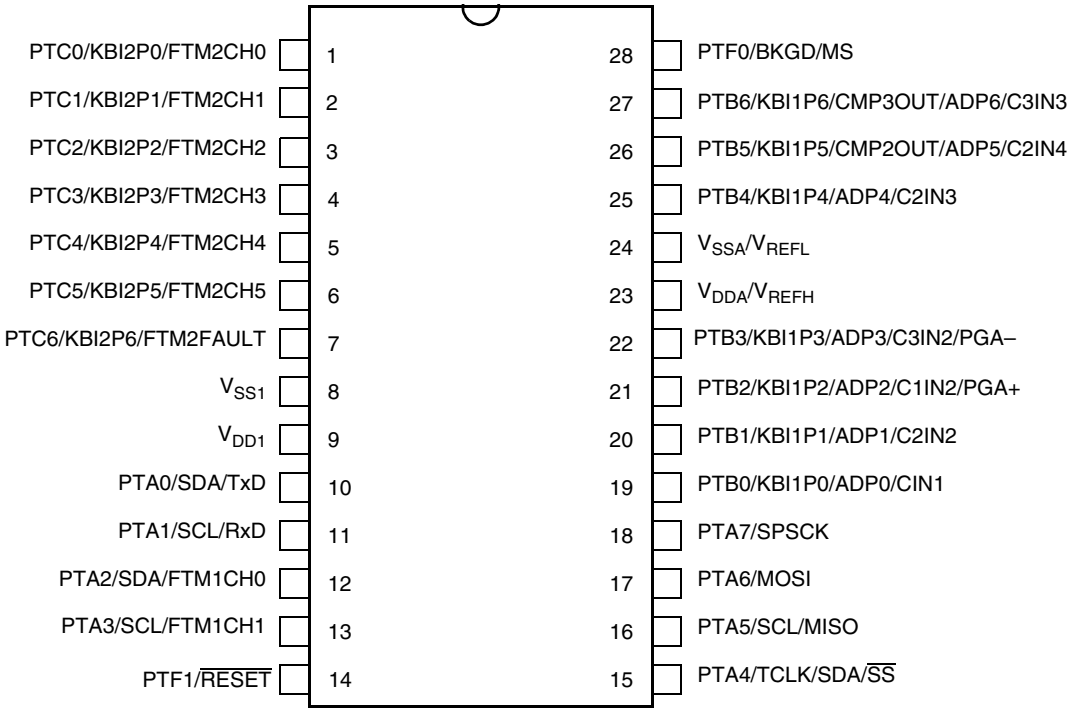


Figure 4. MC9S08MP16 Series in 28-Pin SOIC Package

Table 1. Pin Availability by Package Pin-Count

Pin Number			<-- Lowest Priority --> Highest				
48	32 LQFP	28	Port Pin	Alt 1	Alt 2	Alt3	Alt4
1	3	5	PTC4	KBI2P4	FTM2CH4		
2	4	6	PTC5	KBI2P5	FTM2CH5		
3	5	7	PTC6	KBI2P6	FTM2FAULT		
4	—	—	PTC7	KBI2P7	TCLK[1]		
5	—	—	PTD0	KBI3P0	SDA[5]		
6	—	—	PTD1	KBI3P1	SCL[5]		
7	—	—	PTD2	KBI3P2	PDB1OUT		
8	—	—	PTD3	KBI3P3	FTM1FAULT		
9	6	8					V_{SS1}
10	7	9					V_{DD1}
11	8	10	PTA0	SDA[5]	TxD		
12	9	11	PTA1	SCL[5]	RxD		
13	10	12	PTA2	SDA[5]	FTM1CH0		
14	11	13	PTA3	SCL[5]	FTM1CH1		
15	—	—	PTD4	KBI3P4	PDB2OUT		
16	—	—	PTD5	KBI3P5	CMP1OUT		
17	—	—	PTD6	KBI3P6	CMP2OUT[2]		
18	—	—	PTD7	KBI3P7	CMP3OUT[3]		
19	12	14	PTF1	$\overline{\text{RESET}}$[4]			
20	—	—	PTF2				
21	13	15	PTA4	TCLK[1]	SDA[5]	$\overline{SS}$	
22	14	16	PTA5		SCL[5]	MISO	
23	15	17	PTA6			MOSI	
24	16	18	PTA7			SPSCK	
25	—	—	PTE0		ADP8		
26	—	—	PTE1		ADP9		
27	—	—	PTE2		ADP10		
28	17	19	PTB0	KBI1P0	ADP0[6]	CIN1[6]	
29	18	20	PTB1	KBI1P1	ADP1[6]	C2IN2[6]	
30	19	21	PTB2	KBI1P2	ADP2[6]	C1IN2[6]	PGA+[6]
31	20	22	PTB3	KBI1P3	ADP3[6]	C3IN2[6]	PGA–[6]
32	21	23					V_{DDA}/V_{REFH}
33	22	24					V_{SSA}/V_{REFL}
34	—	—	PTE3		ADP11[6]	C1IN3[6]	

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number			<-- Lowest **Priority** --> Highest				
48	**32 LQFP**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
35	—	—	PTE4		ADP12[6]	C1IN4[6]	
36	23	25	PTB4	KBI1P4		ADP4[6]	C2IN3[6]
37	24	26	PTB5	KBI1P5	CMP2OUT[2]	ADP5[6]	C2IN4[6]
38	25	27	PTB6	KBI1P6	CMP3OUT[3]	ADP6[6]	C3IN3[6]
39	26	—	PTB7	KBI1P7		ADP7[6]	C3IN4[6]
40	27	—	PTE5	XTAL			
41	28	—	PTE6	EXTAL			
42	29	—					V_{SS2}
43	—	—					V_{DD2}
44	30	28	PTF0	BKGD	MS		
45	31	1	PTC0	KBI2P0	FTM2CH0		
46	32	2	PTC1	KBI2P1	FTM2CH1		
47	1	3	PTC2	KBI2P2	FTM2CH2		
48	2	4	PTC3	KBI2P3	FTM2CH3		

1 TCLK pin can be repositioned using TCLKPS in SOPT2. Default reset location is PTC7.

2 HSCMP2 output CMP2OUT can be repositioned using the CMP2OPS in the SOPT2 register. Default reset location is PTD6.

3 HSCMP3 output CMP3OUT can be repositioned using the CMP3OPS in the SOPT2 register. Default reset location is PTD7.

4 Pin is open drain with an internal pullup that is always enabled. Pin does not contain a clamp diode to V_{DD} and should not be driven above V_{DD}. The voltage measured on the internally pulled up $\overline{\text{RESET}}$ will not be pulled to V_{DD}. The internal gates connected to this pin are pulled to V_{DD}.

5 IIC pins SDA and SCL can be repositioned using IICPS in SOPT2. Default reset locations are PTD0 and PTD1.

6 If ADC, HSCMP, or PGA is enabling a shared analog input pin, each has access to the pin.

2 Electrical Characteristics

2.1 Introduction

This section contains electrical and timing specifications for the MC9S08MP16 Series of microcontrollers available at the time of publication.

2.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters that are guaranteed during production testing on each individual device.
C	Those parameters that are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters that are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters that are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTF1/$\overline{\text{RESET}}$ are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		– 2.5	V
	Maximum input voltage limit		7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Charge device model (CDM)	V_{CDM}	± 500	—	V
3	Latch-up current at T_A = 125°C	I_{LAT}	± 100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1	—	Operating Voltage	V_{DD}		2.7	—	5.5	V
2	—	Analog Supply voltage delta to V_{DD} (V_{DD} – V_{DDA})[(2)]	ΔV_{DDA}		—	0	±100	mV
3	—	Analog Ground voltage delta to V_{SS} (V_{SS} – V_{SSA})[(2)]	ΔV_{SSA}		—	0	±100	mV

Table 7. DC Characteristics (continued)

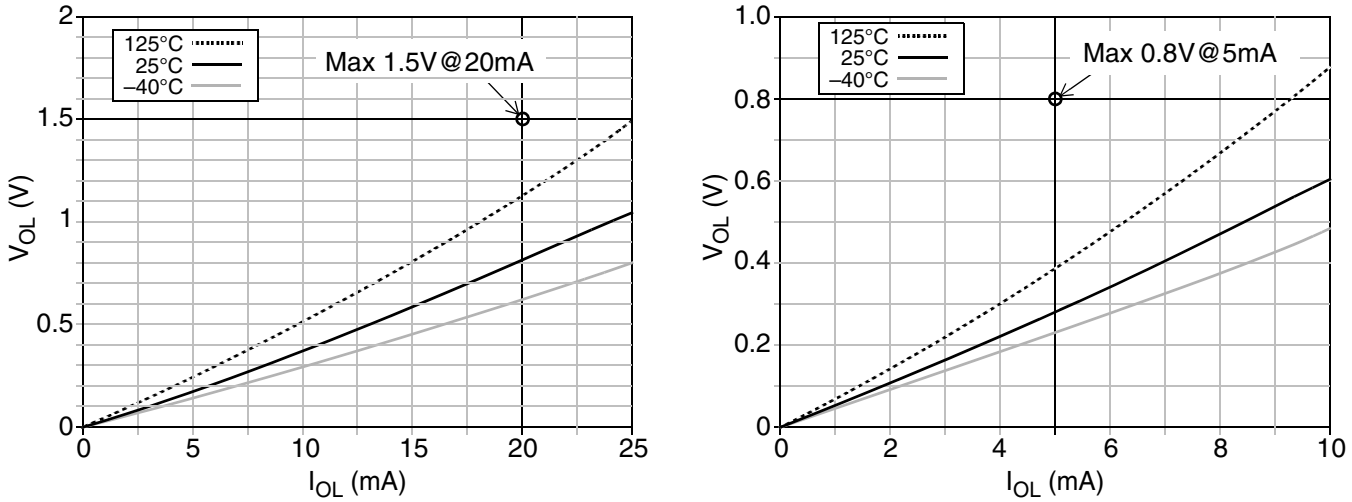
Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
4	C	All I/O pins (except PTF1/$\overline{\text{RESET}}$)	V_{OH}	5 V, I_{Load} = –4 mA	V_{DD} – 1.5	—	—	V
	P	low-drive strength		5 V, I_{Load} = –2 mA	V_{DD} – 0.8	—	—	
	C	Output high		3 V, I_{Load} = –1 mA	V_{DD} – 0.8	—	—	
	C	voltage		5 V, I_{Load} = –20 mA	V_{DD} – 1.5	—	—	
	P	high-drive strength		5 V, I_{Load} = –10 mA	V_{DD} – 0.8	—	—	
	C			3 V, I_{Load} = –5 mA	V_{DD} – 0.8	—	—	
5	D	Output high current — Max total I_{OH} for all ports	I_{OHT}	$V_{OUT} < V_{DD}$	0	—	–100	mA
6	C	All I/O pins	V_{OL}	5 V, I_{Load} = 4 mA	—	—	1.5	V
	P	(except PTF1/$\overline{\text{RESET}}$)		5 V, I_{Load} = 2 mA	—	—	0.8	
	C	low-drive strength		3 V, I_{Load} = 1 mA	—	—	0.8	
	C	All I/O pins		5 V, I_{Load} = 20 mA	—	—	1.5	
	P	Output low (Except PTF1/$\overline{\text{RESET}}$)		5 V, I_{Load} = 10 mA	—	—	0.8	
	C	voltage high-drive strength		3 V, I_{Load} = 5 mA	—	—	0.8	
7	C	PTF1/$\overline{\text{RESET}}$		5 V, I_{Load} = 3.2 mA	—	—	1.5	
8	P			5 V, I_{Load} = 1.6 mA	—	—	0.8	
9	C			3 V, I_{Load} = 0.8 mA	—	—	0.8	
10	D	Output low current — Max total I_{OL} for all ports	I_{OLT}	$V_{OUT} > V_{SS}$	0	—	100	mA
11	P	Input high voltage; all digital inputs	V_{IH}	5V	0.65 x V_{DD}	—	—	V
	C			3V	0.7 x V_{DD}	—	—	
12	P	Input low voltage; all digital inputs	V_{IL}	5V	—	—	0.35 x V_{DD}	V
	C			3V	—	—	0.35 x V_{DD}	
13	C	Input hysteresis	V_{hys}		0.06 x V_{DD}			V
14	P	Input leakage current (per pin)	$\lvert I_{In} \rvert$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	µA
15	P	Hi-Z (off-state) leakage current (per pin)						
		input/output port pins	$\lvert I_{OZ} \rvert$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	µA
		PTF1/$\overline{\text{RESET}}$, PTE5/XTAL pins		$V_{In} = V_{DD}$ or V_{SS}	—	—	2	µA
16	P	Pullup or Pulldown[3] resistors; when enabled — I/O pins	R_{PU},R_{PD}		17	37	52	kΩ
	C	PTF1/$\overline{\text{RESET}}$[4]	R_{PU}		17	37	52	kΩ
17	D	DC injection current [5, 6, 7, 8] — Single pin limit	I_{IC}	$V_{IN} > V_{DD}$	0	—	2	mA
				$V_{IN} < V_{SS}$	0	—	–0.2	mA
		Total MCU limit, includes sum of all stressed pins		$V_{IN} > V_{DD}$	0	—	25	mA
				$V_{IN} < V_{SS}$	0	—	–5	mA

7 All functional non-supply pins except PTF1/$\overline{\text{RESET}}$ are internally clamped to V_{SS} and V_{DD}.

8 The PTF1/$\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

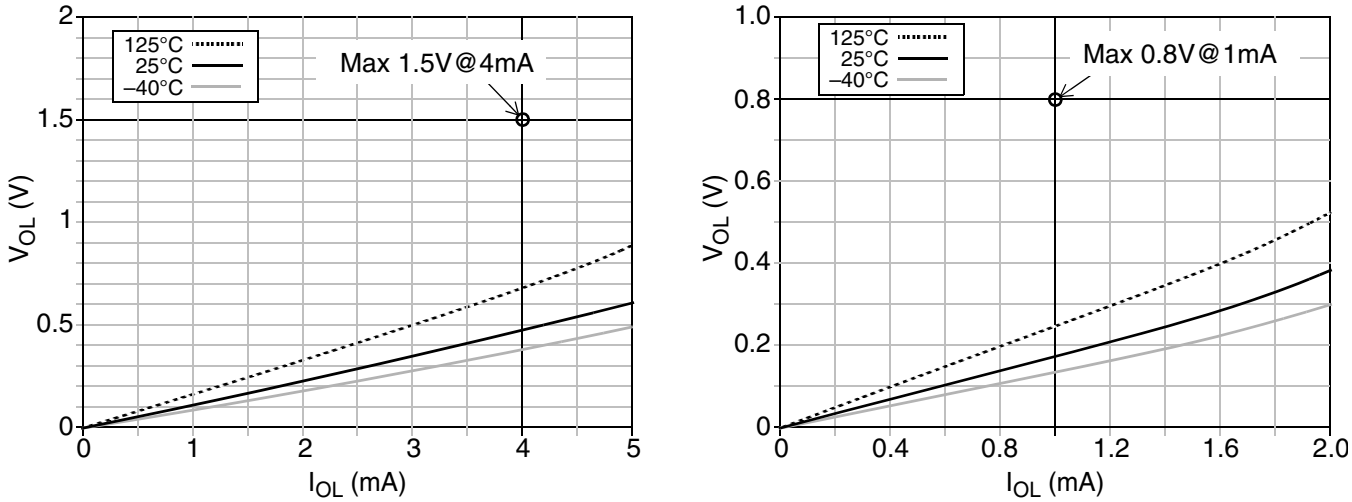
9 Maximum is highest voltage that POR is guaranteed.

10 Factory trimmed at V_{DD} = 5.0 V



a) V_{DD} = 5V, High Drive **b) V_{DD} = 3V, High Drive**

Figure 5. Typical V_{OL} vs I_{OL}, High Drive Strength (except PTF1/RESET)



a) V_{DD} = 5V, Low Drive **b) V_{DD} = 3V, Low Drive**

Figure 6. Typical V_{OL} vs I_{OL}, Low Drive Strength (except PTF1/RESET)

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max[2]	Unit
10	C	LVD adder to stop3 (LVDE = LVDSE = 1)	$S3I_{DDLVD}$	5	110	180	µA
				3	90	160	µA
11	C	Adder to stop3 for oscillator enabled[8] (EREFSTEN =1)	$S3I_{DDOSC}$	5,3	5	8	µA

1 Typical values are based on characterization data at 25°C. See Figure 9 through Figure 14 for typical curves across temperature and voltage.

2 Max values in this column apply for the full operating temperature range of the device unless otherwise noted.

3 All modules except ADC active, ICS configured for FBELP, and does not include any dc loads on port pins

4 All modules except ADC active, ICS configured for FEI, and does not include any dc loads on port pins

5 All modules except ADC active, ICS configured for FEI, and does not include any dc loads on port pins

6 Stop currents are tested in production for 25°C on all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and is approved.

7 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

8 Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal and low power mode (HGO = 0).

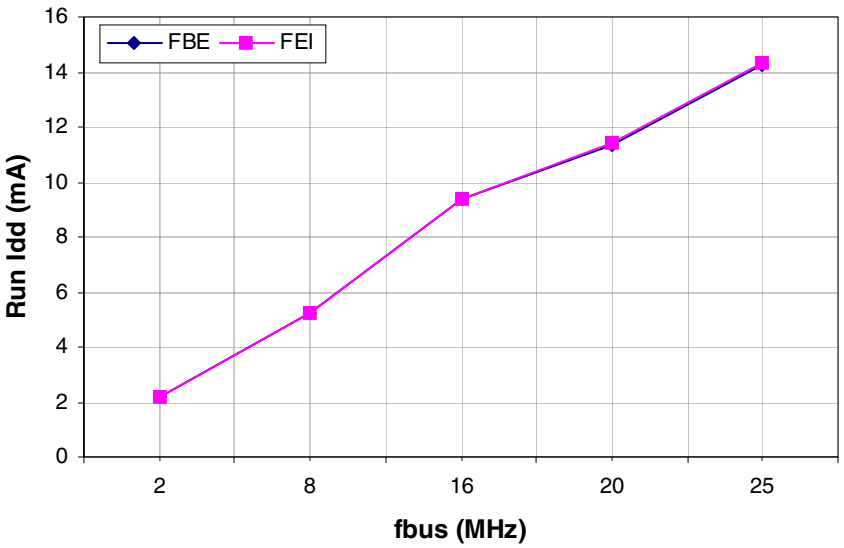


Figure 9. Typical Run I_{DD} vs. Bus Frequency (V_{DD} = 5V)

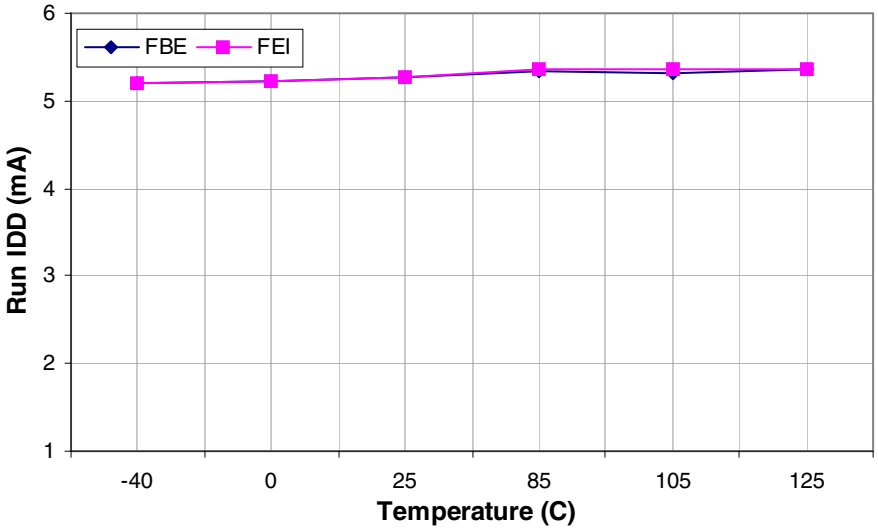


Figure 10. Typical Run I_{DD} vs. Temperature (V_{DD} = 5V, f_{bus} = 8MHz)

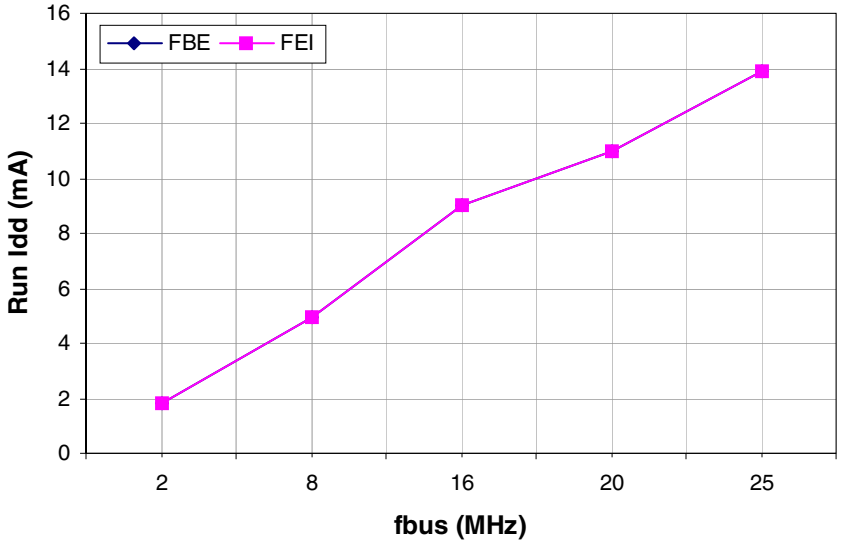


Figure 11. Typical Run I_{DD} vs. Bus Frequency (V_{DD} = 3V)

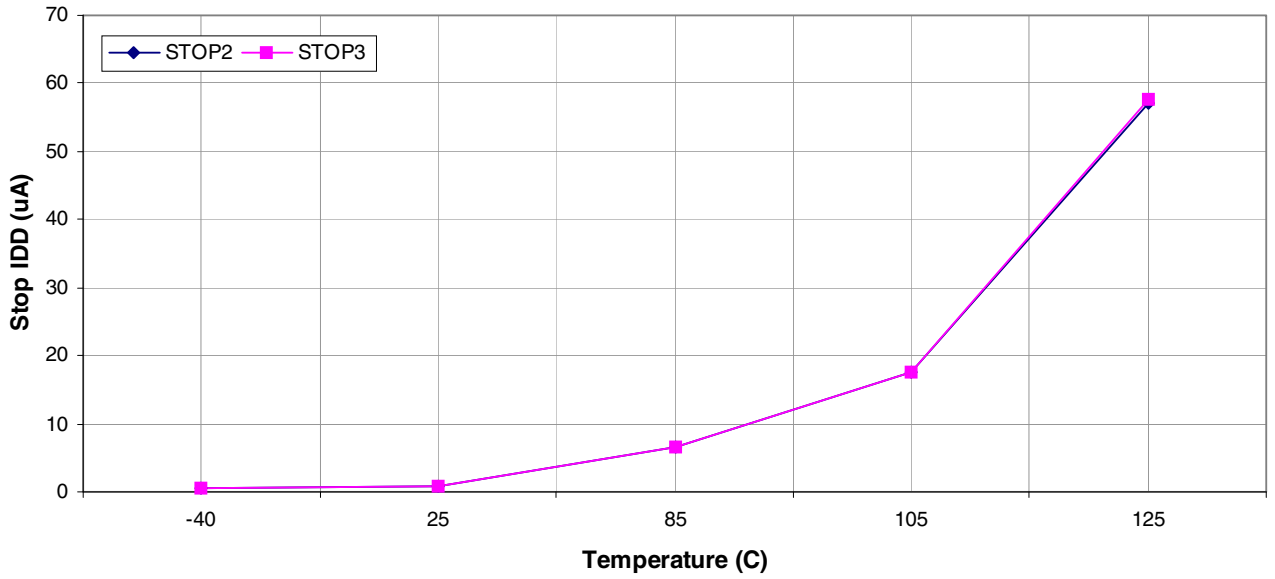


Figure 14. Typical Stop I_{DD} vs. Temperature (V_{DD} = 3V)

2.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1) FEE[2] or FBE[3] mode	f_{hi}	1	—	16	MHz
		High range (RANGE = 1, HGO = 1) FBELP mode	f_{hi-hgo}	1	—	16	MHz
		High range (RANGE = 1, HGO = 0) FBELP mode	f_{hi-lp}	1	—	8	MHz
2	—	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor					
		Low range (32 kHz to 100 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)		—	1	—	
4	—	Series resistor					
		Low range, low gain (RANGE = 0, HGO = 0)	R_S	—	0	—	kΩ
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	
		High range, low gain (RANGE = 1, HGO = 0)		—	0	—	
		High range, high gain (RANGE = 1, HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	

Table 9. Oscillator Electrical Specifications (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
5	T	Crystal start-up time [4] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[5] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 20	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode [2] FBE mode [3] FBELP mode	f_{extal}	 0.03125 0 0	 — — —	 51.34 51.34 51.34	 MHz MHz MHz

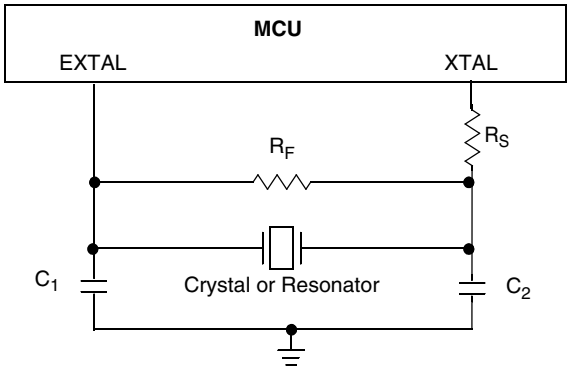
1 Typical data was characterized at 5.0 V, 25°C or is recommended value.

2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 The input clock source must be divided using RDIV to less than or equal to 39.0625 kHz.

4 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

5 4 MHz crystal



2.9 Internal Clock Source (ICS) Characteristics

Table 10. ICS Frequency Specifications

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1a	P	Average internal reference frequency — factory trimmed (consumer- and industrial-qualified devices) at V_{DD} = 5 V and temperature = 25°C	f_{int_t}	—	32.768	—	kHz
1b	P	Average internal reference frequency — factory trimmed (automotive-qualified devices) at V_{DD} = 5 V and temperature = 25°C	f_{int_t}	—	31.25	—	kHz
2	P	Internal reference frequency — user trimmed	f_{int_t}	31.25	—	39.06	kHz
3	T	Internal reference start-up time	t_{irefst}	—	60	100	µs

Table 10. ICS Frequency Specifications (continued)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
4	P	DCO output frequency range — trimmed [2]	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz
	C		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency [2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	± 0.8	± 2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C		Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
10	C	FLL acquisition time [3]		$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [4]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See ADC chapter in the Reference Manual for conversion time variances
		Long Sample (ADLSMP=1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP=1)		—	23.5	—		
T	Temp Sensor Slope	-40°C to 25°C	m	—	3.266	—	mV/°C	
		25°C to 125°C		—	3.638	—		
T	Temp Sensor Voltage	25°C	V_{TEMP25}	—	1.396	—	mV	
T	Total Unadjusted Error	12 bit mode	E_{TUE}	—	±3.0	±6.5	LSB[2]	Includes quantization
P		10 bit mode		—	±1	±2.5		
T		8 bit mode		—	±0.5	±1.0		
T	Differential Non-Linearity	12 bit mode	DNL	—	±1.75	±3.5	LSB[2]	
P		10 bit mode[3]		—	±0.5	±1.0		
T		8 bit mode[3]		—	±0.3	±0.5		
T	Integral Non-Linearity	12 bit mode	INL	—	±1.5	±4.5	LSB[2]	
P		10 bit mode		—	±0.5	±1.0		
T		8 bit mode		—	±0.3	±0.5		
T	Zero-Scale Error	12 bit mode	E_{ZS}	—	±1.5	0.0/ -3.0	LSB[2]	V_{ADIN} = V_{SSAD}
P		10 bit mode		—	±0.5	±1.5		
T		8 bit mode		—	±0.5	±0.5		
T	Full-Scale Error	12 bit mode	E_{FS}	—	±1.0	+1.75/ −1.25	LSB[2]	V_{ADIN} = V_{DDAD}
T		10 bit mode		—	±0.5	±1		
T		8 bit mode		—	±0.5	±0.5		
D	Quantization Error	12 bit mode	E_Q	—	-1 to 0	—	LSB[2]	
		10 bit mode		—	—	±0.5		
		8 bit mode		—	—	±0.5		
D	Input Leakage Error	12 bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
		10 bit mode		—	±0.2	±2.5		
		8 bit mode		—	±0.1	±1		

1 Typical values assume V_{DDAD} = 5.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.11 Digital to Analog (DAC) Characteristics

- The accuracy at worst case: +/- 1.5% maximum
- The settling time must be less than 100 ns
- When changing the output voltage level, the voltage glitch cannot be completely eliminated

Table 13. 5-bit DAC Characteristics

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
2	D	Supply current adder (enabled)	I_{DDAC}	—	—	20	μA
3	D	DAC reference inputs	Vin	V_{SSA}	—	V_{DDA}	V
5	D	DAC step size	V_{step}	$0.75 \times V_{in}/32$	$V_{in}/32$	$1.25 \times V_{in}/32$	V
6	D	DAC voltage range	V_{dacout}	$V_{in}/32$	—	V_{in}	V

2.12 High Speed Comparator (HSCMP) Characteristics

Table 14. High Speed Comparator Electrical Specifications

Num	C	Characteristic[1]	Symbol	Min	Typical	Max	Unit
1	D	Supply current, High Speed Mode (EN=1, PMODE=1)	I_{DDAHS}	—	200		μA
2	D	Supply current, Low Speed Mode (EN=1, PMODE=0)	I_{DDALS}	—	10		μA
3	—	Analog input voltage	V_{AIN}	V_{SSA}	—	V_{DDA}	V
4	P	Analog input offset voltage	V_{AIO}	—	5	40	mV
5	C	Analog Comparator hysteresis	V_H	3.0	9	20.0	mV
6	T	Propagation Delay, High Speed Mode (EN=1, PMODE=1)	t_{DHS}[2]	—	70	120	ns
7	T	Propagation Delay, Low Speed Mode (EN=1, PMODE=0)	t_{DLS}[2]	—	400	600	ns
8	D	Analog comparator initialization delay	t_{AINIT}	—	400	—	ns

1 All timing assumes slew rate control disabled and high drive strength enabled.

2 Delay from analog input to the CMPxOUT output pin. Measured with an input waveform that switches 30 mV above and below the reference.

2.13 Programmable Gain Amplifier (PGA) Characteristics

Table 15. Programmable Gain Amplifier Electrical Specifications

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	T	Supply current adder • normal mode (LP=0) • low power mode (LP=1)	I_{DDON}	 — —	 450 250	 550 300	uA
2	T	Supply current adder (stand-by)	I_{DDAOFF}	—	1	10	nA
3	T	Absolute analog input level	V_{IL}	V_{SSA}	$V_{DDA}/2$	V_{DDA}	V

Table 16. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
7	D	Keyboard interrupt pulse width Asynchronous path[4] Synchronous path[5]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 40 75	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 11 35	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to be recognized as a keyboard interrupt request in stop mode.

5 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

6 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 125°C.

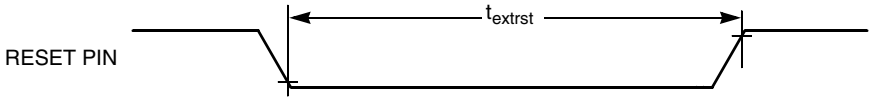


Figure 17. Reset Timing

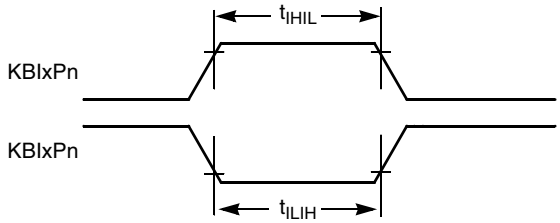


Figure 18. KBIxPn Timing

2.14.2 FTM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the FTM timer counter. These synchronizers operate from the current ICSOUT clock. The ICSOUT clock period = 0.5 × t_{cyc} = 1/(f_{Bus} × 2).

Table 17. FTM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	f_{ICSOUT}/4[1]	Hz
2	D	External clock period	t_{TCLK}	2	—	t_{cyc}
3	D	External clock high time	t_{clkh}	0.75	—	t_{cyc}

Table 17. FTM Input Timing (continued)

No.	C	Function	Symbol	Min	Max	Unit
4	D	External clock low time	t_{clkl}	0.75	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	0.75	—	t_{cyc}

1 The maximum external clock frequency is limited to 10MHz due to input filter characteristics.

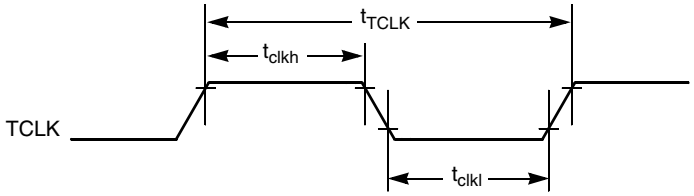


Figure 19. FTM External Clock

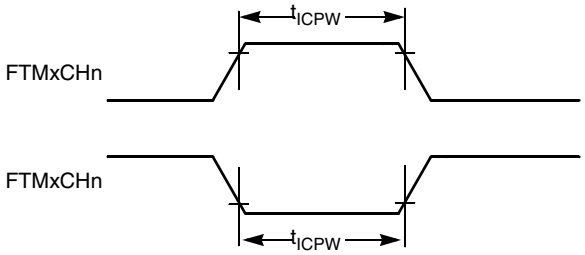


Figure 20. FTM Input Capture Pulse

2.14.3 MTIM Module Timing

Synchronizer circuits determine the fastest clock that can be used as the optional external clock source to the MTIM timer counter. These synchronizers operate from the current bus rate clock.

Table 18. MTIM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}

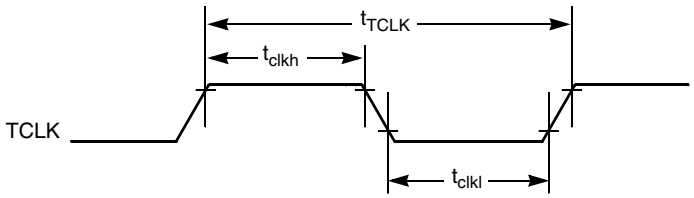


Figure 21. MTIM Timer External Clock

2.14.4 SPI

Table 19 and Figure 22 through Figure 25 describe the timing requirements for the SPI system.

Table 19. SPI Electrical Characteristics

Num[1]	C	Rating[2]	Symbol	Min	Max	Unit
1	D	Cycle time Master Slave	 t_{SCK} t_{SCK}	 2 4	 4096 —	 t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	 t_{Lead} t_{Lead}	 — 1/2	 1/2 —	 t_{SCK} t_{SCK}
3	D	Enable lag time Master Slave	 t_{Lag} t_{Lag}	 — 1/2	 1/2 —	 t_{SCK} t_{SCK}
4	D	Clock (SPSCK) high time Master and Slave	t_{SCKH}	1/2 t_{SCK} – 25	—	ns
5	D	Clock (SPSCK) low time Master and Slave	t_{SCKL}	1/2 t_{SCK} – 25	—	ns
6	D	Data setup time (inputs) Master Slave	 $t_{SI(M)}$ $t_{SI(S)}$	 30 30	 — —	 ns ns
7	D	Data hold time (inputs) Master Slave	 $t_{HI(M)}$ $t_{HI(S)}$	 30 30	 — —	 ns ns
8	D	Access time, slave[3]	t_A	0	40	ns
9	D	Disable time, slave[4]	t_{dis}	—	40	ns
10	D	Data setup time (outputs) Master Slave	 t_{SO} t_{SO}	 — —	 25 25	 ns ns
11	D	Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 –10 –10	 — —	 ns ns
12	D	Operating frequency Master (SPIFE=0) Slave (SPIFE=0) Master (SPIFE=1) Slave (SPIFE=1)	f_{op}	f_{Bus}/4096 dc f_{Bus}/4096 dc	8[5] f_{Bus}/4 5[6] 5[6]	MHz MHz MHz

1 Refer to Figure 22 through Figure 25.

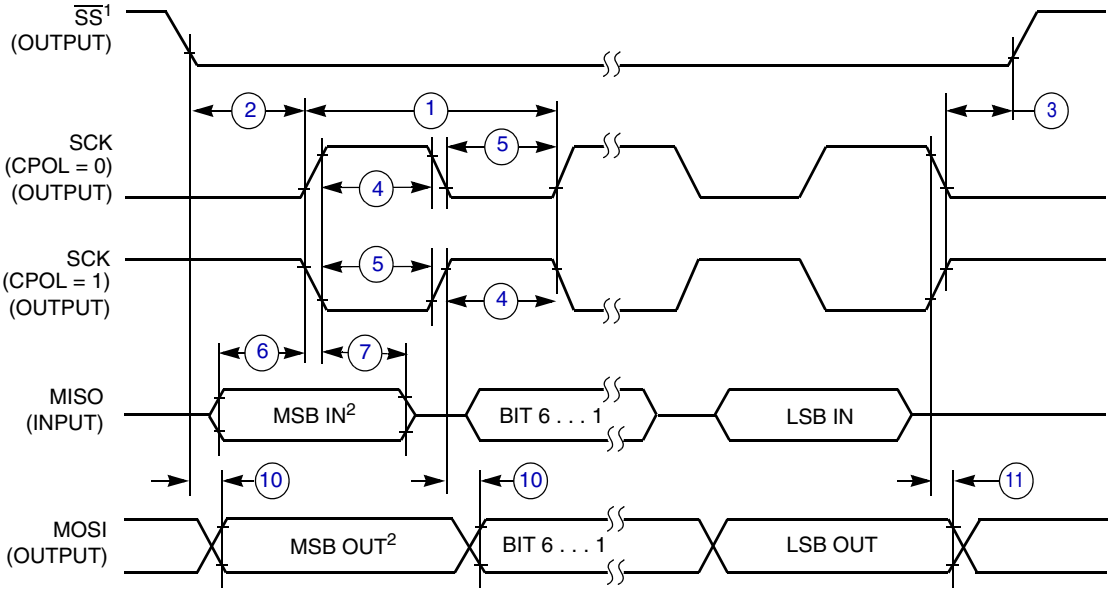
2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.

4 Hold time to high-impedance state.

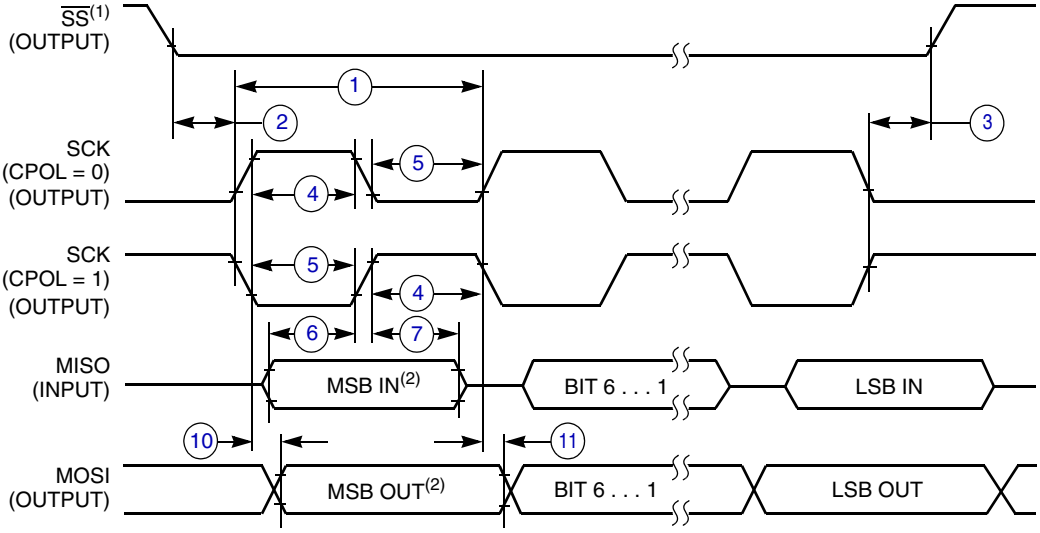
5 Maximum baud rate must be limited to 8 MHz.

6 Maximum baud rate must be limited to 5 MHz due to input filter characteristics.



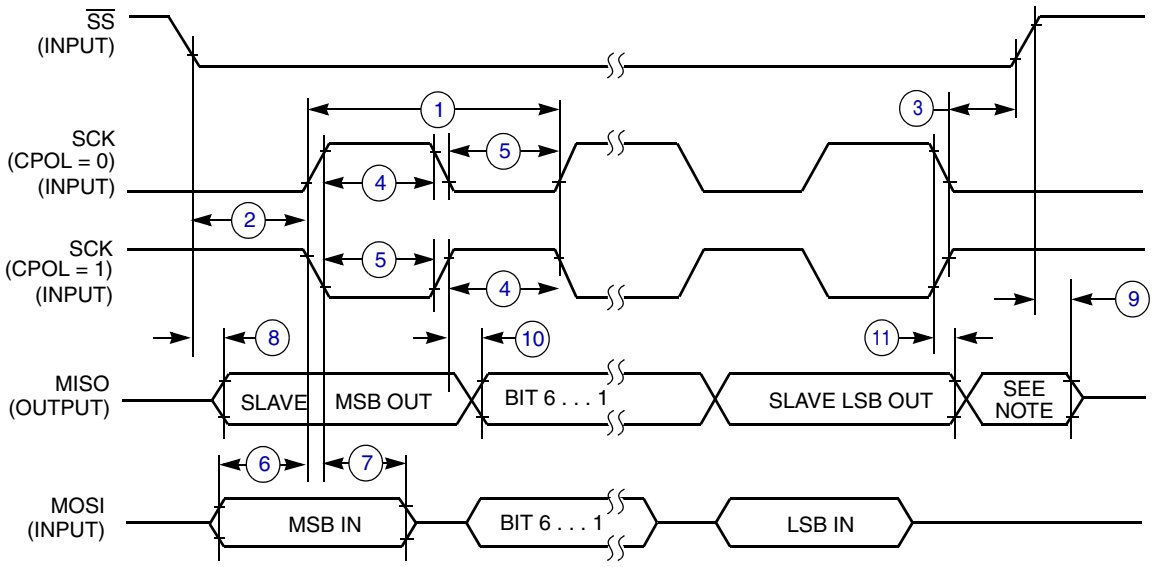
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

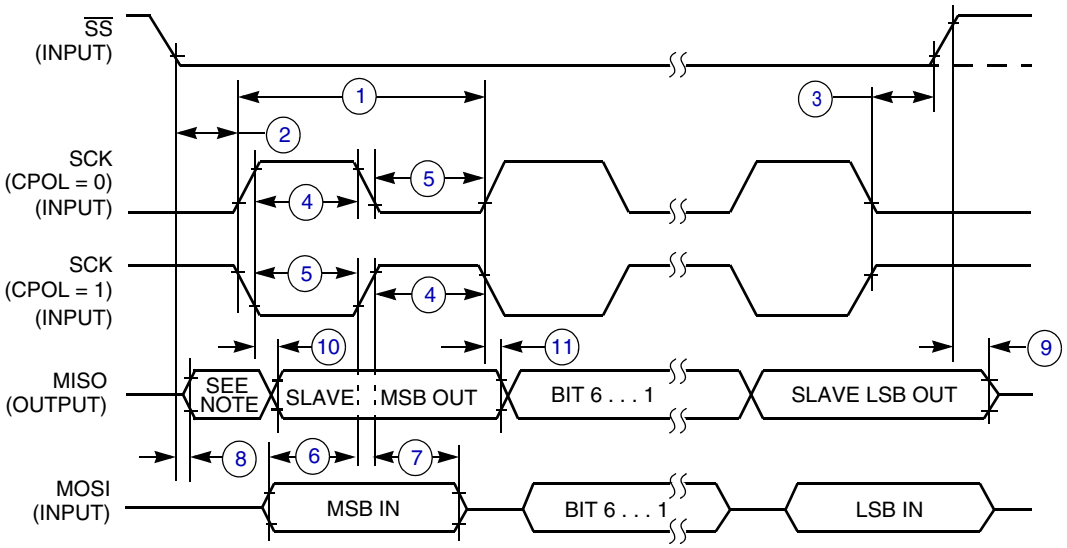
Figure 23. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 24. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 25. SPI Slave Timing (CPHA = 1)