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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f24k42t-i-so">https://www.e-xfl.com/product-detail/microchip-technology/pic18f24k42t-i-so</a>

## REGISTER 3-4: DMA2PR: DMA2 PRIORITY REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1	R/W-1/1
—	—	—	—	—	DMA2PR2	DMA2PR1	DMA2PR0
bit 7					bit 0		

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 u = Bit is unchanged      x = Bit is unknown      -n/n = Value at POR and BOR/Value at all other Resets  
 1 = bit is set      0 = bit is cleared      HS = Hardware set

bit 7-3      **Unimplemented:** Read as '0'

bit 2-0      **DMA2PR<2:0>:** DMA2 Priority Selection bits

## REGISTER 3-5: SCANPR: SCANNER PRIORITY REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1/1	R/W-0/0	R/W-0/0
—	—	—	—	—	SCANPR2	SCANPR1	SCANPR0
bit 7					bit 0		

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 u = Bit is unchanged      x = Bit is unknown      -n/n = Value at POR and BOR/Value at all other Resets  
 1 = bit is set      0 = bit is cleared      HS = Hardware set

bit 7-3      **Unimplemented:** Read as '0'

bit 2-0      **SCANPR<2:0>:** DMA2 Priority Selection bits

## REGISTER 3-6: PRLOCK: PRIORITY LOCK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0
—	—	—	—	—	—	—	PRLOCKED
bit 7					bit 0		

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 u = Bit is unchanged      x = Bit is unknown      -n/n = Value at POR and BOR/Value at all other Resets  
 1 = bit is set      0 = bit is cleared      HS = Hardware set

bit 7-1      **Unimplemented:** Read as '0'

bit 0      **PRLOCKED:** PR Register Lock bit<sup>(1, 2)</sup>

0 = Priority Registers can be modified by write operations; Peripherals do not have access to the memory

1 = Priority Registers are locked and cannot be written; Peripherals do not have access to the memory

**Note 1:** The PRLOCKED bit can only be set or cleared after the unlock sequence.

**2:** If PR1WAY = 1, the PRLOCKED bit cannot be cleared after it has been set. A system Reset will clear the bit and allow one more set.

## 8.11 Start-up Sequence

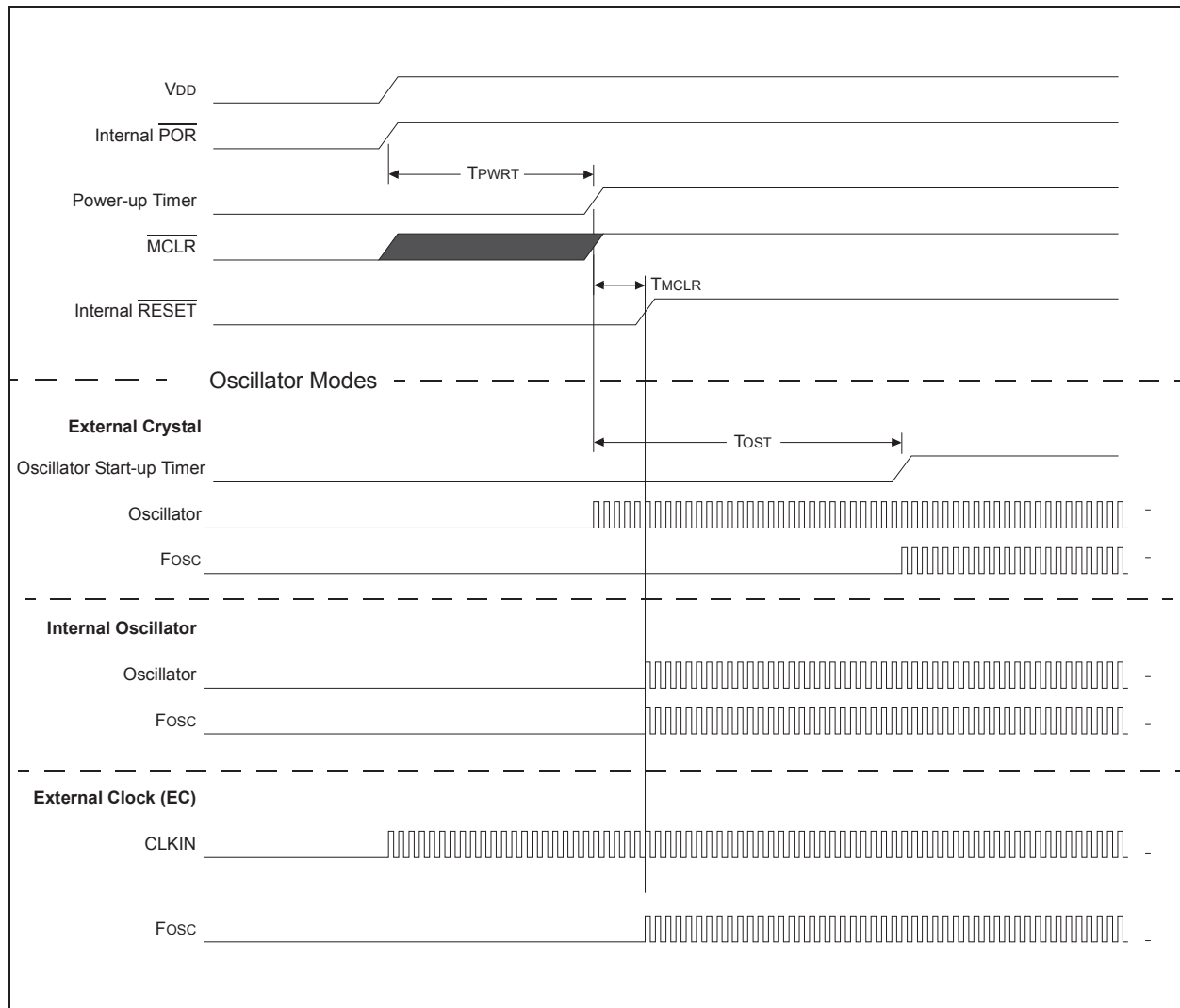
Upon the release of a POR or BOR, the following must occur before the device will begin executing:

1. Power-up Timer runs to completion (if enabled).
2. Oscillator start-up timer runs to completion (if required for selected oscillator source).
3.  $\overline{\text{MCLR}}$  must be released (if enabled).

The total time out will vary based on oscillator configuration and Power-up Timer configuration. See **Section 9.0 “Oscillator Module (with Fail-Safe Clock Monitor)”** for more information.

The Power-up Timer and oscillator start-up timer run independently of  $\overline{\text{MCLR}}$  Reset. If  $\overline{\text{MCLR}}$  is kept low long enough, the Power-up Timer and oscillator Start-up Timer will expire. Upon bringing  $\overline{\text{MCLR}}$  high, the device will begin execution after 10 Fosc cycles (see [Figure 8-4](#)). This is useful for testing purposes or to synchronize more than one device operating in parallel.

**FIGURE 8-4: RESET START-UP SEQUENCE**



## REGISTER 11-27: IPR2: PERIPHERAL INTERRUPT Priority REGISTER 2

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
I2C1RXIP	SPI1IP	SPI1TXIP	SPI1RXIP	DMA1AIP	DMA1ORIP	DMA1DCNTIP	DMA1SCNTIP
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7	<b>I2C1RXIP:</b> I <sup>2</sup> C1 Receive Interrupt Priority bit 1 = High priority 0 = Low priority
bit 6	<b>SPI1IP:</b> SPI1 Transmit Interrupt Priority bit 1 = High priority 0 = Low priority
bit 5	<b>SPI1TXIP:</b> I <sup>2</sup> C1 Transmit Interrupt Priority bit 1 = High priority 0 = Low priority
bit 4	<b>SPI1RXIP:</b> SPI1 Receive Interrupt Priority bit 1 = High priority 0 = Low priority
bit 3	<b>DMA1AIP:</b> DMA1 Abort Transmit Interrupt Priority bit 1 = High priority 0 = Low priority
bit 2	<b>DMA1ORIP:</b> DMA1 Overrun Interrupt Priority bit 1 = High priority 0 = Low priority
bit 1	<b>DMA1DCNTIP:</b> DMA1 Destination Count Interrupt Priority bit 1 = High priority 0 = Low priority
bit 0	<b>DMA1SCNTIP:</b> DMA1 Source Count Interrupt Priority bit 1 = High priority 0 = Low priority

## 16.8 Scanner Module Overview

The Scanner allows segments of the Program Flash Memory or Data EEPROM, to be read out (scanned) to the CRC Peripheral. The Scanner module interacts with the CRC module and supplies it data one word at a time. Data is fetched from the address range defined by SCANLADR registers up to the SCANHADR registers.

The Scanner begins operation when the SGO bit is set (SCANCON0 Register) and ends when either SGO is cleared by the user or when SCANLADR increments past SCANHADR. The SGO bit is also cleared by clearing the EN bit (CRCCON0 register).

## 16.9 Configuring the Scanner

The scanner module may be used in conjunction with the CRC module to perform a CRC calculation over a range of program memory or Data EEPROM addresses. In order to set up the scanner to work with the CRC, perform the following steps:

1. Set up the CRC module (See [Section 16.7 “Configuring the CRC”](#)) and enable the Scanner module by setting the EN bit in the SCANCON0 register.
2. Choose which memory region the Scanner module should operate on and set the MREG bit of the SCANCON0 register appropriately.
3. If trigger is used for scanner operation, set the TRIGEN bit of the SCANCON0 register and select the trigger source using SCANTRIG register. Select the trigger source using SCANTRIG register and then set the TRIGEN bit of the SCANCON0 register. See [Table 16-2](#) for Scanner Operation.
4. If Burst mode of operation is desired, set the BURSTMD bit (SCANCON0 register). See [Table 16-2](#) for Scanner Operation.
5. Set the SCANLADRL/H/U and SCANHADRL/H/U registers with the beginning and ending locations in memory that are to be scanned.
6. Select the priority level for the Scanner module (See [Section 3.1 “System Arbitration”](#)) and lock the priorities (See [Section 3.1.1 “Priority Lock”](#)).
7. Both CRCEN and CRCGO bits must be enabled to use the scanner. Setting the SGO bit will start the scanner operation.

## 16.10 Scanner Interrupt

The scanner will trigger an interrupt when the SCANLADR increments past SCANHADR. The SCANIF bit can only be cleared in software.

## 16.11 Scanning Modes

The interaction of the scanner with the system operation is controlled by the priority selection in the System Arbiter (see [Section 3.2 “Memory Access Scheme”](#)). Additionally, BURSTMD and TRIGEN also determine the operation of the Scanner.

### 16.11.1 TRIGEN = 0, BURSTMD = 0

In this case, the memory access request is granted to the scanner if no other higher priority source is requesting access.

All sources with lower priority than the scanner will get the memory access cycles that are not utilized by the scanner.

### 16.11.2 TRIGEN = 1, BURSTMD = 0

In this case, the memory access request is generated when the CRC module is ready to accept.

The memory access request is granted to the scanner if no other higher priority source is requesting access. All sources with lower priority than the scanner will get the memory access cycles that are not utilized by the scanner.

The memory access request is granted to the scanner if no other higher priority source is requesting access. All sources with lower priority than the scanner will get the memory access cycles that are not utilized by the scanner.

### 16.11.3 TRIGEN = x, BURSTMD = 1

In this case, the memory access is always requested by the scanner.

The memory access request is granted to the scanner if no other higher priority source is requesting access. The memory access cycles will not be granted to lower priority sources than the scanner until it completes operation i.e. SGO = 0 (SCANCON0 register)

**Note:** If TRIGEN = 1 and BURSTMD = 1, the user should ensure that the trigger source is active for the Scanner operation to complete.

## REGISTER 16-14: SCANLADRL: SCAN LOW ADDRESS LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
LADR<7:0> <sup>(1, 2)</sup>							
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0      **LADR<7:0>**: Scan Start/Current Address bits<sup>(1, 2)</sup>  
Least Significant bits of the current address to be fetched from, value increments on each fetch of memory

**Note 1:** Registers SCANLADRU/H/L form a 22-bit value, but are not guarded for atomic or asynchronous access; registers should only be read or written while SGO = 0 (SCANCON0 register).

**2:** While SGO = 1 (SCANCON0 register), writing to this register is ignored.

## REGISTER 16-15: SCANHADRU: SCAN HIGH ADDRESS UPPER BYTE REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	HADR<21:16>					
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6      **Unimplemented:** Read as '0'

bit 5-0      **HADR<21:16>**: Scan End Address bits<sup>(1, 2)</sup>  
Upper bits of the address at the end of the designated scan

**Note 1:** Registers SCANHADRU/H/L form a 22-bit value but are not guarded for atomic or asynchronous access; registers should only be read or written while SGO = 0 (SCANCON0 register).

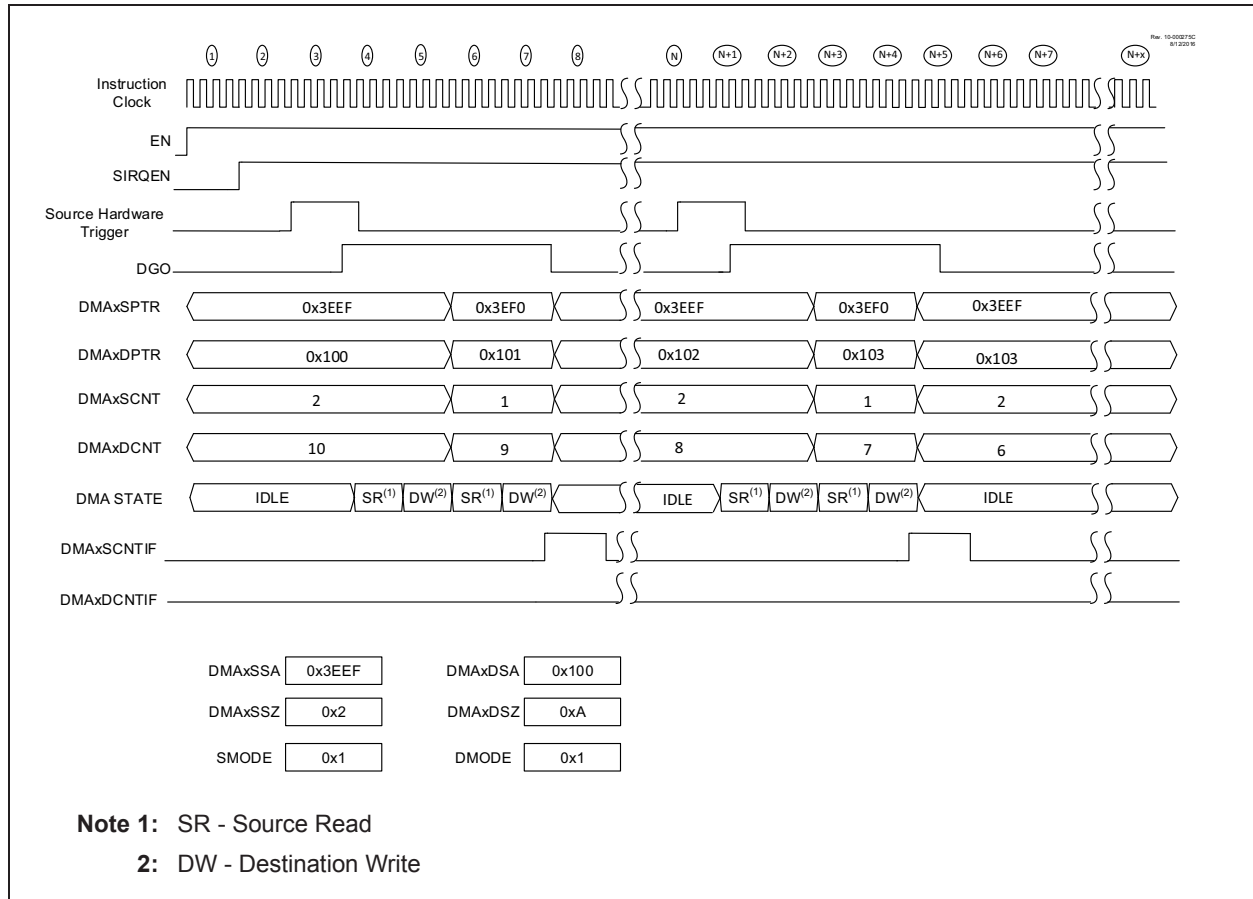
**2:** While SGO = 1 (SCANCON0 register), writing to this register is ignored.

## 17.9.4 TRANSFER FROM SFR TO GPR

The following visual reference describes the sequence of events when copying ADC results to a GPR location. The ADC Interrupt Flag can be chosen as the Source

Hardware trigger, the Source address can be set to point to the ADC Result registers at 3EEF, the Destination address can be set to point to any GPR location of our choice (Example 0x100).

**FIGURE 17-8: SFR SPACE TO GPR SPACE TRANSFER**



**TABLE 17-6: EXAMPLE DMA USE CASE TABLE**

Source Module	Source Register(s)	Destination Module	Destination Register(s)	DCHxSIRQ	Comment
Signal Measurement Timer (SMT)	SMTxCPW[U:H:L]	GPR	GPR[x,y,z]	SMTxPWAIF	Store Captured Pulse-width values
	SMTxCPR[U:H:L]			SMTxPRAIF	Store Captured Period values
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x,y]	TMR0	TMR0[H:L]	TMR0IF	Use as a Timer0 reload for custom 16-bit value
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x]	TMR0	PR0	ANY	Update TMR0 frequency based on a specific trigger
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x,y]	TMR1	TMR1[H:L]	TMR1IF	Use as a Timer1 reload for custom 16-bit value
TMR1	TMR1[H:L]	GPR	GPR[x,y]	TMR1GIF	Use TMR1 Gate interrupt flag to read data out of TMR1 register
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x]	TMR2	PR2	TMR2IF	
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x,y,z]	TMR2 CCP or PWM	PR2 CCPR[H:L] or PWMDC[H:L]	ANY	Frequency generator with 50% duty cycle look up table
CCP	CCPR[H:L]	GPR	GPR[x,y]	CCPxIF	Move data from CCP 16b Capture
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x,y]	CCP	CCPR[H:L]	ANY	Load Compare value or PWM values into the CCP
GPR/SFR/Program Flash/Data EEPROM	MEMORY [x,y,z,u,v,w]	CCPx CCPy CCPz	CCPxR[H:L] CCPyR[H:L] CCPzR[H:L]	ANY	Update multiple PWM values at the same time e.g. 3-phase motor control
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x,y,z]	NCO	NCOxINC[U:H:L]	ANY	Frequency Generator look up table
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x]	DAC	DACxCON0	ANY	Update DAC values
GPR/SFR/Program Flash/Data EEPROM	MEMORY[x]	OSCTUNE	OSCTUNE	ANY	Automated Frequency dithering



## 18.3.4 OPEN-DRAIN CONTROL

The ODCONx register ([Register 18-6](#)) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONx bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONx bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

**Note:** It is not necessary to set open-drain control when using the pin for I<sup>2</sup>C; the I<sup>2</sup>C module controls the pin and makes the pin open-drain.

## 18.3.5 SLEW RATE CONTROL

The SLRCONx register ([Register 18-7](#)) controls the slew rate option for each port pin. Slew rate for each port pin can be controlled independently. When an SLRCONx bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONx bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

## 18.3.6 INPUT THRESHOLD CONTROL

The INLVLx register ([Register 18-8](#)) controls the input voltage threshold for each of the available PORTx input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTx register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See [Table 46-8](#) for more information on threshold levels.

**Note:** Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

## 18.3.7 WEAK PULL-UP CONTROL

The WPUx register ([Register 18-5](#)) controls the individual weak pull-ups for each port pin.

## 18.3.8 EDGE SELECTABLE INTERRUPT-ON-CHANGE

An interrupt can be generated by detecting a signal at the port pin that has either a rising edge or a falling edge. Any individual pin can be configured to generate an interrupt. The interrupt-on-change module is present on all the pins. For further details about the IOC module refer to [Section 20.0 “Interrupt-on-Change”](#).

## 18.3.9 CURRENT-CONTROL DRIVE MODE CONTROL

The CCDPx and CCDNx registers ([Register 18-11](#)) and ([Register 18-12](#)) control the Drive mode for both the positive-going and negative-going drivers. When a CCDPx[y] or CCDNx[y] bit is set and the CCDEN bit of the CCDCON register is set, the Current-Controlled mode is enabled for the corresponding port pin. When the CCDPx[y] or CCDNx[y] bit is clear, the Current-Controlled mode for the corresponding port pin is disabled. If the CCDPx[y] or CCDNx[y] bit is set and the CCDEN bit is clear, operation of the port pin is undefined (see [Section 18.2 “I/O Priorities”](#)).

## 18.3.10 I<sup>2</sup>C PAD CONTROL

For the PIC18(L)F2xK42 devices, the I<sup>2</sup>C specific pads are available on pins RB1, RB2, RC3 and RC4. The I<sup>2</sup>C characteristics of each of these pins is controlled by the RxyI2C registers (see [Register 18-9](#)). These characteristics include enabling I<sup>2</sup>C specific slew rate (over standard GPIO slew rate), selecting internal pull-ups for I<sup>2</sup>C pins, and selecting appropriate input threshold as per SMBus specifications.

**REGISTER 18-3: LATx: LATx REGISTER<sup>(1)</sup>**

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATx7	LATx6	LATx5	LATx4	LATx3	LATx2	LATx1	LATx0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0      **LATx<7:0>**: Rx7:Rx0 Output Latch Value bits

**Note 1:** Writes to LATx are equivalent with writes to the corresponding PORTx register. Reads from LATx register return register values, not I/O pin values.

**TABLE 18-3: LAT REGISTERS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LATA	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0

## REGISTER 24-2: TxRST: TIMER2 EXTERNAL RESET SIGNAL SELECTION REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	RSEL<4:0>				
bit 7							
							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-5

**Unimplemented:** Read as '0'

bit 4-0

**RSEL<4:0>:** Timer2 External Reset Signal Source Selection bits

RSEL<4:0>	T2TMR	TMR4	TMR6
	Reset Source	Reset Source	Reset Source
11111-11001	Reserved	Reserved	Reserved
11000	UART2_tx_edge	UART2_tx_edge	UART2_tx_edge
10111	UART2_rx_edge	UART2_rx_edge	UART2_rx_edge
10110	UART1_tx_edge	UART1_tx_edge	UART1_tx_edge
10101	UART1_rx_edge	UART1_rx_edge	UART1_rx_edge
10100	CLC4_out	CLC4_out	CLC4_out
10011	CLC3_out	CLC3_out	CLC3_out
10010	CLC2_out	CLC2_out	CLC2_out
10001	CLC1_out	CLC1_out	CLC1_out
10000	ZCD_OUT	ZCD_OUT	ZCD_OUT
01111	CMP2OUT	CMP2OUT	CMP2OUT
01110	CMP1OUT	CMP1OUT	CMP1OUT
01101-01100	Reserved	Reserved	Reserved
01011	PWM8OUT	PWM8OUT	PWM8OUT
01010	PWM7OUT	PWM7OUT	PWM7OUT
01001	PWM6OUT	PWM6OUT	PWM6OUT
01000	PWM5OUT	PWM5OUT	PWM5OUT
00111	CCP4OUT	CCP4OUT	CCP4OUT
00110	CCP3OUT	CCP3OUT	CCP3OUT
00101	CCP2OUT	CCP2OUT	CCP2OUT
00100	CCP1OUT	CCP1OUT	CCP1OUT
00011	TMR6 post-scaled	TMR6 post-scaled	Reserved
00010	TMR4 post-scaled	Reserved	TMR4 post-scaled
00001	Reserved	T2TMR post-scaled	T2TMR post-scaled
00000	Pin selected by T2INPPS	Pin selected by T4INPPS	Pin selected by T6INPPS

**TABLE 24-3: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TxPR	Timer2 Module Period Register								323*
TxTMR	Holding Register for the 8-bit T2TMR Register								323*
TxCON	ON	CKPS<2:0>			OUTPS<3:0>				341
TxCLK	—	—	—	—	—	CS<2:0>			338
TxRST	—	—	—	—	RSEL<3:0>				339
TxHLT	$\overline{\text{PSYNC}}$	CPOL	$\overline{\text{CSYNC}}$	MODE<4:0>				342	

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

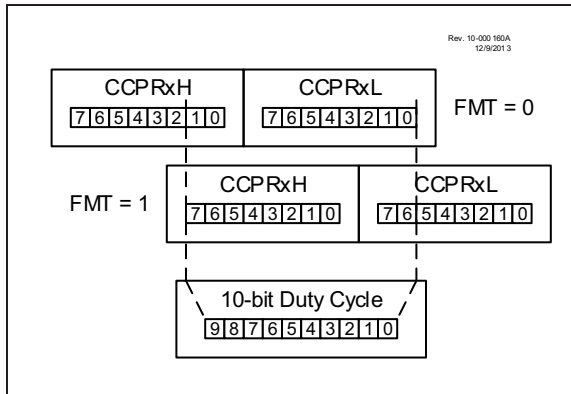
\* Page provides register information.

## 25.4.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the CCPRxH:CCPRxL register pair. The alignment of the 10-bit value is determined by the FMT bit of the CCPxCON register (see Figure 25-5). The CCPRxH:CCPRxL register pair can be written to at any time; however the duty cycle value is not latched into the 10-bit buffer until after a match between T2PR and T2TMR.

Equation 25-2 is used to calculate the PWM pulse width. Equation 25-3 is used to calculate the PWM duty cycle ratio.

**FIGURE 25-5: PWM 10-BIT ALIGNMENT**



**EQUATION 25-2: PULSE WIDTH**

$$\text{Pulse Width} = (\text{CCPRxH:CCPRxL register pair}) \cdot T_{\text{OSC}} \cdot (\text{TMR2 Prescale Value})$$

**EQUATION 25-3: DUTY CYCLE RATIO**

$$\text{Duty Cycle Ratio} = \frac{(\text{CCPRxH:CCPRxL register pair})}{4(T2PR + 1)}$$

CCPRxH:CCPRxL register pair are used to double buffer the PWM duty cycle. This double buffering provides glitchless PWM operation.

The 8-bit timer T2TMR register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH:CCPRxL register pair, then the CCPx pin is cleared (see Figure 25-4).

## 25.4.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when T2PR is 255. The resolution is a function of the T2PR register value as shown by Equation 25-4.

**EQUATION 25-4: PWM RESOLUTION**

$$\text{Resolution} = \frac{\log[4(T2PR + 1)]}{\log(2)} \text{ bits}$$

**Note:** If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

## 26.1 PWMx Pin Configuration

All PWM outputs are multiplexed with the PORT data latch. The user must configure the pins as outputs by clearing the associated TRIS bits.

### 26.1.1 FUNDAMENTAL OPERATION

The PWM module produces a 10-bit resolution output. The PWM timer can be selected using the PxTSEL bits in the CCPTMRS1 register. The default selection for PWMx is T2TMR. Please note that the PWM module operation in the following sections is described with respect to T2TMR. Timer2 and T2PR set the period of the PWM. The PWMxDCL and PWMxDCH registers configure the duty cycle. The period is common to all PWM modules, whereas the duty cycle is independently controlled.

**Note:** The Timer2 postscaler is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

All PWM outputs associated with Timer2 are set when T2TMR is cleared. Each PWMx is cleared when T2TMR is equal to the value specified in the corresponding PWMxDCH (8 MSb) and PWMxDCL<7:6> (2 LSb) registers. When the value is greater than or equal to T2PR, the PWM output is never cleared (100% duty cycle).

**Note:** The PWMxDCH and PWMxDCL registers are double buffered. The buffers are updated when Timer2 matches T2PR. Care should be taken to update both registers before the timer match occurs.

### 26.1.2 PWM OUTPUT POLARITY

The output polarity is inverted by setting the PWMxPOL bit of the PWMxCON register.

### 26.1.3 PWM PERIOD

The PWM period is specified by the T2PR register of Timer2. The PWM period can be calculated using the formula of Equation 26-1. It is required to have Fosc/4 as clock input to Timer2/4/6 for correct PWM operation.

#### EQUATION 26-1: PWM PERIOD

$$PWM\ Period = [(T2PR) + 1] \cdot 4 \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

**Note:** TOSC = 1/FOSC

When T2TMR is equal to T2PR, the following three events occur on the next increment cycle:

- T2TMR is cleared
- The PWM output is active. (Exception: When the PWM duty cycle = 0%, the PWM output will remain inactive.)
- The PWMxDCH and PWMxDCL register values are latched into the buffers.

**Note:** The Timer2 postscaler has no effect on the PWM operation.

### 26.1.4 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the PWMxDCH and PWMxDCL register pair. The PWMxDCH register contains the eight MSbs and the PWMxDCL<7:6>, the two LSbs. The PWMxDCH and PWMxDCL registers can be written to at any time.

Equation 26-2 is used to calculate the PWM pulse width.

Equation 26-3 is used to calculate the PWM duty cycle ratio.

#### EQUATION 26-2: PULSE WIDTH

$$Pulse\ Width = (PWMxDCH:PWMxDCL<7:6>) \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

**Note:** TOSC = 1/FOSC

#### EQUATION 26-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(PWMxDCH:PWMxDCL<7:6>)}{4(T2PR + 1)}$$

The 8-bit timer T2TMR register is concatenated with the two Least Significant bits of 1/FOSC, adjusted by the Timer2 prescaler to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

## 26.1.9 SETUP FOR PWM OPERATION USING PWMx PINS

The following steps should be taken when configuring the module for PWM operation using the PWMx pins:

1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the T2PR register with the PWM period value.
4. Load the PWMxDCH register and bits <7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
  - Clear the TMR2IF interrupt flag bit of the respective PIR register. See Note 1 below.
  - Select the timer clock source to be as  $F_{osc}/4$  using the TxCLK register. This is required for correct operation of the PWM module.
  - Configure the CKPS bits of the T2CON register with the Timer2 prescale value.
  - Enable Timer2 by setting the ON bit of the T2CON register.
6. Enable PWM output pin and wait until Timer2 overflows, TMR2IF bit of the respective PIR register is set. See note below.
7. Enable the PWMx pin output driver(s) by clearing the associated TRIS bit(s) and setting the desired pin PPS control bits.
8. Configure the PWM module by loading the PWMxCON register with the appropriate values.

**Note 1:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be followed in the order given. If it is not critical to start with a complete PWM signal, then move Step 8 to replace Step 4.

**2:** For operation with other peripherals only, disable PWMx pin outputs.

## 26.1.10 SETUP FOR PWM OPERATION TO OTHER DEVICE PERIPHERALS

The following steps should be taken when configuring the module for PWM operation to be used by other device peripherals:

1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the T2PR register with the PWM period value.
4. Load the PWMxDCH register and bits <7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
  - Clear the TMR2IF interrupt flag bit of the respective PIR register. See Note 1 below.
  - Select the timer clock source to be as  $F_{osc}/4$  using the TxCLK register. This is required for correct operation of the PWM module.
  - Configure the CKPS bits of the T2CON register with the Timer2 prescale value.
  - Enable Timer2 by setting the ON bit of the T2CON register.
6. Enable PWM output pin:
  - Wait until Timer2 overflows, TMR2IF bit of the respective PIR register is set. See Note 1 below.
7. Configure the PWM module by loading the PWMxCON register with the appropriate values.

**Note 1:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

## 27.8 Register Definitions: SMT Control

Long bit name prefixes for the Signal Measurement Timer peripherals are shown in [Section 1.4 “Register and Bit naming conventions”](#).

**TABLE 27-2: LONG BIT NAMES PREFIXES FOR SMT PERIPHERALS**

Peripheral	Bit Name Prefix
SMT1	SMT1

**REGISTER 27-1: SMT1CON0: SMT CONTROL REGISTER 0**

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN <sup>(1)</sup>	—	STP	WPOL	SPOL	CPOL	PS<1:0>	
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

‘1’ = Bit is set

‘0’ = Bit is cleared

- bit 7 **EN:** SMT Enable bit<sup>(1)</sup>  
 1 = SMT is enabled  
 0 = SMT is disabled; internal states are reset, clock requests are disabled
- bit 6 **Unimplemented:** Read as ‘0’
- bit 5 **STP:** SMT Counter Halt Enable bit  
 When SMT1TMR = SMT1PR:  
 1 = Counter remains SMT1PR; period match interrupt occurs when clocked  
 0 = Counter resets to 24’h000000; period match interrupt occurs when clocked
- bit 4 **WPOL:** SMT1WIN Input Polarity Control bit  
 1 = SMT1WIN signal is active-low/falling edge enabled  
 0 = SMT1WIN signal is active-high/rising edge enabled
- bit 3 **SPOL:** SMT1SIG Input Polarity Control bit  
 1 = SMT1\_signal is active-low/falling edge enabled  
 0 = SMT1\_signal is active-high/rising edge enabled
- bit 2 **CPOL:** SMT Clock Input Polarity Control bit  
 1 = SMT1TMR increments on the falling edge of the selected clock signal  
 0 = SMT1TMR increments on the rising edge of the selected clock signal
- bit 1-0 **PS<1:0>:** SMT Prescale Select bits  
 11 = Prescaler = 1:8  
 10 = Prescaler = 1:4  
 01 = Prescaler = 1:2  
 00 = Prescaler = 1:1

**Note 1:** Setting EN to ‘0’ does not affect the register contents.



## 34.3.3 TRANSMIT AND RECEIVE FIFOS

The transmission and reception of data from the SPI module is handled by two FIFOs, one for reception and one for transmission (addressed by the SFRs SPIRXB and SPIXTB, respectively). The TXFIFO is written by software and is read by the SPI module to shift the data onto the SDO pin. The RXFIFO is written by the SPI module as it shifts in the data from the SDI pin and is read by software. Setting the CLRBF bit of SPIXSTATUS resets the occupancy for both FIFOs, emptying both buffers. The FIFOs are also reset by disabling the SPI module.

**Note:** TXFIFO occupancy and RXFIFO occupancy simply refer to the number of bytes that are currently being stored in each FIFO. These values are used in this chapter to illustrate the function of these FIFOs and are not directly accessible through software.

The SPIRXB register addresses the receive FIFO and is read-only. Reading from this register will read from the first FIFO location that was written to by hardware and decrease the RXFIFO occupancy. If the FIFO is empty, reading from this register will instead return a value of zero and set the RXRE (Receive Buffer Read Error) bit of the SPIXSTATUS register. The RXRE bit must then be cleared in software in order to properly reflect the status of the read error. When RXFIFO is full, the RXBF bit of the SPIXSTATUS register will be set. When the device receives data on the SDI pin, the receive FIFO may be written to by hardware and the occupancy increased, depending on the mode and receiver settings, as summarized in [Table 34-1](#).

The SPIXTB register addresses the transmit FIFO and is write-only. Writing to the register will write to the first empty FIFO location and increase the occupancy. If the FIFO is full, writing to this register will not affect the data and will set the TXWE bit of the SPIXSTATUS register. When the TXFIFO is empty, the TXBE bit of SPIXSTATUS will be set. When a data transfer occurs, data may be read from the first FIFO location written to and the occupancy decreases, depending on mode and transmitter settings, as summarized in [Table 34-1](#) and [Section 34.6.1 “Slave Mode Transmit options”](#).

## 34.3.4 LSB VS. MSB-FIRST OPERATION

Typically, SPI communication is output Most-Significant bit first, but some devices/buses may not conform to this standard. In this case, the LSBF bit may be used to alter the order in which bits are shifted out during the data exchange. In both Master and Slave mode, the LSBF bit of SPIXCON0 controls if data is shifted MSb or LSb first. Clearing the bit (default) configures the data to transfer MSb first, which is traditional SPI operation, while setting the bit configures the data to transfer LSb first.

## 34.3.5 INPUT AND OUTPUT POLARITY BITS

SPIXCON1 has three bits that control the polarity of the SPI inputs and outputs. The SDIP bit controls the polarity of the SDI input, the SDOP bit controls the polarity of the SDO output, and the SSP bit controls the polarity of both the slave  $\overline{SS}$  input and the master SS output. For all three bits, when the bit is clear, the input or output is active-high, and when the bit is set, the input or output is active-low. When the EN bit of SPIXCON0 is cleared,  $\overline{SS}(\text{out})$  and SCK(out) both revert to the inactive state dictated by their polarity bits. The SDO output state when the EN bit of SPIXCON0 is cleared is determined by several factors.

- When the associated TRIS bit for the SDO pin is cleared, and the SPI goes Idle after a transmission, the SDO output will remain at the last bit level. The SDO pin will revert to the Idle state if EN is cleared.
- When the associated TRIS bit for the SDO pin is set, behavior varies in Slave and Master mode.
  - In Slave mode, the SDO pin tri-states when:
    - Slave Select is inactive,
    - the EN bit of SPIXCON0 is cleared, or when
    - the TXR bit of SPIXCON2 is cleared.
  - In Master mode, the SDO pin tri-states when TXR = 0. When TXR = 1 and the SPI goes Idle after a transmission, the SDO output will remain at the last bit level. The SDO pin will revert to the Idle state if EN is cleared.

## 34.5.6 MASTER MODE SPI CLOCK CONFIGURATION

### 34.5.6.1 SPI Clock Selection

The clock source for SPI master modes is selected by the SPIxCLK register. Selections include the following:

- FOSC
- HFINTOSC
- CLKREF
- Timer0\_overflow
- Timer2\_Postscaled
- Timer4\_Postscaled
- Timer6\_Postscaled
- SMT\_match

The SPIxBAUD register allows for dividing this clock. The frequency of the SCK output is defined by [Equation 34-1](#):

#### EQUATION 34-1: FREQUENCY OF SCK OUTPUT SIGNAL

$$F_{BAUD} = \frac{F_{CSEL}}{(2 \cdot (BAUD + 1))}$$

where FBAUD is the baud rate frequency output on the SCK pin, FCSEL is the frequency of the input clock selected by the SPIxCLK register, and BAUD is the value contained in the SPIxBAUD register.

### 34.5.6.2 CKE, CKP and SMP

The CKP, CKE, and SMP bits control the relationship between the SCK clock output, SDO output data changes, and SDI input data sampling. The bit functions are as follows:

- CKP - SCK output polarity
- CKE - SDO output change relative to the SCK clock
- SMP - SDI input sampling relative to the clock edges

The CKE bit, when set, inverts the low Idle state of the SCK output to a high Idle state.

[Figure 34-7](#) through [Figure 34-10](#) illustrate the eight possible combinations of the CKP, CKE, and SMP bit selections.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. When the CKE bit is cleared, the SDO data is undefined prior to the first SCK edge.

**Note:** All timing diagrams assume the LSBF bit of SPIxCON0 is cleared.

## 36.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of  $V_{DD}$ , with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- ADC positive reference
- Comparator input
- Digital-to-Analog Converter (DAC)

The FVR can be enabled by setting the EN bit of the FVRCON register.

**Note:** Fixed Voltage Reference output cannot exceed  $V_{DD}$ .

### 36.1 Independent Gain Amplifiers

The output of the FVR, which is connected to the ADC, Comparators, and DAC, is routed through two independent programmable gain amplifiers. Each amplifier can be programmed for a gain of 1x, 2x or 4x, to produce the three possible voltage levels.

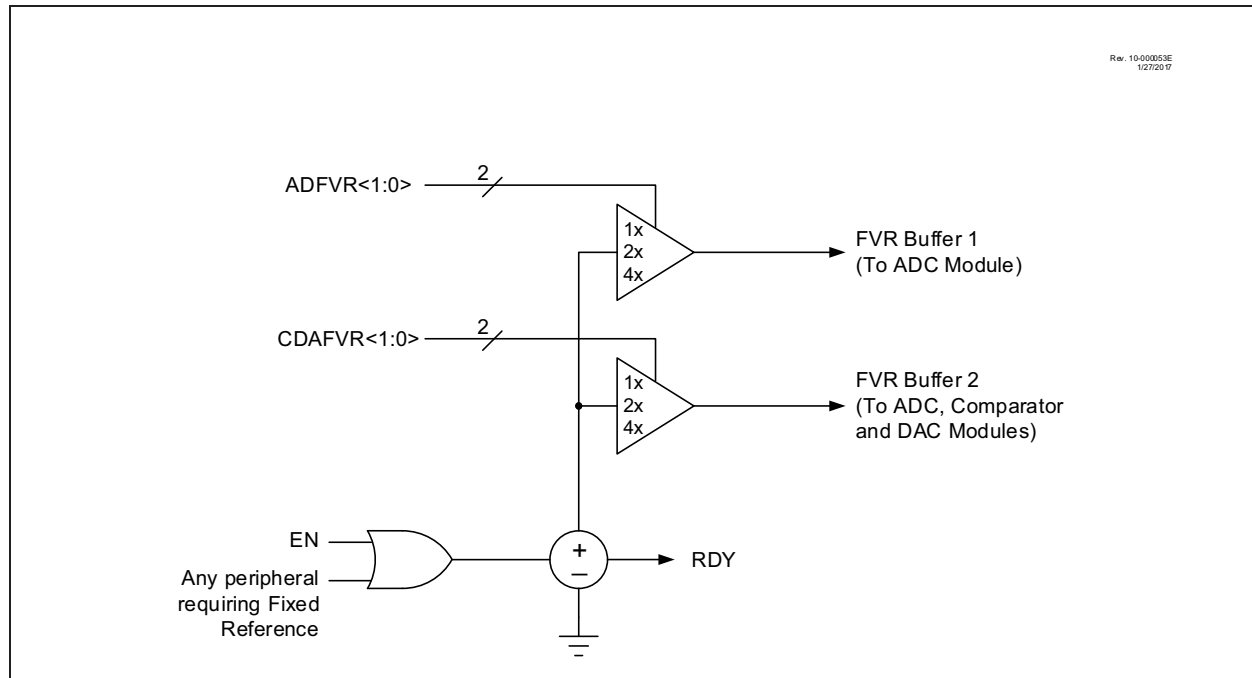
The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference **Section 38.0 “Analog-to-Digital Converter with Computation (ADC2) Module”** for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the DAC and comparator module. Reference **Section 39.0 “5-Bit Digital-to-Analog Converter (DAC) Module”** and **Section 40.0 “Comparator Module”** for additional information.

### 36.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the RDY bit of the FVRCON register will be set.

**FIGURE 36-1: VOLTAGE REFERENCE BLOCK DIAGRAM**



## 36.3 Register Definitions: FVR Control

**REGISTER 36-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER**

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	RDY <sup>(1)</sup>	TSEN <sup>(3)</sup>	TSRNG <sup>(3)</sup>	CDAFVR<1:0>		ADFVR<1:0>	
bit 7				bit 0			

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	<b>EN:</b> Fixed Voltage Reference Enable bit 1 = Fixed Voltage Reference is enabled 0 = Fixed Voltage Reference is disabled
bit 6	<b>RDY:</b> Fixed Voltage Reference Ready Flag bit <sup>(1)</sup> 1 = Fixed Voltage Reference output is ready for use 0 = Fixed Voltage Reference output is not ready or not enabled
bit 5	<b>TSEN:</b> Temperature Indicator Enable bit <sup>(3)</sup> 1 = Temperature Indicator is enabled 0 = Temperature Indicator is disabled
bit 4	<b>TSRNG:</b> Temperature Indicator Range Selection bit <sup>(3)</sup> 1 = V <sub>OUT</sub> = 3V <sub>T</sub> (High Range) 0 = V <sub>OUT</sub> = 2V <sub>T</sub> (Low Range)
bit 3-2	<b>CDAFVR&lt;1:0&gt;:</b> Comparator FVR Buffer Gain Selection bits 11 = FVR Buffer 1 Gain is 4x, (4.096V) <sup>(2)</sup> 10 = FVR Buffer 1 Gain is 2x, (2.048V) <sup>(2)</sup> 01 = FVR Buffer 1 Gain is 1x, (1.024V) 00 = FVR Buffer 1 is off
bit 1-0	<b>ADFVR&lt;1:0&gt;:</b> ADC FVR Buffer Gain Selection bit 11 = FVR Buffer 2 Gain is 4x, (4.096V) <sup>(2)</sup> 10 = FVR Buffer 2 Gain is 2x, (2.048V) <sup>(2)</sup> 01 = FVR Buffer 2 Gain is 1x, (1.024V) 00 = FVR Buffer 2 is off

- Note 1:** FVRRDY is always '1'.  
**2:** Fixed Voltage Reference output cannot exceed V<sub>DD</sub>.  
**3:** See **Section 37.0 "Temperature Indicator Module"** for additional information.

**TABLE 36-1: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	EN	RDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		600

**Legend:** — = Unimplemented location, read as '0'. Shaded cells are not used with the Fixed Voltage Reference.

## 40.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the HYS bit of the CMxCON0 register.

See Comparator Specifications in [Table 46-15](#) for more information.

### 40.3.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the SYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used, the CxOUT bit is synchronized with the timer, so that the software sees no ambiguity due to timing. See the Comparator Block Diagram ([Figure 40-2](#)) and the Timer1 Block Diagram ([Figure 23-1](#)) for more information.

## 40.4 Comparator Interrupt

An interrupt can be generated for every rising or falling edge of the comparator output.

When either edge detector is triggered and its associated enable bit is set (INTP and/or INTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the respective PIR register) will be set.

To enable the interrupt, you must set the following bits:

- EN bit of the CMxCON0 register
- CxIE bit of the respective PIE register
- INTP bit of the CMxCON1 register (for a rising edge detection)
- INTN bit of the CMxCON1 register (for a falling edge detection)
- GIE bit of the INTCON0 register

The associated interrupt flag bit, CxIF bit of the respective PIR register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

**Note:** Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the POL bit of the CMxCON0 register, or by switching the comparator on or off with the EN bit of the CMxCON0 register.

## 40.5 Comparator Positive Input Selection

Configuring the PCH<2:0> bits of the CMxPCH register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN0+, CxIN1+ analog pin
- DAC output
- FVR (Fixed Voltage Reference)
- Vss (Ground)

See [Section 36.0 “Fixed Voltage Reference \(FVR\)”](#) for more information on the Fixed Voltage Reference module.

See [Section 39.0 “5-Bit Digital-to-Analog Converter \(DAC\) Module”](#) for more information on the DAC input signal.

Any time the comparator is disabled (EN = 0), all comparator inputs are disabled.

## 40.6 Comparator Negative Input Selection

The NCH<2:0> bits of the CMxNCH register direct an analog input pin and internal reference voltage or analog ground to the inverting input of the comparator:

- CxIN0-, CxIN1-, CxIN2-, CxIN3- analog pin
- FVR (Fixed Voltage Reference)
- Analog Ground

**Note:** To use CxINy+ and CxINy- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.