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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf24k42-i-sp

eXtreme Low-Power (XLP) Features

- Sleep mode: 60 nA @ 1.8V, typical
- Watchdog Timer: 720 nA @ 1.8V, typical
- Secondary Oscillator: 580 nA @ 32 kHz
- Operating Current:
  - 4 uA @ 32 kHz, 1.8V, typical
  - 45 uA/MHz @ 1.8V, typical

Digital Peripherals

- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Four 16-Bit Timers (TMR0/1/3/5)
- Four Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Three Complementary Waveform Generators (CWGs):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Four Capture/Compare/PWM (CCP) modules
- Four 10-bit Pulse Width Modulators (PWMs)
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0 Hz < f_{NCO} < 32 MHz
  - Resolution: f_{NCO}/220
- DSM: Data Signal Modulator
  - Multiplex two carrier clocks, with glitch prevention feature
  - Multiple sources for each carrier
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for fail-safe operation (e.g., Class B)
  - Calculate CRC over any portion of program memory
- Two UART Modules:
  - Modules are Asynchronous, RS-232, RS-485 compatibility.
  - One of the UART modules supports LIN Master and Slave, DMX mode, DALI Gear and Device protocols
  - Automatic and user-timed BREAK period generation
  - DMA Compatible
  - Automatic checksums
  - Programmable 1, 1.5, and 2 stop bits
  - Wake-up on BREAK reception
  - Automatic and user-timed BREAK period generation
- One SPI module:
  - Configurable length bytes
  - Arbitrary length data packets
  - Receive-without-transmit option
  - Transmit-without-receive option
  - Transfer byte counter
  - Separate Transmit and Receive Buffers with 2-byte FIFO and DMA capabilities
- Two I^{2}C modules, SMBus, PMBus™ compatible:
  - Dedicated Address, Transmit and Receive buffers
  - Bus Collision Detection with arbitration
  - Bus time-out detection and handling
  - Multi-Master mode
  - Separate Transmit and Receive Buffers with 2-byte FIFO and DMA capabilities
  - I^{2}C, SMBus, 2.0 and SMBus 3.0, and 1.8V input level selections
- Device I/O Port Features:
  - 25 I/O pins (PIC18(L)F24/25/26/27K42)
  - 36 I/O pins (PIC18(L)F45/46/47K42)
  - 44 I/O pins (PIC18(L)F55/56/57K42)
  - One input only pin
  - Individually programmable I/O direction, open-drain, slew rate, weak pull-up control
  - High-current source/sink for direct LED drive
  - Interrupt-on-change
  - Three External Interrupt Pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Hardware Limit Timer (HLT):
  - Hardware monitoring and Fault detection
- Signal Measurement Timer (SMT):
  - 24-bit timer/counter with prescaler

4.3.2 LOOK-UP TABLES IN PROGRAM MEMORY

There may be programming situations that require the creation of data structures, or look-up tables, in program memory. For PIC18 devices, look-up tables can be implemented in two ways:

- Computed `GOTO`
- Table Reads

4.3.2.1 Computed `GOTO`

A computed `GOTO` is accomplished by adding an offset to the program counter. An example is shown in Example 4-2.

A look-up table can be formed with an `ADDWF PCL` instruction and a group of `RETLW nn` instructions. The W register is loaded with an offset into the table before executing a call to that table. The first instruction of the called routine is the `ADDWF PCL` instruction. The next instruction executed will be one of the `RETLW nn` instructions that returns the value ‘`nn`’ to the calling function.

The offset value (in WREG) specifies the number of bytes that the program counter should advance and should be multiples of two (LSb = `0`).

In this method, only one data byte may be stored in each instruction location and room on the return address stack is required.

EXAMPLE 4-2: COMPUTED GOTO USING AN OFFSET VALUE

```
        MOVF    OFFSET, W
        CALL    TABLE
ORG     nn00h
TABLE   ADDWF   PCL
        RETLW   nnh
        RETLW   nnh
        RETLW   nnh
        .
        .
        .
```

4.3.2.2 Table Reads and Table Writes

A better method of storing data in program memory allows two bytes of data to be stored in each instruction location.

Look-up table data may be stored two bytes per program word by using table reads and writes. The Table Pointer (TBLPTR) register specifies the byte address and the Table Latch (TABLAT) register contains the data that is read from or written to program memory. Data is transferred to or from read/write latches one byte at a time.

Table read and table write operations are discussed further in **Section 15.1.1 “Table Reads and Table Writes”**.

5.2 Register Definitions: Configuration Words

REGISTER 5-1: CONFIGURATION WORD 1L (30 0000h)

U-1	R/W-1	R/W-1	R/W-1	U-1	R/W-1	R/W-1	R/W-1
—	RSTOSC<2:0>			—	FEXTOSC<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’	
-n = Value for blank device	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘1’

bit 6-4 **RSTOSC<2:0>:** Power-up Default Value for COSC bits

This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.
111 = EXTOSC operating per FEXTOSC<2:0> bits (device manufacturing default)
110 = HFINTOSC with FRQ = 4 MHz and CDIV = 4:1
101 = LFINTOSC
100 = SOSC
011 = Reserved
010 = EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC<2:0> bits
001 = Reserved
000 = HFINTOSC with FRQ = 64 MHz and CDIV = 1:1; resets COSC/NOSC to 3’b110

bit 3 **Unimplemented:** Read as ‘1’

bit 2-0 **FEXTOSC<2:0>:** FEXTOSC External Oscillator Mode Selection bits

111 = EC (External Clock) above 8 MHz
110 = EC (External Clock) for 500 kHz to 8 MHz
101 = EC (External Clock) below 500 kHz
100 = Oscillator is not enabled
011 = Reserved (do not use)
010 = HS (crystal oscillator) above 8 MHz
001 = XT (crystal oscillator) above 500 kHz, below 8 MHz
000 = LP (crystal oscillator) optimized for 32.768 kHz; PFM set to low power

9.2.2.3 Internal Oscillator Frequency Adjustment

The internal oscillator is factory-calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 9-3).

The default value of the OSCTUNE register is 00h. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE **does not affect** the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), WWDT, Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

9.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is a factory-calibrated 31 kHz internal clock source.

The LFINTOSC is the frequency for the Power-up Timer (PWRT), Windowed Watchdog Timer (WWDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled through one of the following methods:

- Programming the RSTOSC<2:0> bits of Configuration Word 1 to enable LFINTOSC.
- Write to the NOSC<2:0> bits of the OSCCON1 register during run-time. See **Section 9.3, Clock Switching** for more information.

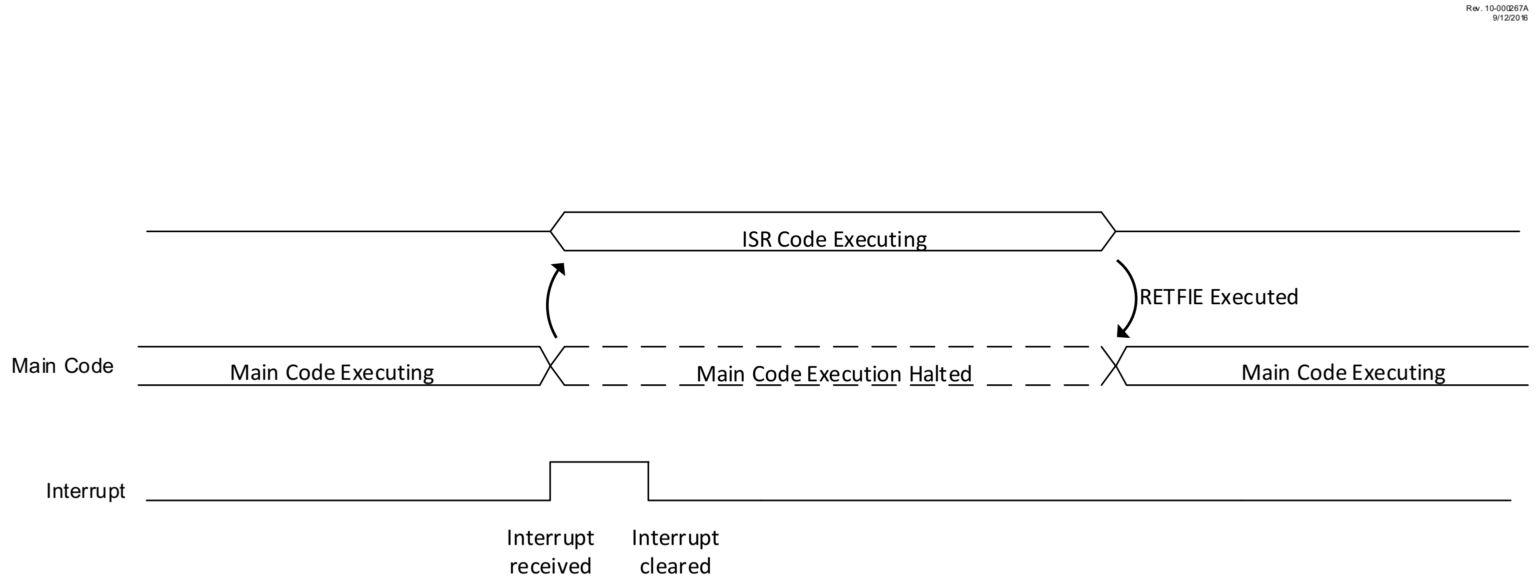
9.2.2.5 ADCRC

The ADCRC is an oscillator dedicated to the ADC^2 module. The ADCRC oscillator can be manually enabled using the ADOEN bit of the OSCEN register. The ADCRC runs at a fixed frequency of 600 kHz. ADCRC is automatically enabled if it is selected as the clock source for the ADC^2 module.

11.4.1 SERVING A HIGH OR LOW PRIORITY INTERRUPT WHEN MAIN ROUTINE CODE IS EXECUTING

When a high or low priority interrupt is requested when the main routine code is executing, the main routine execution is halted and the ISR is addressed, see Figure 11-2. Upon a return from the ISR (by executing the RETFIE instruction), the main routine resumes execution.

FIGURE 11-2: INTERRUPT EXECUTION: HIGH/LOW PRIORITY INTERRUPT WHEN EXECUTING MAIN ROUTINE



REGISTER 11-21: PIE7: PERIPHERAL INTERRUPT ENABLE REGISTER 7

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0
—	—	INT2IE	CLC2IE	CWG2IE	—	CCP2IE	TMR4IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **INT2IE:** External Interrupt 2 Enable bit
1 = Enabled
0 = Disabled

bit 4 **CLC2IE:** CLC2 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 3 **CWG2IE:** CWG2 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **CCP2IE:** CCP2 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 **TMR4IE:** TMR4 Interrupt Enable bit
1 = Enabled
0 = Disabled

REGISTER 12-2: CPUDOZE: DOZE AND IDLE REGISTER

R/W-0/u	R/W/HC/HS-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
IDLEN	DOZEN	ROI	DOE	—	DOZE<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **IDLEN:** Idle Enable bit
1 = A SLEEP instruction inhibits the CPU clock, but not the peripheral clock(s)
0 = A SLEEP instruction places the device into full Sleep mode

bit 6 **DOZEN:** Doze Enable bit[1,2]
1 = The CPU executes instruction cycles according to DOZE setting
0 = The CPU executes all instruction cycles (fastest, highest power operation)

bit 5 **ROI:** Recover-On-Interrupt bit
1 = Entering the Interrupt Service Routine (ISR) makes DOZEN = 0 bit, bringing the CPU to full-speed operation
0 = Interrupt entry does not change DOZEN

bit 4 **DOE:** Doze-On-Exit bit
1 = Executing RETFIE makes DOZEN = 1, bringing the CPU to reduced speed operation
0 = RETFIE does not change DOZEN

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DOZE<2:0>:** Ratio of CPU Instruction Cycles to Peripheral Instruction Cycles
111 =1:256
110 =1:128
101 =1:64
100 =1:32
011 =1:16
010 =1:8
001 =1:4
000 =1:2

Note 1: When ROI = 1 or DOE = 1, DOZEN is changed by hardware interrupt entry and/or exit.
2: Entering ICD overrides DOZEN, returning the CPU to full execution speed; this bit is not affected.

TABLE 12-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
VREGCON	—	—	—	—	—	—	VREGPM	Reserved	180
CPUDOZE	IDLEN	DOZEN	ROI	DOE	—	DOZE<2:0>			181

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used in Power-Down mode.

15.4 Register Definitions: Nonvolatile Memory

REGISTER 15-1: NVMCON1: NONVOLATILE MEMORY CONTROL 1 REGISTER

R/W-0/0	R/W-0/0	U-0	R/S/HC-0/0	R/W/HS-x/q	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
REG<1:0>		—	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	HC = Bit is cleared by hardware
x = Bit is unknown	-n = Value at POR	S = Bit can be set by software, but not cleared
‘0’ = Bit is cleared	‘1’ = Bit is set	U = Unimplemented bit, read as ‘0’

bit 7-6 **REG<1:0>:** NVM Region Selection bit
10 =Access PFM Locations
x1 = Access User IDs, Configuration Bits, DIA, DCI, Rev ID and Device ID
00 = Access Data EEPROM Memory Locations

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **FREE:** Program Flash Memory Erase Enable bit[1]
1 = Performs an erase operation on the next WR command
0 = The next WR command performs a write operation

bit 3 **WRERR:** Write-Reset Error Flag bit[2,3,4]
1 = A write operation was interrupted by a Reset (hardware set),
or WR was written to 1’b1 when an invalid address is accessed (Table 9-1, Table 15-1)
or WR was written to 1’b1 when REG<1:0> and address do not point to the same region
or WR was written to 1’b1 when a write-protected address is accessed (Table 9-2).
0 = All write operations have completed normally

bit 2 **WREN:** Program/Erase Enable bit
1 = Allows program/erase and refresh cycles
0 = Inhibits programming/erasing and user refresh of NVM

bit 1 **WR:** Write Control bit[5,6,7]
When REG points to a Data EEPROM Memory location:
1 = Initiates an erase/program cycle at the corresponding Data EEPROM Memory location
When REG points to a PFM location:
1 = Initiates the PFM write operation with data from the holding registers
0 = NVM program/erase operation is complete and inactive

bit 0 **RD:** Read Control bit[8]
1 = Initiates a read at address pointed by REG and NVMADR, and loads data into NVMDAT
0 = NVM read operation is complete and inactive

Note 1: This can only be used with PFM.
2: This bit is set when WR = 1 and clears when the internal programming timer expires or the write is completed successfully.
3: Bit must be cleared by the user; hardware will not clear this bit.
4: Bit may be written to ‘1’ by the user in order to implement test sequences.
5: This bit can only be set by following the unlock sequence of **Section 15.1.4 “NVM Unlock Sequence”**.
6: Operations are self-timed and the WR bit is cleared by hardware when complete.
7: Once a write operation is initiated, setting this bit to zero will have no effect.
8: The bit can only be set in software. The bit is cleared by hardware when the operation is complete.

REGISTER 17-3: DMAxBUF – DMAx DATA BUFFER REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
BUF7	BUF6	BUF5	BUF4	BUF3	BUF2	BUF1	BUF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	

-n/n = Value at POR and BOR/Value at all other Resets	1 = bit is set	0 = bit is cleared	x = bit is unknown
			u = bit is unchanged

bit 7-0 **BUF<7:0>:** DMA Internal Data Buffer bits

DMABUF<7:0>

These bits reflect the content of the internal data buffer the DMA peripheral uses to hold the data being moved from the source to destination.

REGISTER 17-4: DMAxSSAL – DMAx SOURCE START ADDRESS LOW REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SSA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	

-n/n = Value at POR and BOR/Value at all other Resets	1 = bit is set	0 = bit is cleared	x = bit is unknown
			u = bit is unchanged

bit 7-0 **SSA<7:0>:** Source Start Address bits

REGISTER 17-5: DMAxSSAH – DMAx SOURCE START ADDRESS HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SSA<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	

-n/n = Value at POR and BOR/Value at all other Resets	1 = bit is set	0 = bit is cleared	x = bit is unknown
			u = bit is unchanged

bit 7-0 **SSA<15:8>:** Source Start Address bits

REGISTER 17-15: DMAxDSAH – DMAx DESTINATION START ADDRESS HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
DSA<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	

-n/n = Value at POR and BOR/Value at all other Resets	1 = bit is set	0 = bit is cleared	x = bit is unknown
			u = bit is unchanged

bit 7-0 **DSA<15:8>:** Destination Start Address bits

REGISTER 17-16: DMAxDPTRL – DMAx DESTINATION POINTER LOW REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DPTR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	

-n/n = Value at POR and BOR/Value at all other Resets	1 = bit is set	0 = bit is cleared	x = bit is unknown
			u = bit is unchanged

bit 7-0 **DPTR<7:0>:** Current Destination Address Pointer

REGISTER 17-17: DMAxDPTRH – DMAx DESTINATION POINTER HIGH REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DPTR<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	

-n/n = Value at POR and BOR/Value at all other Resets	1 = bit is set	0 = bit is cleared	x = bit is unknown
			u = bit is unchanged

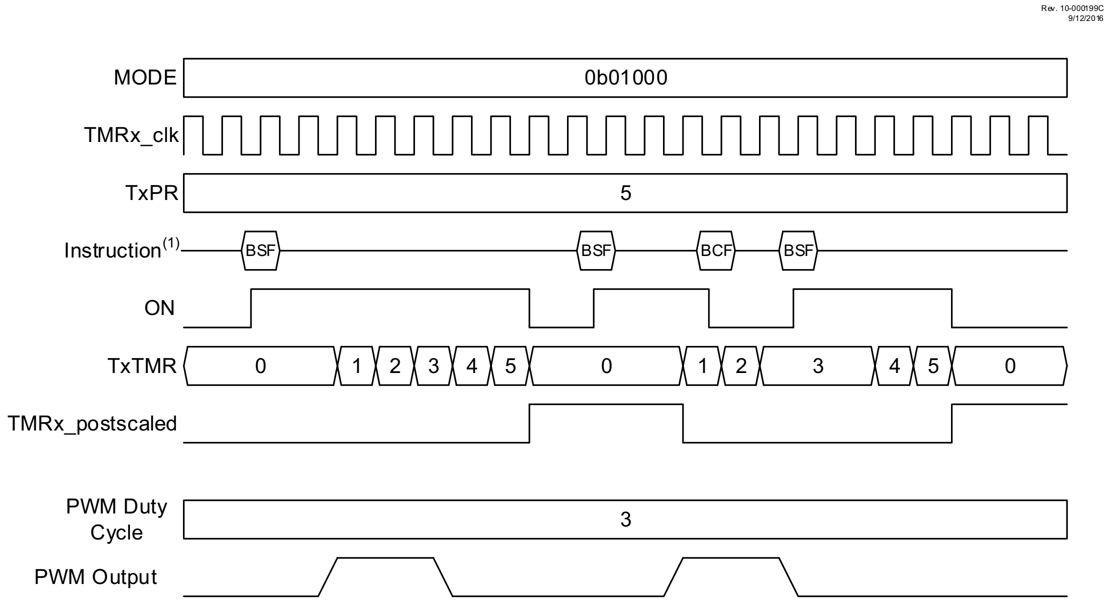
bit 7-0 **DPTR<15:8>:** Current Destination Address Pointer

24.5.5 SOFTWARE START ONE-SHOT MODE

In One-Shot mode the timer resets and the ON bit is cleared when the timer value matches the T2PR period value. The ON bit must be set by software to start another timer cycle. Setting MODE<4:0> = `01000` selects One-Shot mode which is illustrated in Figure 24-8. In the example, ON is controlled by BSF and BCF instructions. In the first case, a BSF instruction sets ON and the counter runs to completion and clears ON. In the second case, a BSF instruction starts the cycle, BCF/BSF instructions turn the counter off and on during the cycle, and then it runs to completion.

When One-Shot mode is used in conjunction with the CCP PWM operation the PWM pulse drive starts concurrent with setting the ON bit. Clearing the ON bit while the PWM drive is active will extend the PWM drive. The PWM drive will terminate when the timer value matches the CCPRx pulse width value. The PWM drive will remain off until software sets the ON bit to start another cycle. If software clears the ON bit after the CCPRx match but before the T2PR match then the PWM drive will be extended by the length of time the ON bit remains cleared. Another timing cycle can only be initiated by setting the ON bit after it has been cleared by a T2PR period count match.

FIGURE 24-8: SOFTWARE START ONE-SHOT MODE TIMING DIAGRAM (MODE = `01000`)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

25.5 Register Definitions: CCP Control

Long bit name prefixes for the CCP peripherals are shown in Table 25-4. Refer to **Section 1.4.2.2 “Long Bit Names”** for more information.

TABLE 25-4:

Peripheral	Bit Name Prefix
CCP1	CCP1
CCP2	CCP2
CCP3	CCP3
CCP4	CCP4

REGISTER 25-1: CCPxCON: CCPx CONTROL REGISTER

R/W-0/0	U-0	R-x	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	OUT	FMT	MODE<3:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’

-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7 **EN:** CCP Module Enable bit
1 = CCP is enabled
0 = CCP is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **OUT:** CCPx Output Data bit (read-only)

bit 4 **FMT:** CCPW (pulse-width) Alignment bit
MODE = Capture mode:
Unused
MODE = Compare mode:
Unused
MODE = PWM mode:
1 = Left-aligned format
0 = Right-aligned format

bit 3-0 **MODE<3:0>:** CCPx Mode Select bits

MODE	Operating Mode	Operation	Set CCPxIF
11xx	PWM	PWM operation	Yes
1011	Compare	Pulse output; clear TMR1[2]	Yes
1010		Pulse output	Yes
1001		Clear output[1]	Yes
1000		Set output[1]	Yes
0111	Capture	Every 16th rising edge of CCPx input	Yes
0110		Every 4th rising edge of CCPx input	Yes
0101		Every rising edge of CCPx input	Yes
0100		Every falling edge of CCPx input	Yes
0011		Every edge of CCPx input	Yes
0010	Compare	Toggle output	Yes
0001		Toggle output; clear TMR1[2]	Yes
0000	Disabled		—

Note 1: The set and clear operations of the Compare mode are reset by setting MODE = 4’b0000 or EN = 0.
2: When MODE = 0001 or 1011, then the timer associated with the CCP module is cleared. TMR1 is the default selection for the CCP module, so it is used for indication purpose only.

26.1.5 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when T2PR is 255. The resolution is a function of the T2PR register value as shown by Equation 26-4.

EQUATION 26-4: PWM RESOLUTION

$$Resolution = \frac{log[4(T2PR + 1)]}{log(2)}\ bits$$

Note: If the pulse-width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 26-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	0.31 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	64	4	1	1	1	1
T2PR Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 26-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	0.31 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	64	4	1	1	1	1
T2PR Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

26.1.6 OPERATION IN SLEEP MODE

In Sleep mode, the T2TMR register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, T2TMR will continue from its previous state.

26.1.7 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (FOSC). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for additional details.

26.1.8 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the PWM registers to their Reset states.

34.3 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SPIxCON0<2:0>, SPIxCON1<7:4>, SPIxCON1<2:0>, and SPIxCON2<2:0>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Input, Output, and Slave Select Polarity
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on first/second edge of SCK)
- Clock Rate (Master mode only)
- Slave Select Mode (Master or Slave mode)
- MSB-First or LSB-First
- Receive/Transmit Modes
    - Full duplex
    - Receive-without-transmit
    - Transmit-without-receive
- Transfer Counter Mode (Transmit-without-receive mode)

34.3.1 ENABLING AND DISABLING THE SPI MODULE

To enable the serial peripheral, the SPI enable bit (EN in SPIxCON0) must be set. To reset or reconfigure SPI mode, clear the EN bit, re-initialize the SSPxCONx registers and then set the EN bit. Setting the EN bit enables the SPI inputs and outputs: SDI, SDO, SCK(out), SCK(in), SS(out), and SS(in). All of these inputs and outputs are steered by PPS, and thus must have their functions properly mapped to device pins to function (see **Section 19.0 "Peripheral Pin Select (PPS) Module"**). In addition, SS(out) and SCK(out) must have the pins they are steered to set as outputs (TRIS bits must be 0) in order to properly output. Clearing the TRIS bit of the SDO pin will cause the SPI module to always control that pin, but is not necessary for SDO functionality. (see **Section 34.3.5 "Input and Output Polarity Bits"**). Configurations selected by the following registers should not be changed while the EN bit is set:

- SPIxBAUD
- SPIxCON1
- SPIxCON0 (except to clear the EN bit)

Clearing the EN bit aborts any transmissions in progress, disables the setting of interrupt flags by hardware, and resets the FIFO occupancy (see **Section 34.3.3 "Transmit and Receive FIFOs"** for more FIFO details).

34.3.2 BUSY BIT

While a data transfer is in progress, the SPI module sets the BUSY bit of SPIxCON2. This bit can be polled by the user to determine the current status of the SPI module, and to know when a communication is complete. The following registers/bits should not be written by software while the BUSY bit is set:

- SPIxTCNTH/L
- SPIxTWIDTH
- SPIxCON2
- The CLRBF bit of SPIxSTATUS

Note:	It is also not recommended to read SPIxTCNTH/L while the BUSY bit is set, as the value in the registers may not be a reliable indicator of the Transfer Counter. Use the Transfer Count Zero Interrupt Flag (the TCZIF bit of SPIxINTF) to accurately determine that the Transfer Counter has reached zero.

34.4.3 TRANSFER COUNTER IN SLAVE MODE

In Slave Mode, the transfer counter will still decrement as data is shifted in and out of the SPI module, but it will not control data transfers. In addition, in slave mode, the BMODE bit along with the transfer counter is used to determine when the device should look for Slave Select faults. If BMODE = 0, the SSFLT bit will be set if Slave Select transitions from its active to inactive state during bytes of data, as well as if it transitions before the last bit sent during the final byte (if SPIx-TWIDTH≠0). If BMODE=1, the SSFLT bit will be set if Slave Select transitions from its active to inactive state before the final bit of each individual transfer is completed. Note that SSFLT does not have an associated interrupt, so it should be checked in software. An ideal time to do this is when the End of Slave Select Interrupt (EOSIF) is triggered (see **Section 34.8.3.3 “Start of Slave Select and End of Slave Select Interrupts”**).

34.5 Master mode

In master mode, the device controls the SCK line, and as such, initiates data transfers and determines when any slaves broadcast data onto the SPI bus.

Master mode of this device can be configured in four different modes, configured by the TXR and RXR bits:

- Full Duplex mode
- Receive Only mode
- Transmit Only mode
- Transfer Off mode

The modes are illustrated in Table 34-1, below:

TABLE 34-1: MASTER MODE TXR/RXR SETTINGS

	TXR = 1	**TXR = 0**
RXR = 1	Full Duplex Mode If BMODE = 1, transfer when RxFIFO is not full and TxFIFO is not empty If BMODE = 0, Transfer when RXFIFO is not full, TXFIFO is not empty, and the Transfer Counter is non-zero	Receive Only mode Transfer when RxFIFO is not full and the Transfer Counter is non-zero Transmitted data is either the top of the FIFO or the most recently received data
RXR = 0	Transmit Only Mode If BMODE = 1, transfer when TxFIFO is not empty If BMODE = 0, Transfer when TXFIFO is not empty and the Transfer Counter is non-zero Received data is not stored	No Transfers

34.6.3 SLAVE MODE SLAVE SELECT

In Slave mode, an external Slave Select Signal can be used to synchronize communication with the Master device. The Slave Select line is held in its inactive state (high by default) until the master device is ready to communicate. When the Slave Select transitions to its active state, the slave knows that a new transmission is starting.

When the Slave Select goes false at the end of the transmission the receive function of the selected SPI Slave device returns to the inactive state. The slave is then ready to receive a new transmission when the Slave Select goes True again.

The Slave Select signal is received on the $\overline{SS}$ input pin. This pin is remappable with the SPIxSSPPS register (see **Section 19.1 "PPS Inputs"**). When the input on this pin is true, transmission and reception are enabled, and the SDO pin is driven. When the input on this pin is false, the SDO pin is either tri-stated (if the TRIS bit associated with the SDO pin is set) or driven to the value of the LAT bit associated with the SDO pin (if the TRIS bit associated with the SDO pin is cleared). In addition, the SCK input is ignored.

If the SS input goes False, while a data transfer is still in progress, it is considered a slave select fault. The SSFLT bit of SPIxCON2 indicates whether such an event has occurred. The transfer counter value determines the number of bits in a valid data transfer (see **Section 34.4 "Transfer Counter"** for more details).

The Slave Select polarity is controlled by the SSP bit of SPIxCON1. When SSP is set (its default state), the Slave Select input is active-low, and when it is cleared, the Slave Select input is active-high.

The Slave Select for the SPI module is controlled by the SSET bit of SPIxCON2. When the bit is cleared (its default state), the slave select will act as described above. When the bit is set, the SPI module will behave as if the SS input was always in its active state.

Note:	When SSET is set, the effective SS(in) signal is always active. Hence, the SSFLT bit may be disregarded.

34.6.4 SLAVE MODE CLOCK CONFIGURATION

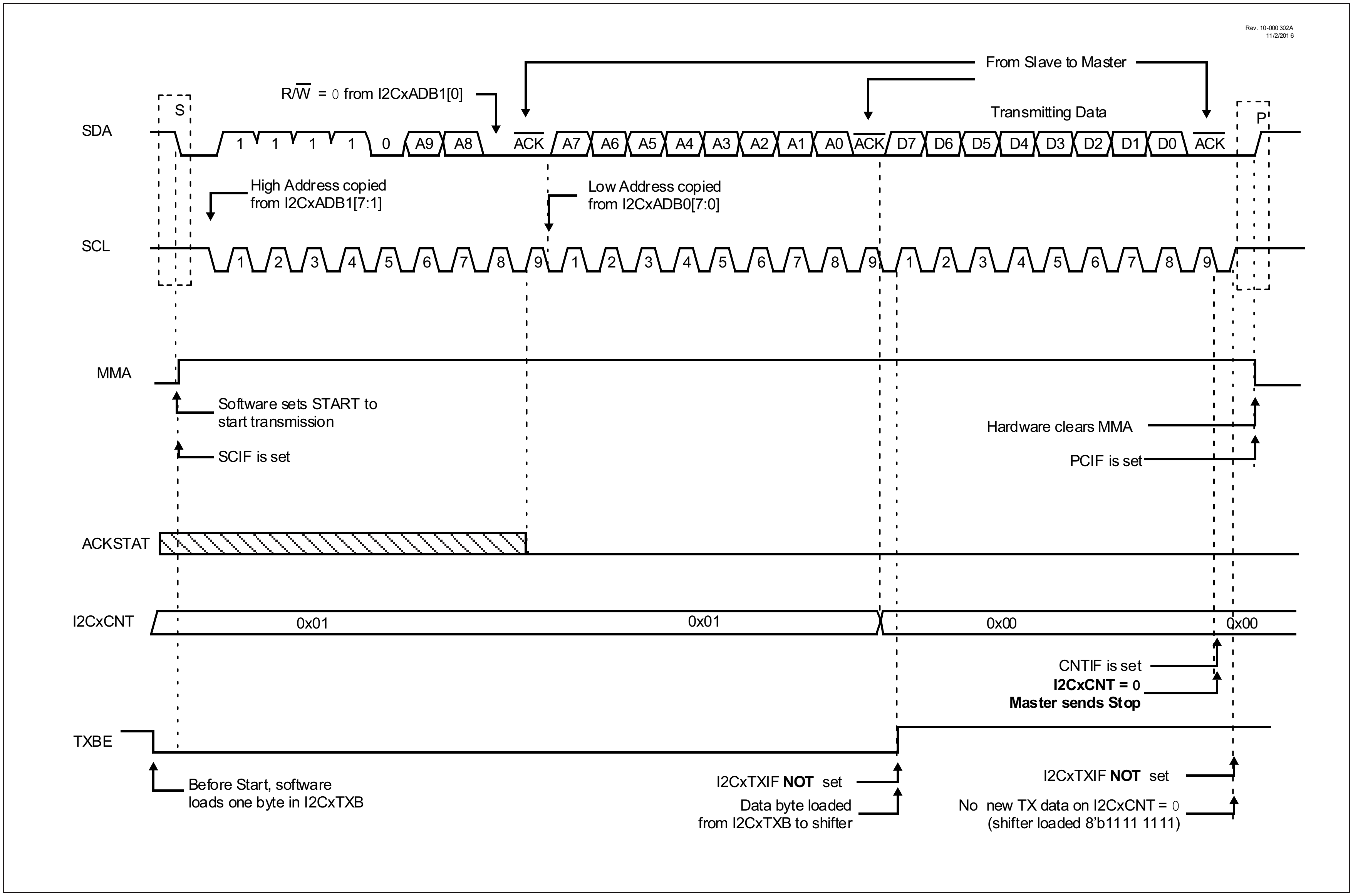
In Slave Mode, SCK is an input, and must be configured to the same polarity and clock edge as the master device. As in Master mode, the polarity of the clock input is controlled by the CKP bit of SPIxCON1 and the clock edge used for transmitting data is controlled by the CKE bit of SPIxCON1.

34.6.5 DAISY-CHAIN CONFIGURATION

The SPI bus can be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device connected to all slave devices (alternately, the slave devices can be configured to ignore the slave select line by setting the SSET bit). In a typical Daisy-Chain configuration, the SCK signal from the master is connected to each of the slave device SCK inputs. However, the SCK input and output are separate signals selected by the PPS control. When the PPS selection is made to configure the SCK input and SCK output on separate pins then, the SCK output will follow the SCK input, allowing for SCK signals to be daisy-chained like the SDO/SDI signals.

Figure 34-12 shows the block diagram of a typical daisy-chain connection, and Figure 30-13 shows the block diagram of a daisy-chain connection possible using this SPI module.

FIGURE 35-21: I^2C MASTER, 10-BIT ADDRESS, TRANSMISSION WITH STOP


Rev. 10-000302A
11/2/2016
From Slave to Master
R/W = 0 from I2CxADB1[0]
Transmitting Data
S
P
SDA
1 1 1 1 0 A9 A8 ACK A7 A6 A5 A4 A3 A2 A1 A0 ACK D7 D6 D5 D4 D3 D2 D1 D0 ACK
High Address copied from I2CxADB1[7:1]
Low Address copied from I2CxADB0[7:0]
SCL
1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9
MMA
Software sets START to start transmission
SCIF is set
Hardware clears MMA
PCIF is set
ACKSTAT
I2CxCNT
0x01
0x01
0x00
0x00
CNTIF is set
I2CxCNT = 0
Master sends Stop
TXBE
Before Start, software loads one byte in I2CxTXB
I2CxTXIF NOT set
Data byte loaded from I2CxTXB to shifter
I2CxTXIF NOT set
No new TX data on I2CxCNT = 0
(shifter loaded 8'b1111 1111)

Preliminary

ADDWFC ADD W and CARRY bit to f

Syntax:	ADDWFC f {,d {,a}}
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]
Operation:	(W) + (f) + (C) → dest
Status Affected:	N,OV, C, DC, Z
Encoding:	`0010` `00da` `ffff` `ffff`
Description:	Add W, the CARRY flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 43.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `ADDWFC REG, 0, 1`

Before Instruction

CARRY bit	=	1
REG	=	02h
W	=	4Dh

After Instruction

CARRY bit	=	0
REG	=	02h
W	=	50h

ANDLW AND literal with W

Syntax:	ANDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .AND. k → W
Status Affected:	N, Z
Encoding:	`0000` `1011` `kkkk` `kkkk`
Description:	The contents of W are AND'ed with the 8-bit literal 'k'. The result is placed in W.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example: `ANDLW 05Fh`

Before Instruction

W = A3h

After Instruction

W = 03h

TABLE 46-21: SPI MODE REQUIREMENTS

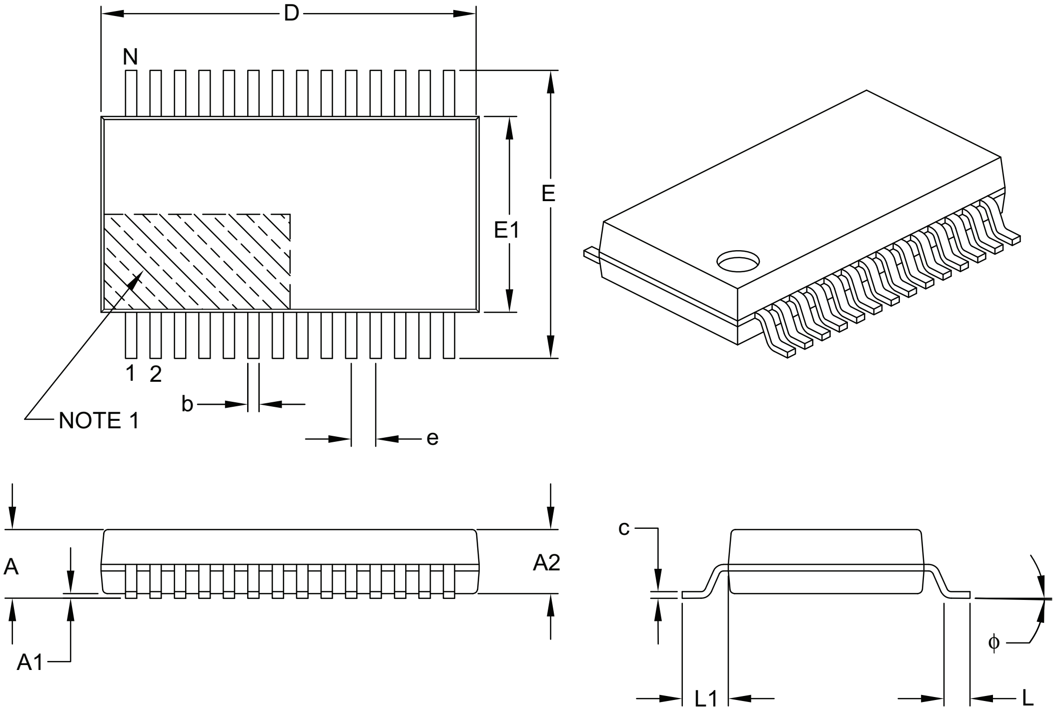
Standard Operating Conditions (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
SP70*	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input	2.25*Tcy	—	—	ns	
SP71*	TscH	SCK input high time (Slave mode)	Tcy + 20	—	—	ns	
SP72*	TscL	SCK input low time (Slave mode)	Tcy + 20	—	—	ns	
SP73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	—	ns	
SP74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
SP75*	TdoR	SDO data output rise time	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP76*	TdoF	SDO data output fall time	—	10	25	ns	
SP77*	TssH2doZ	$\overline{SS}$↑ to SDO output high-impedance	10	—	50	ns	
SP78*	TscR	SCK output rise time (Master mode)	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP79*	TscF	SCK output fall time (Master mode)	—	10	25	ns	
SP80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	3.0V ≤ VDD ≤ 5.5V
			—	—	145	ns	1.8V ≤ VDD ≤ 5.5V
SP81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	1 Tcy	—	—	ns	
SP82*	TssL2doV	SDO data output valid after $\overline{SS}$↓ edge	—	—	50	ns	
SP83*	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK edge	1.5 Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B