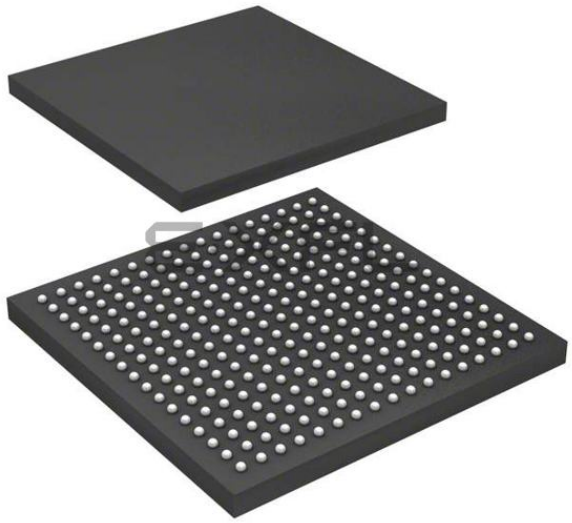

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Electrophoretic, LCD
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6y1dvm05aa

The i.MX 6ULL processors are specifically useful for applications such as:

- Telematics
- Audio playback
- Connected devices
- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Portable medical and health care
- IP phones
- Smart appliances
- eReaders

The features of the i.MX 6ULL processors include:

- Single-core Arm Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, an Electrophoretic Display (EPD) controller, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- 2x Ethernet interfaces—2x 10/100 Mbps Ethernet controllers.
- Human-machine interface—Each processor supports one digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: two high-speed USB on-the-go with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), two 12-bit ADC modules with up to 10 total input channels and two CAN ports.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, AES-128 encryption, SHA-1, SHA-256 HW acceleration engine, and secure software downloads. The security features are discussed in the *i.MX 6ULL Security Reference Manual* (IMX6ULLSRM).

  - Cortex-A7 NEON Media Processing Engine (MPE) Co-processor
- General Interrupt Controller (GIC) with 128 interrupts support
- Global Timer
- Snoop Control Unit (SCU)
- 128 KB unified I/D L2 cache
- Single Master AXI bus interface output of L2 cache
- Frequency of the core (including Neon and L1 cache), as per Table 10, "Operating Ranges," on page 24.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
  - 32 double-precision VFPv3 floating point registers

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia/shared, fast access RAM (OCRAM, 128 KB)
- External memory interfaces: The i.MX 6ULL processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
  - 16-bit LP-DDR2-800, 16-bit DDR3-800 and DDR3L-800
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bits.
  - 16/8-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.

Each i.MX 6ULL processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays:
  - One parallel display port, support max 85 MHz display clock and up to WXGA (1366 x 768) at 60 Hz
  - Support 24-bit, 18-bit, 16-bit, and 8-bit parallel display
  - Electrophoretic display controller support direct-driver for E-Ink EPD panel, with up to 2048x1536 resolution at 106 Hz
- Camera sensors:
  - One parallel camera port, up to 24 bit and 133.3 MHz pixel clock
  - Support 24-bit, 16-bit, 10-bit, and 8-bit input
  - Support BT.656 interface
- Expansion cards:
  - Two MMC/SD/SDIO card ports all supporting:

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6ULL processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6ULL processor system.

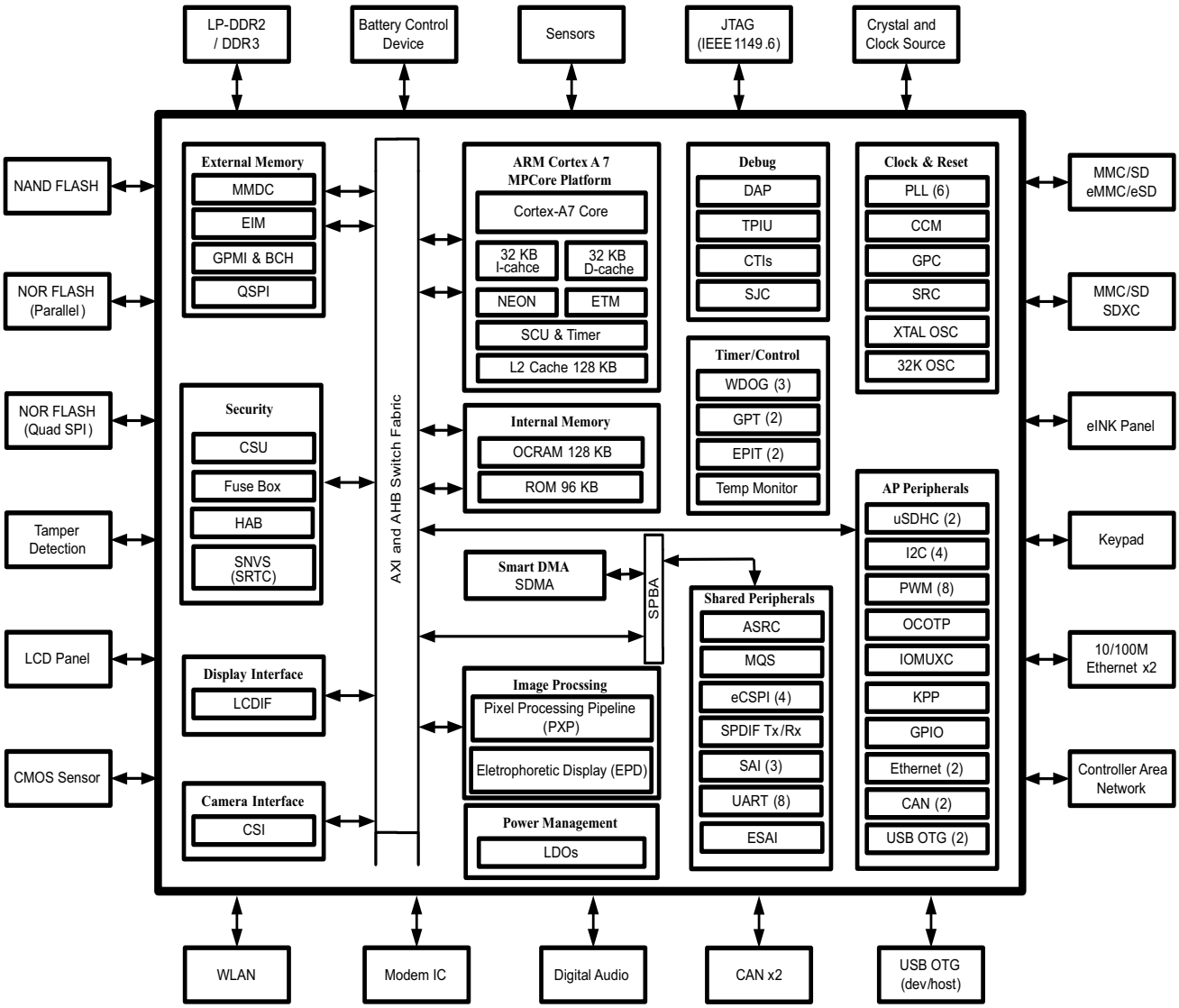

Figure 2. i.MX 6ULL System Block Diagram

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.
RNGB	Random Number Generator	Security	Random number generating module.
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6ULL processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments"." Signal descriptions are provided in the *i.MX 6ULL Reference Manual* (IMX6ULLRM).

Table 3. Special Signal Considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX 6ULL Reference Manual* (IMX6ULLRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused, either or both of the CLK1_N/P pairs may remain unconnected.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required, system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI is not connected. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when two DDR3 ICs plus the i.MX 6ULL are drawing current on the resistor divider.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused
CCM	CCM_CLK1_N, CCM_CLK1_P	Not connect
USB	USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS	Not connect
ADC	ADC_VREFH	Tie to VDDA_ADC_3P3
	VDDA_ADC_3P3	VDDA_ADC_3P3 must be powered even if the ADC is not used.

Table 42. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see 2]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see 2]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see 2]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see 2]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see 2]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see 3,2]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see 2]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see 2]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see 2]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see 5,6]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see 5,6]	—	ns

1 GPMI's Async Mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is guaranteed by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 24), NF16/NF17 is different from the definition in non-EDO mode (Figure 23). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 6ULL Reference Manual*). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 26 to Figure 28 show the write and read timing of Source Synchronous Mode.

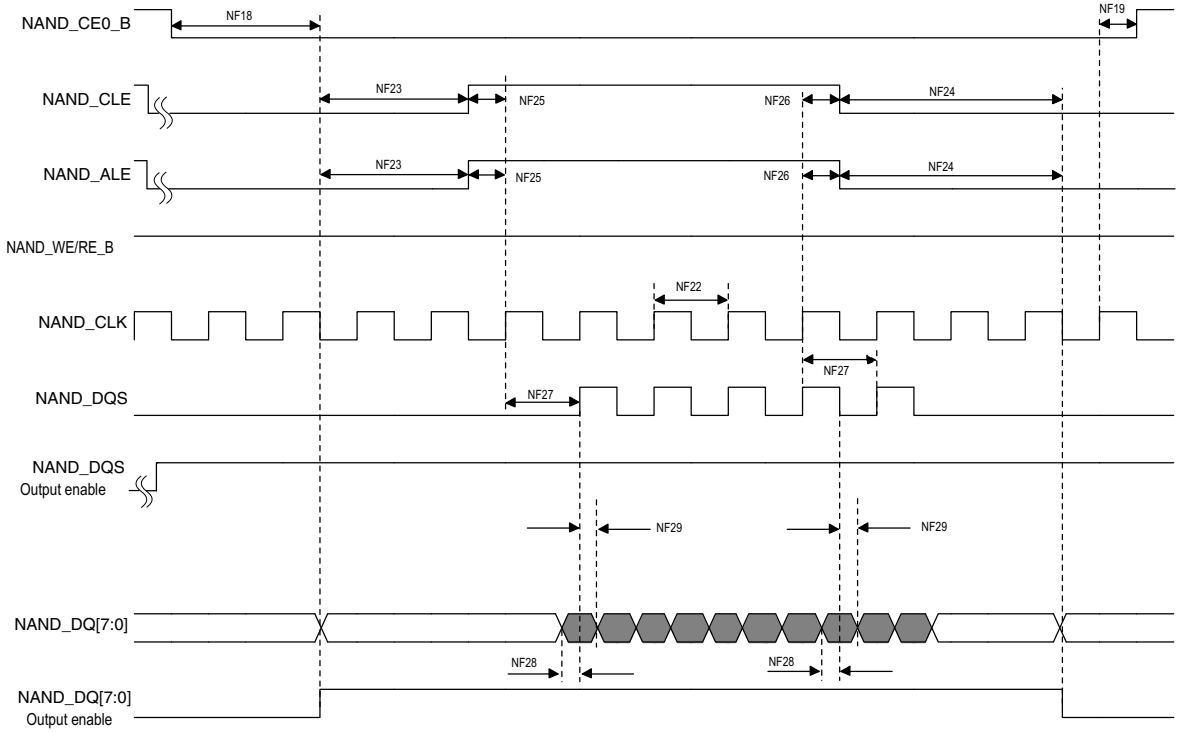

Figure 27. Source Synchronous Mode Data Write Timing Diagram

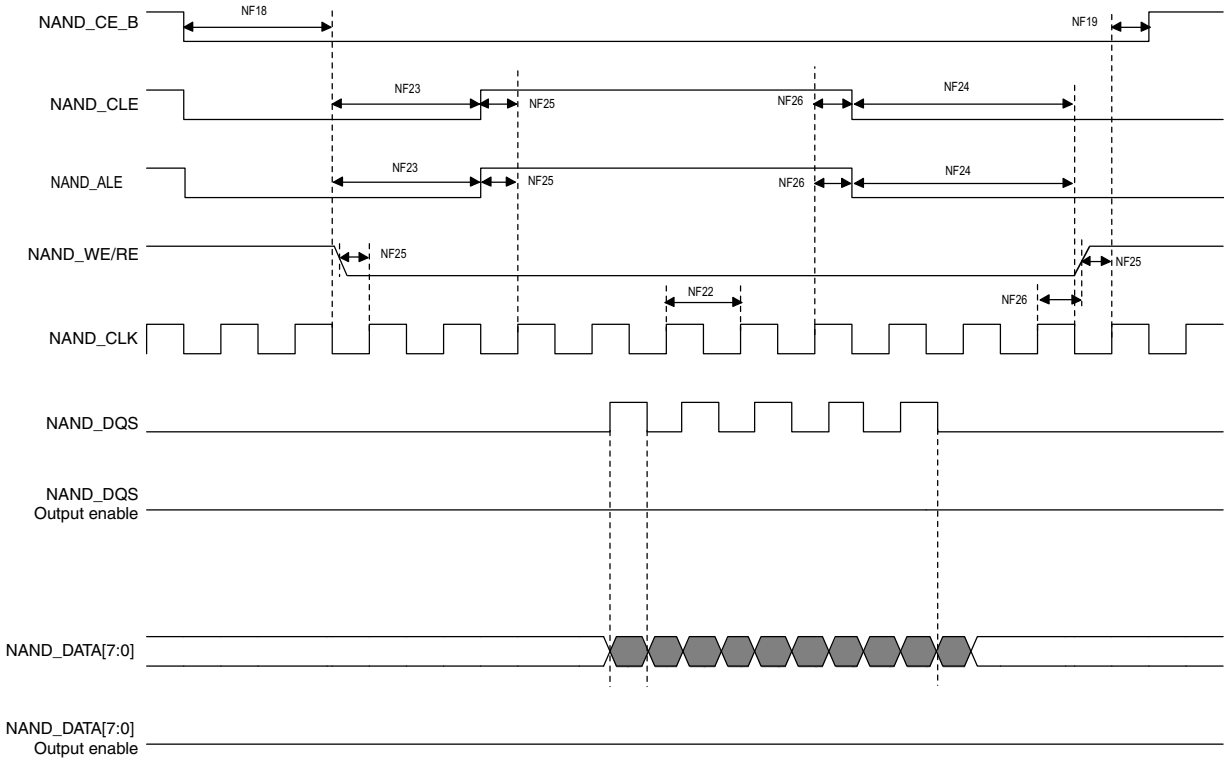

Figure 28. Source Synchronous Mode Data Read Timing Diagram

Figure 48 shows RMII mode timings. Table 58 describes the timing parameters (M16–M21) shown in the figure.

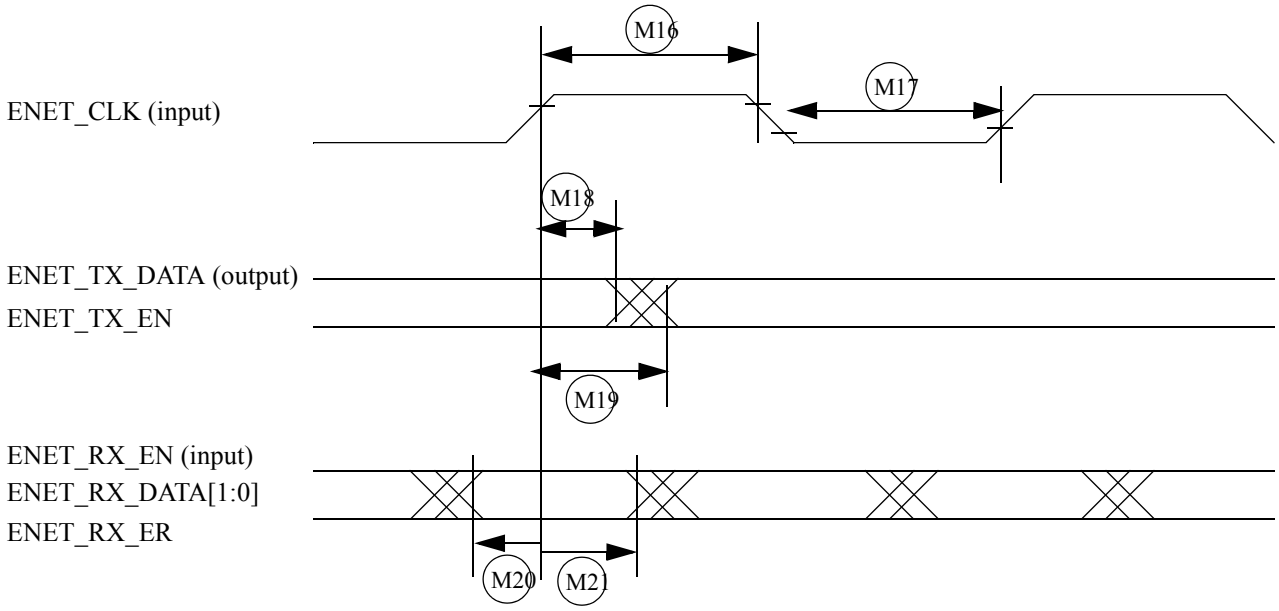

Figure 48. RMII Mode Signal Timing Diagram

Table 58. RMII Signal Timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	13	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	2	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.12.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6ULL Reference Manual* (IMX6ULLRM) to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.12.10 QUAD SPI (QSPI) Timing Parameters

Measurement conditions are with 35 pF load on SCK and SIO pins and input slew rate of 1 V/ns.

4.12.10.1 SDR Mode

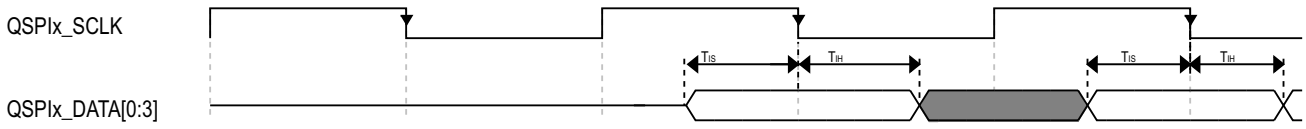

Figure 51. QuadSPI Input/Read Timing (SDR mode with internal sampling)

Table 62. QuadSPI Input Timing (SDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

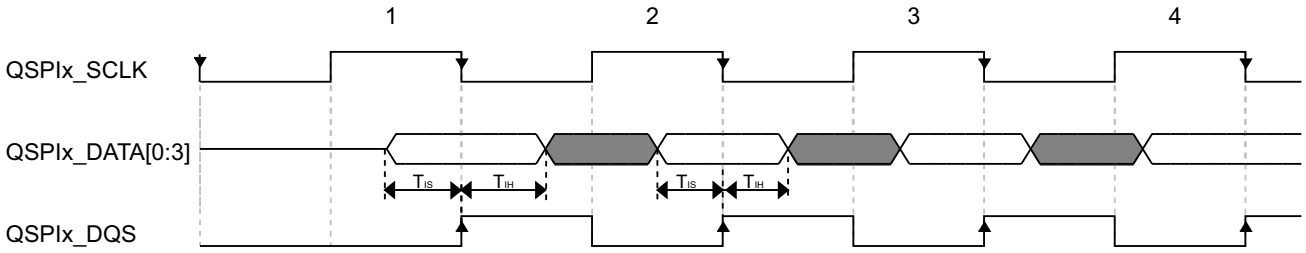

Figure 52. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Table 63. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

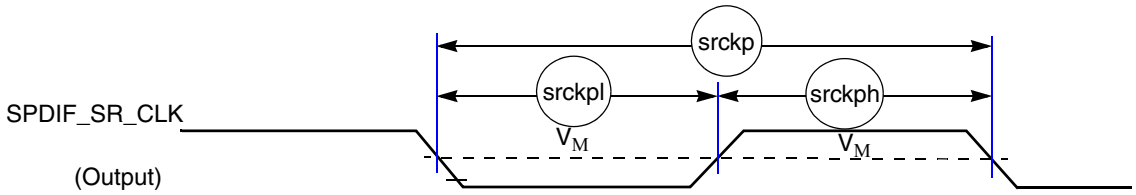

Figure 63. SPDIF_SR_CLK Timing Diagram

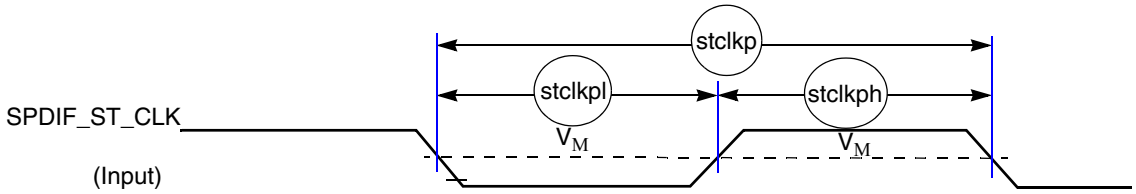

Figure 64. SPDIF_ST_CLK Timing Diagram

4.12.14 UART I/O Configuration and Timing Parameters

4.12.14.1 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.14.1.1 UART Transmitter

Figure 65 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 72 lists the UART RS-232 serial mode transmits timing characteristics.

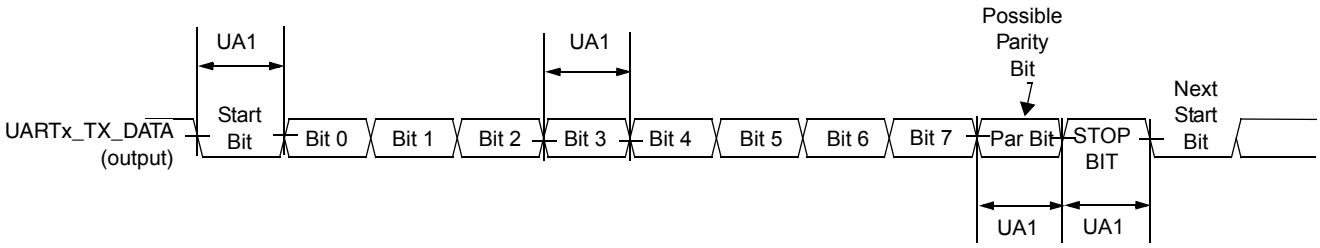

Figure 65. UART RS-232 Serial Mode Transmit Timing Diagram

Table 72. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.
2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 68 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 75 lists the receive timing characteristics.

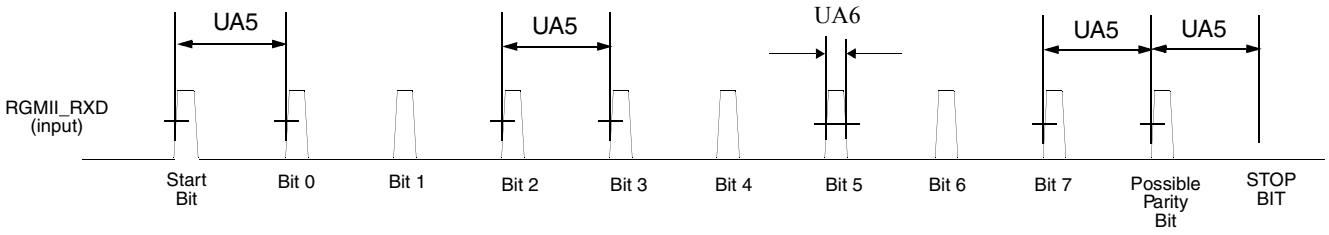

Figure 68. UART IrDA Mode Receive Timing Diagram

Table 75. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.
2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.15 USB PHY Parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0

Table 76. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	—	40	MHz	—
	ADLPC=0, ADHSC=0 12 bit mode		4	—	30	MHz	—
	ADLPC=1, ADHSC=0 12 bit mode		4	—	20	MHz	—

1 Typical values assume VDDAD = 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential differences

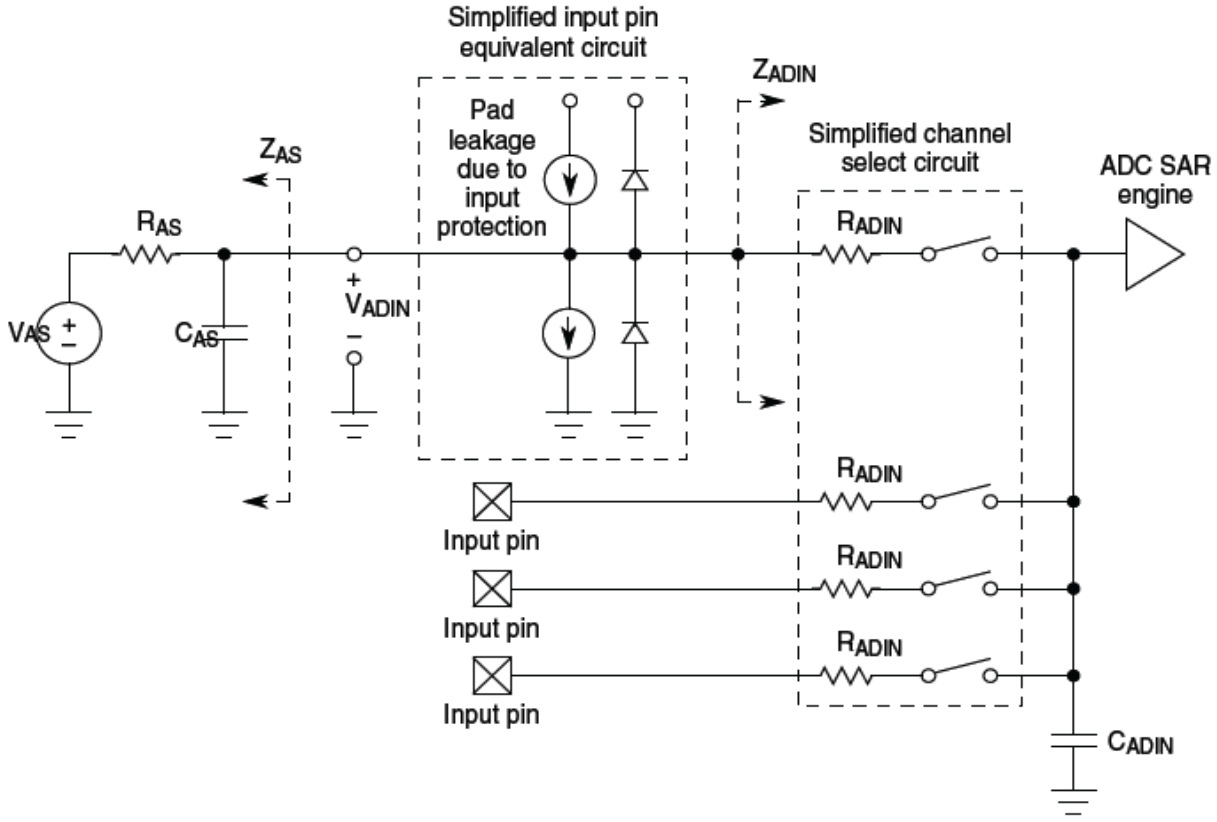

Figure 69. 12-bit ADC Input Impedance Equivalency Diagram

Table 77. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
[P:][C:] Integral Non-Linearity	12 bit mode	INL	—	2.6	—	LSB	—
	10bit mode		—	0.8	—		
	8 bit mode		—	0.3	—		
Zero-Scale Error	12 bit mode	E_{ZS}	—	-0.3	—	LSB	—
	10bit mode		—	-0.15	—		
	8 bit mode		—	-0.15	—		
Full-Scale Error	12 bit mode	E_{FS}	—	-2.5	—	LSB	—
	10bit mode		—	-0.6	—		
	8 bit mode		—	-0.3	—		
[L:] Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	—	Bits	—
[L:] Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	—

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

2 Typical values assume V_{DDAD} = 3.0 V, Temp = 25°C, F_{adck}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 78 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6ULL Fuse Map document and the System Boot chapter in *i.MX 6ULL Reference Manual (IMX6ULLRM)*.

Table 78. Fuses and Associated Pins Used for Boot

Pin	Direction at reset	eFuse name	Details
BOOT_MODE0	Input with 100 K pull-down	N/A	Boot mode selection
BOOT_MODE1	Input with 100 K pull-down	N/A	Boot mode selection

Table 81. SPI Boot through ECSPI2 (continued)

LCD_VSYNC	ecspi2.SS2	Alt 8				Yes	
LCD_RESET	ecspi2.SS3	Alt 8					Yes

Table 82. SPI Boot through ECSPI3

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4[5:4]=01b	BOOT_CFG4[5:4]=10b	BOOT_CFG4 [5:4]=11b
UART2_RTS_B	ecspi3.MISO	Alt 8	Yes				
UART2_CTS_B	ecspi3.MOSI	Alt 8	Yes				
UART2_RX_DATA	ecspi3.SCLK	Alt 8	Yes				
UART2_TX_DATA	ecspi3.SS0	Alt 8		Yes			
NAND_ALE	ecspi3.SS1	Alt 8			Yes		
NAND_RE_B	ecspi3.SS2	Alt 8				Yes	
NAND_WE_B	ecspi3.SS3	Alt 8					Yes

Table 83. SPI Boot through ECSPI4

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4[5:4]=01b	BOOT_CFG4[5:4]=10b	BOOT_CFG 4[5:4]=11b
ENET2_TX_CLK	ecspi4.MISO	Alt 3	Yes				
ENET2_TX_EN	ecspi4.MOSI	Alt 3	Yes				
ENET2_TX_DATA1	ecspi4.SCLK	Alt 3	Yes				
ENET2_RX_ER	ecspi4.SS0	Alt 3		Yes			
NAND_DATA01	ecspi4.SS1	Alt 8			Yes		
NAND_DATA02	ecspi4.SS2	Alt 8				Yes	
NAND_DATA03	ecspi4.SS3	Alt 8					Yes

Table 84. NAND Boot through GPMI

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_CLE	rawnand.CLE	Alt 0	Yes		
NAND_ALE	rawnand.ALE	Alt 0	Yes		
NAND_WP_B	rawnand.WP_B	Alt 0	Yes		
NAND_READY_B	rawnand.READY_B	Alt 0	Yes		
NAND_CE0_B	rawnand.CE0_B	Alt 0	Yes		
NAND_CE1_B	rawnand.CE1_B	Alt 0		Yes	Yes
NAND_RE_B	rawnand.RE_B	Alt 0	Yes		

Table 87. NOR/OneNAND Boot through EIM (continued)

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
CSI_PIXCLK	weim.OE	Alt 4	Yes		
CSI_VSYNC	weim.RW	Alt 4	Yes		

Table 88. Serial Download through UART1

Ball Name	Signal Name	Mux Mode	Common
UART1_TX_DATA	uart1.TX_DATA	Alt 0	Yes
UART1_RX_DATA	uart1.RX_DATA	Alt 0	Yes

Table 89. Serial Download through UART2

Ball Name	Signal Name	Mux Mode	Common
UART2_TX_DATA	uart2.TX_DATA	Alt 0	Yes
UART2_RX_DATA	uart2.RX_DATA	Alt 0	Yes

Table 91 shows an alpha-sorted list of functional contact assignments for the 14 x 14 mm package.

Table 91. 14 x 14 mm Functional Contact Assignments

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
BOOT_MODE0	T10	VDD_SNVS_IN	GPIO	ALT5	GPIO5_IO10	Input	100 kΩ pull-down
BOOT_MODE1	U10	VDD_SNVS_IN	GPIO	ALT5	GPIO5_IO11	Input	100 kΩ pull-down
CCM_CLK1_N	P16	VDD_HIGH_CAP	CCM	—	CCM_CLK1_N	—	—
CCM_CLK1_P	P17	VDD_HIGH_CAP	CCM	—	CCM_CLK1_P	—	—
CCM_PMIC_STBY_REQ	U9	VDD_SNVS_IN	CCM	ALT0	CCM_PMIC_VSTBY_REQ	Output	—
CSI_DATA00	E4	NVCC_CSI	GPIO	ALT5	GPIO4_IO21	Input	Keeper
CSI_DATA01	E3	NVCC_CSI	GPIO	ALT5	GPIO4_IO22	Input	Keeper
CSI_DATA02	E2	NVCC_CSI	GPIO	ALT5	GPIO4_IO23	Input	Keeper
CSI_DATA03	E1	NVCC_CSI	GPIO	ALT5	GPIO4_IO24	Input	Keeper
CSI_DATA04	D4	NVCC_CSI	GPIO	ALT5	GPIO4_IO25	Input	Keeper
CSI_DATA05	D3	NVCC_CSI	GPIO	ALT5	GPIO4_IO26	Input	Keeper
CSI_DATA06	D2	NVCC_CSI	GPIO	ALT5	GPIO4_IO27	Input	Keeper
CSI_DATA07	D1	NVCC_CSI	GPIO	ALT5	GPIO4_IO28	Input	Keeper
CSI_HSYNC	F3	NVCC_CSI	GPIO	ALT5	GPIO4_IO20	Input	Keeper
CSI_MCLK	F5	NVCC_CSI	GPIO	ALT5	GPIO4_IO17	Input	Keeper
CSI_PIXCLK	E5	NVCC_CSI	GPIO	ALT5	GPIO4_IO18	Input	Keeper
CSI_VSYNC	F2	NVCC_CSI	GPIO	ALT5	GPIO4_IO19	Input	Keeper
DRAM_ADDR00	L5	NVCC_DRAM	MMDC	ALT0	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	H2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	100 kΩ pull-up
DRAM_ADDR02	K1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	100 kΩ pull-up
DRAM_ADDR03	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	100 kΩ pull-up
DRAM_ADDR04	K4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	100 kΩ pull-up
DRAM_ADDR05	L1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	100 kΩ pull-up
DRAM_ADDR06	G2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	100 kΩ pull-up

Table 91. 14 x 14 mm Functional Contact Assignments (continued)

DRAM_ADDR07	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	L2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	M4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	K3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	L4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	H3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	G1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	100 kΩ pull-up
DRAM_ADDR15	K5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	100 kΩ pull-up
DRAM_CAS_B	J2	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	100 kΩ pull-up
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	100 kΩ pull-up
DRAM_CS1_B	H5	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	100 kΩ pull-up
DRAM_DATA00	T4	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_DATA01	U6	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_DATA02	T6	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_DATA03	U7	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_DATA04	U8	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_DATA05	T8	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_DATA06	T5	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_DATA07	U4	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_DATA08	U2	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up

Table 95. 9x9 mm, 0.5 mm Pitch, Ball Map (continued)

P	N	M	L	K	J	H
DRAM_DATA08	DRAM_DATA14	VSS	DRAM_CS0_B	DRAM_SDCKE1	DRAM_ADDR09	DRAM_ADDR02
DRAM_DATA15	DRAM_DATA13	DRAM_ADDR10	DRAM_SDCKE0	DRAM_ODT0	DRAM_ADDR03	DRAM_ADDR05
DRAM_DATA10	DRAM_SDQS1_P	VSS	DRAM_ADDR12	DRAM_SDCLK0_P	VSS	DRAM_SDBA0
DRAM_DATA12	DRAM_SDQS1_N	DRAM_ADDR04	DRAM_RAS_B	DRAM_SDCLK0_N	DRAM_ADDR07	DRAM_ADDR13
DRAM_SDQS0_P	DRAM_DATA01	NVCC_DRAM	NVCC_DRAM	DRAM_ADDR11	DRAM_ADDR08	DRAM_CSI_B
SNVS_TAMPER1	NVCC_DRAM			NVCC_DRAM_2P5		VSS
SNVS_TAMPER4	TEST_MODE		VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER5	SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER9	SNVS_TAMPER7		VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER3	SNVS_DAMPER2	NGND_KEL0	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
USB_OTG1_DP	VDD_USB_CAP		VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
VDD_SNVS_IN	VDD_SNVS_CAP			VSS		VSS
JTAG_TRST_B	ADC_VREFH	NVCC_GPIO	NVCC_UART	UART5_TX_DATA	UART5_RX_DATA	ENET2_RX_ER
GPIO1_IO08	GPIO1_IO07	GPIO1_IO00	UART1_CTS_B	UART1_RTS_B	UART2_RTS_B	ENET2_TX_CLK
GPIO1_IO05	GPIO1_IO06	GPIO_IO01	UART1_TX_DATA	UART3_RX_DATA	VSS	UART3_RTS_B
GPIO1_IO09	GPIO1_IO03	GPIO1_IO02	UART2_TX-DATA	UART2_RX_DATA	UART4_TX_DATA	UART3_CTS_B
JTAG_TDI	GPIO1_IO04	VSS	UART1_RX_DATA	UART3_TX_DATA	UART2_CTS_B	UART4_RX_DATA
P	N	M	L	K	J	H