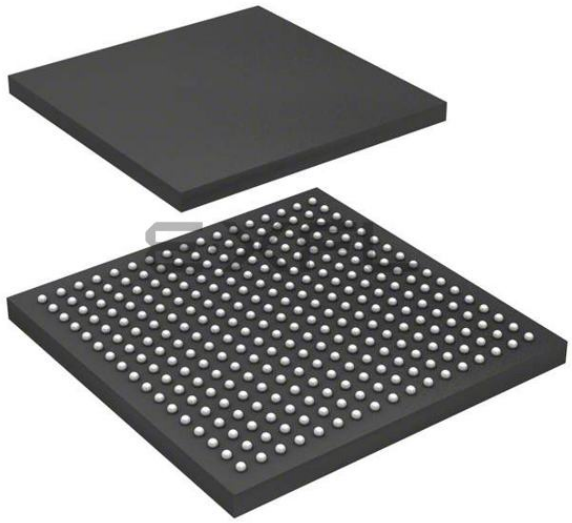

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Electrophoretic, LCD
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6y1dvm05ab

The i.MX 6ULL processors are specifically useful for applications such as:

- Telematics
- Audio playback
- Connected devices
- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Portable medical and health care
- IP phones
- Smart appliances
- eReaders

The features of the i.MX 6ULL processors include:

- Single-core Arm Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, an Electrophoretic Display (EPD) controller, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- 2x Ethernet interfaces—2x 10/100 Mbps Ethernet controllers.
- Human-machine interface—Each processor supports one digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: two high-speed USB on-the-go with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), two 12-bit ADC modules with up to 10 total input channels and two CAN ports.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, AES-128 encryption, SHA-1, SHA-256 HW acceleration engine, and secure software downloads. The security features are discussed in the *i.MX 6ULL Security Reference Manual* (IMX6ULLSRM).

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6ULL features, see Section 1.2, “Features"”.

1.1 Ordering Information

Table 1 provides examples of orderable part numbers covered by this data sheet.

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6Y0DVM05AA MCIMX6Y0DVM05AB	Features supports: • 528 MHz, commercial grade for general purpose • No security • No LCD/CSI • No CAN • Ethernet x1 • USB OTG x1 • ADC x1 • UART x4 • SAI x1 • No ESAI • Timer x2 • PWM x4 • I2C x2 • SPI x2	14 x 14 mm, 0.8 pitch MAPBGA	0 to +95
MCIMX6Y1DVM05AA MCIMX6Y1DVM05AB	Features supports: • 528 MHz, commercial grade for general purpose • Basic security • No LCD/CSI • CAN x1 • Ethernet x1 • USB OTG x2 • ADC x1 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	14 x 14 mm, 0.8 pitch MAPBGA	0 to +95

The i.MX 6ULL processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6ULL processors incorporate the following hardware accelerators:

- PXP—Pixel Processing Pipeline for image resize, rotation, overlay and CSC. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- Arm TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock, both active tamper and passive tamper detection logic has up to 10 tamper inputs. Voltage monitor, temperature monitor, and clock frequency monitor protects the secure key storage.
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: AES-128 encryption, SHA-1, and SHA-256 HW acceleration engine, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1. Functions, such as display and camera interfaces, connectivity interfaces.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
GPANAIO	This signal is reserved for NXP manufacturing use only. This output must remain unconnected.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6ULL reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be disconnected by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.
TEST_MODE	TEST_MODE is for NXP factory use. The user must tie this pin directly to GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6ULL processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6ULL Chip-Level Conditions

For these characteristics	Topic appears
Absolute Maximum Ratings	on page 22
Thermal Resistance	on page 22
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximum Supply Currents	on page 27
Power Modes	on page 28
USB PHY Current Consumption	on page 31

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core Supply Voltage	VDDSOC_IN	-0.3	1.6	V
Internal Supply Voltage	VDDARM_CAP VDDSOC_CAP	-0.3	1.4	V
GPIO Supply Voltage	NVCC_CSI NVCC_ENET NVCC_GPIO NVCC_UART NVCC_LCD NVCC_NAND NVCC_SD1	-0.5	3.7	V
DDR IO Supply Voltage	NVCC_DRAM	-0.4	1.975[1]	V
VDD_SNVS_IN Supply Voltage	VDD_SNVS_IN	-0.3	3.6	V
VDDHIGH_IN Supply voltage	VDD_HIGH_IN	-0.3	3.7	V
USB VBUS	USB_OTG1_VBUS USB_OTG2_VBUS	—	5.5	V
Input voltage on USB_OTG_DP and USB_OTG_DN pins	USB_OTG1_DP/USB_OTG1_DN USB_OTG2_DP/USB_OTG2_DN	-0.3	3.63	V
Input/Output Voltage Range	$V_{in/Vout}$	-0.5	OVDD+0.3[2]	V
ESD damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	Vesd	 — —	 2000 500	V
Storage Temperature Range	TSTORAGE	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575 V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 14 x 14 mm (VM) Package Thermal Resistance

Table 8 displays the 14 x 14 mm (VM) package thermal resistance data.

Table 8. 14 x 14 (VM) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural convection	Single-layer board (1s)	$R_{\theta JA}$	58.4	°C/W	1,2
Junction to Ambient Natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	37.6	°C/W	1,2,3

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the *i.MX 6ULL Power Consumption Measurement Application Note (AN4581)* or examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Power Modes

The i.MX 6ULL has the following power modes:

- RUN Mode: CPU is active, some portion of the chip can be clock gated or power gated. Support multiple voltage/frequency scaling set point for power saving;
- Low Power Mode: CPU in WFI state or power gate, some portion of the chip can be shut off for power saving. The Suspend, Low Power Idle, System Idle are consider as sub-modes of the RUN mode;
- SNVS Mode: only RTC and tamper detection logic is active, with 12 GPIOs in low power state retention mode;
- OFF Mode: all power rails are off.

The following table summarizes the external power supply state in all the power modes.

Table 14. Power Supply State in Power Modes

Power Rail	RUN	Low Power	SNVS	OFF
VDD_SOC_IN	ON	ON	OFF	OFF
VDD_HIGH_IN	ON	ON	OFF	OFF
VDD_SNVS	ON	ON	ON	OFF
USB_OTG1_VBUS USB_OTG2_VBUS	ON / OFF	ON / OFF	OFF	OFF
NVCC_DRAM_2P5	ON	ON	OFF	OFF
VDDA_ADC_3P3	ON / OFF	ON / OFF	OFF	OFF
NVCC_DRAM	ON	ON	OFF	OFF
NVCC_XXX	ON / OFF	ON / OFF	OFF	OFF

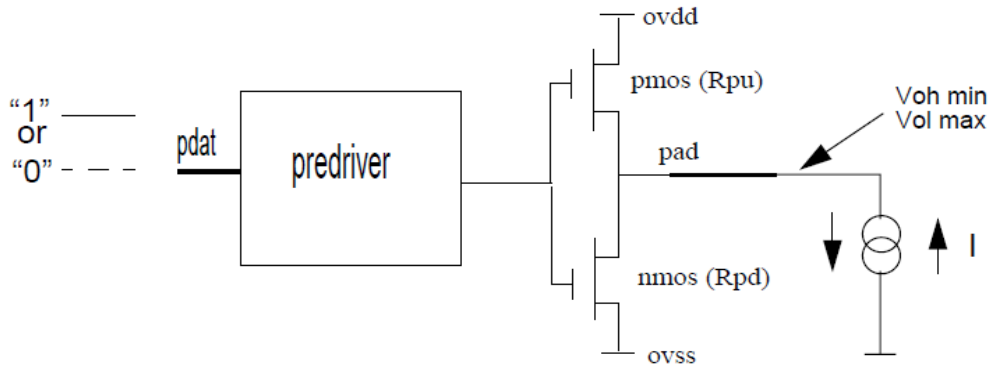

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 23 shows the DC parameters for the clock inputs.

Table 23. XTALI and RTC_XTALI DC Parameters [1]

Parameter	Symbol	Test Conditions	Min	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL	NVCC_PLL	V
XTALI low-level DC input voltage	Vil	—	0	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	1.1	V
RTC_XTALI low-level DC input voltage	Vil	—	0	0.2	V

[1] The DC parameters are for external clock input only.

4.6.2 Single Voltage General Purpose I/O (GPIO) DC Parameters

Table 24 shows DC parameters for GPIO pads. The parameters in Table 24 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 24. Single Voltage GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Ioh= -0.1mA (ipp_dse=001,010) Ioh= -1mA (ipp_dse=011,100,101,110,111)	OVDD-0.15	–	V
Low-level output voltage[1]	VOL	Iol= 0.1mA (ipp_dse=001,010) Iol= 1mA (ipp_dse=011,100,101,110,111)	–	0.15	V
High-Level input voltage[1,2]	VIH	—	0.7 x OVDD	OVDD	V
Low-Level input voltage[1,2]	VIL	—	0	0.3 x OVDD	V
Input Hysteresis (OVDD= 1.8V)	VHYS_LowVDD	OVDD=1.8V	200	—	mV
Input Hysteresis (OVDD=3.3V	VHYS_HighVDD	OVDD=3.3V	200	—	mV

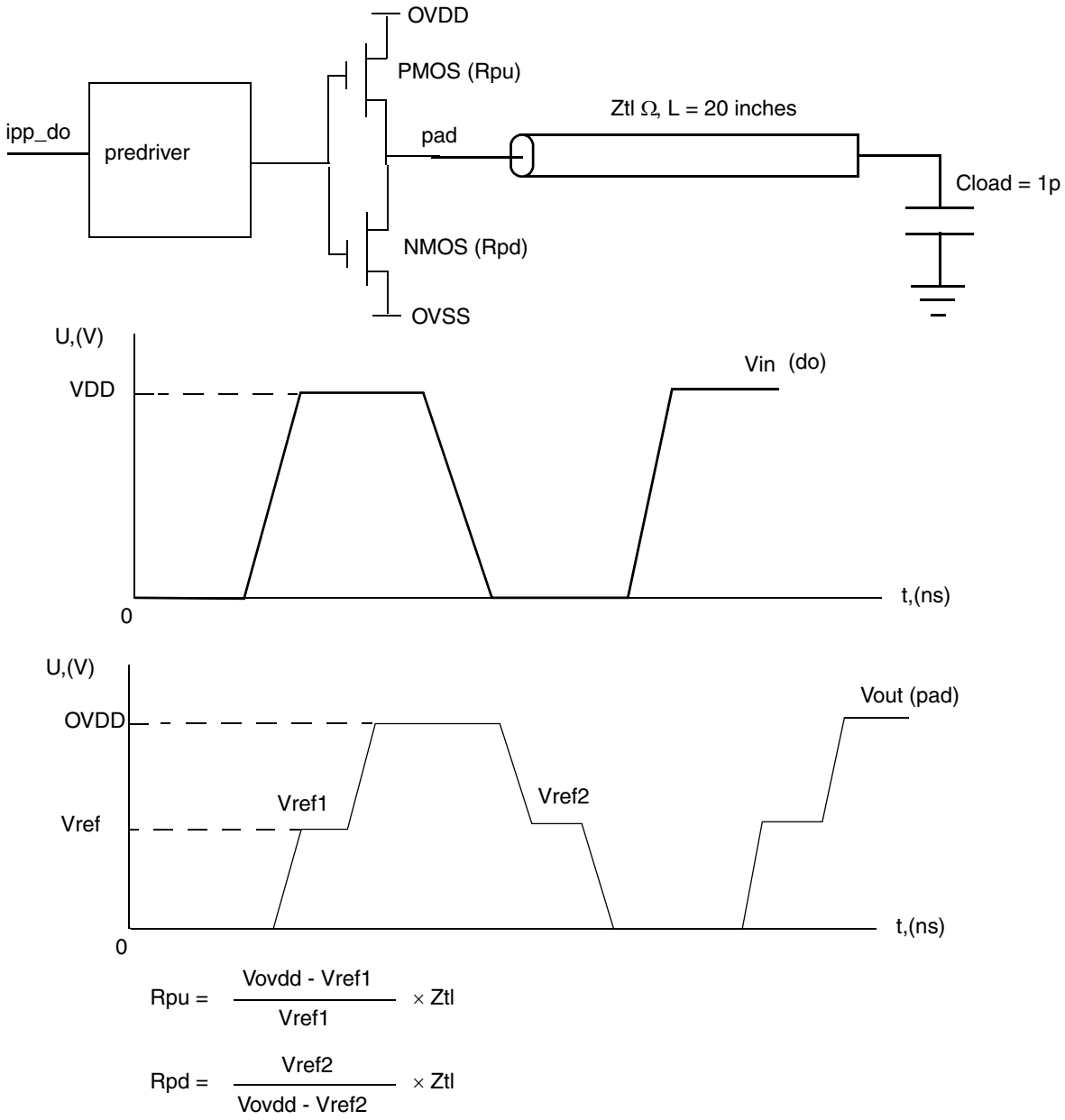

Figure 6. Impedance Matching Load for Measurement

4.8.1 Single Voltage GPIO Output Buffer Impedance

Table 33 shows the GPIO output buffer impedance (OVDD 1.8 V).

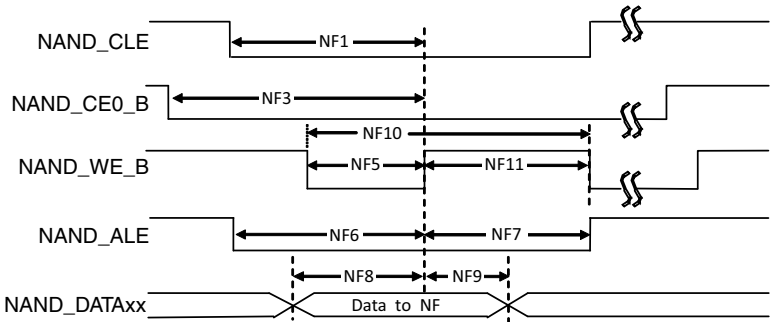

Figure 23. Write Data Latch Cycle Timing Diagram

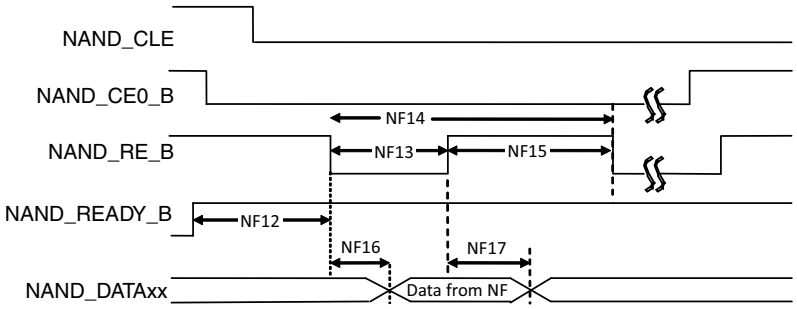

Figure 24. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

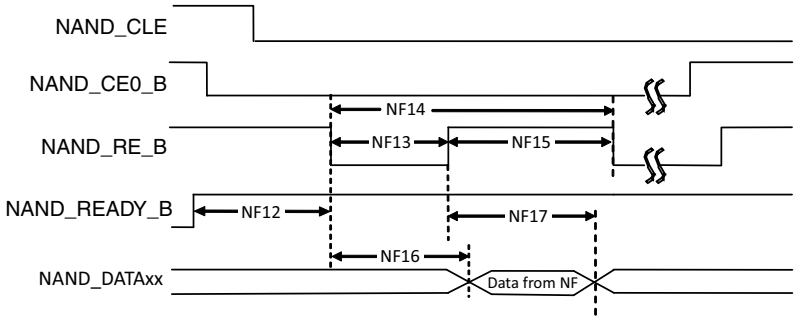

Figure 25. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 42. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		ns
NF3	NAND_CE0_B setup time	tCS	(AS + DS + 1) × T [see 3,2]		ns
NF4	NAND_CE0_B hold time	tCH	(DH+1) × T - 1 [see 2]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		ns

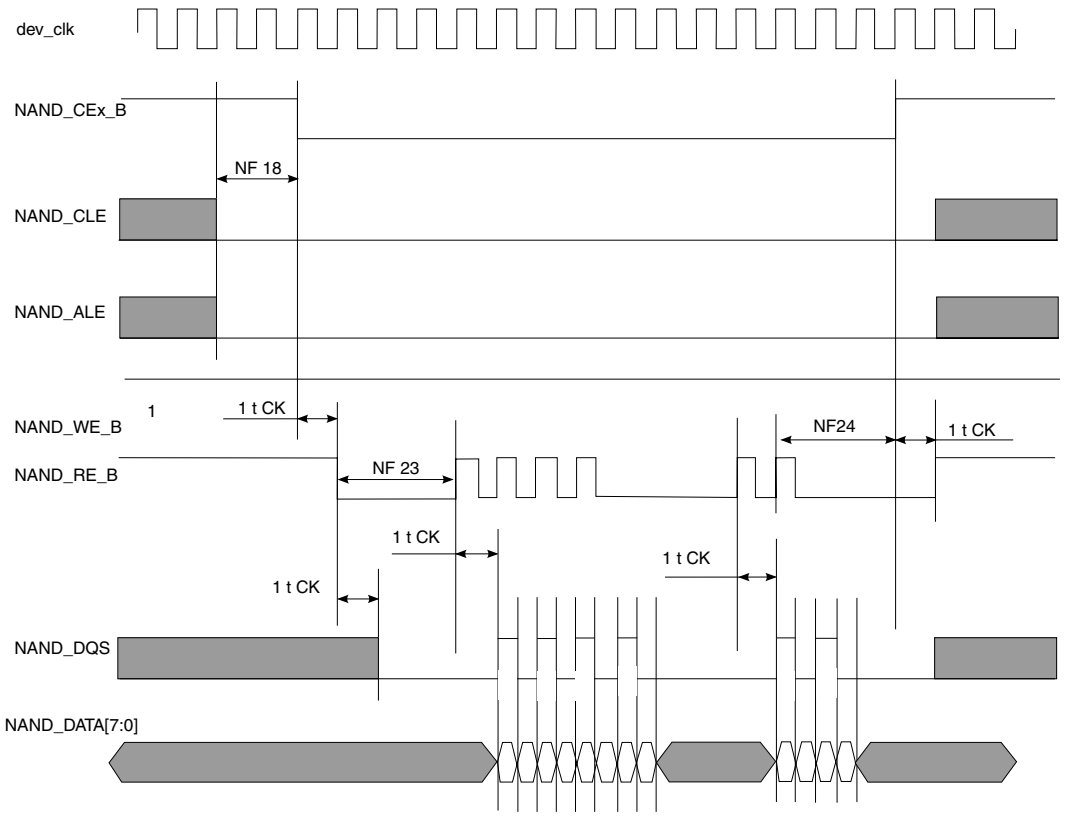

Figure 31. Samsung Toggle Mode Data Read Timing

Table 44. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see [2,3]]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see [2]]		—
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see [3,2]]		—
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see [2]]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see [2]]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see [3,2]]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see [2]]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see [2]]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see [2]]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see [4,2]]	—	ns
NF22	clock period	tCK	—	—	ns

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

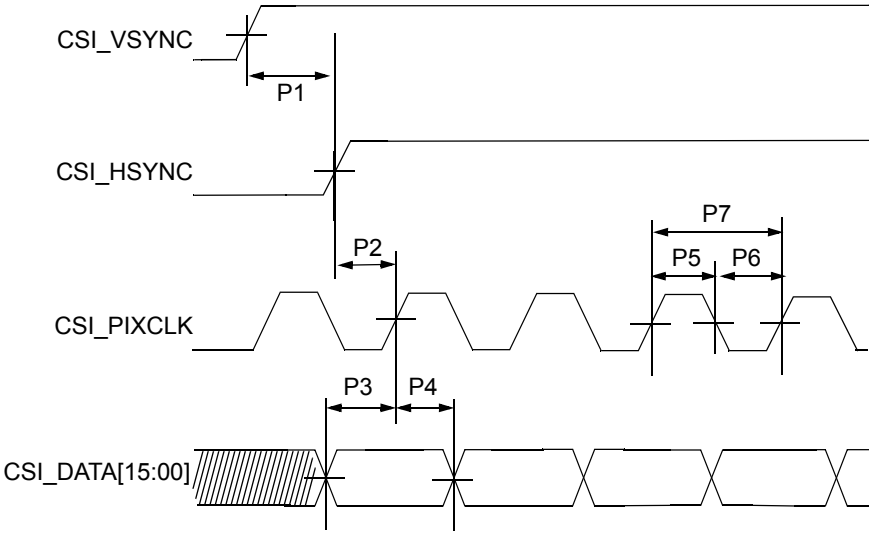

Figure 32. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

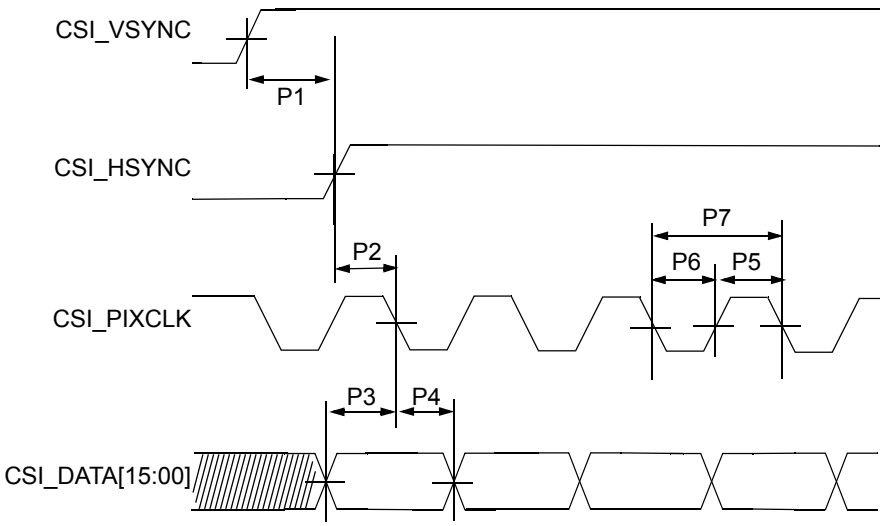

Figure 33. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 45. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns

4.12.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.12.2.1 ECSPI Master Mode Timing

Figure 35 depicts the timing of ECSPI in master mode. Table 47 lists the ECSPI master mode timing characteristics.

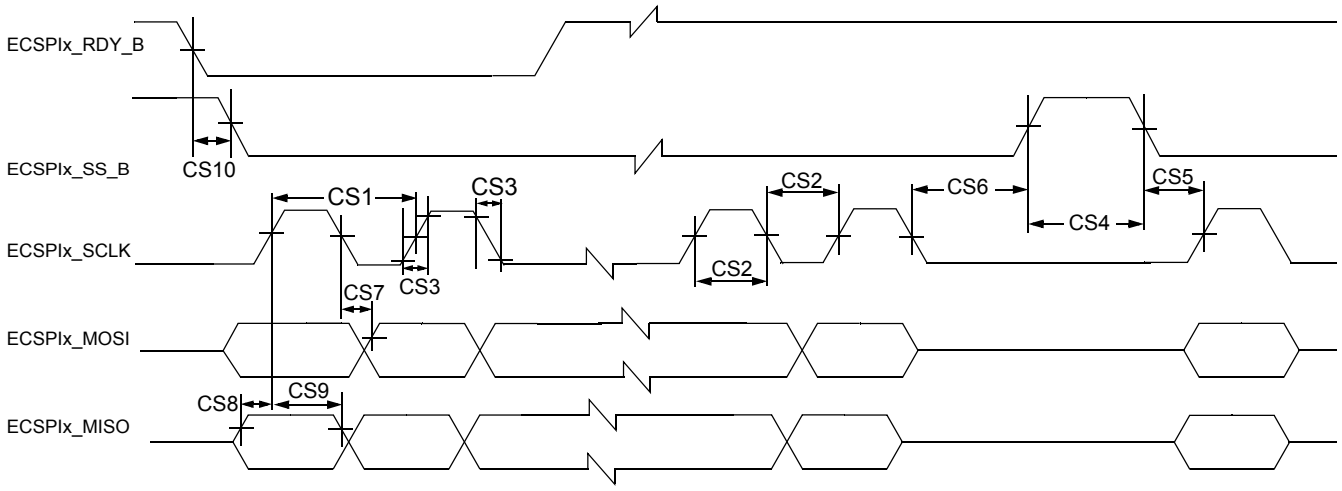

Figure 35. ECSPI Master Mode Timing Diagram

Table 47. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	14	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.7, “I/O AC Parameters”.”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

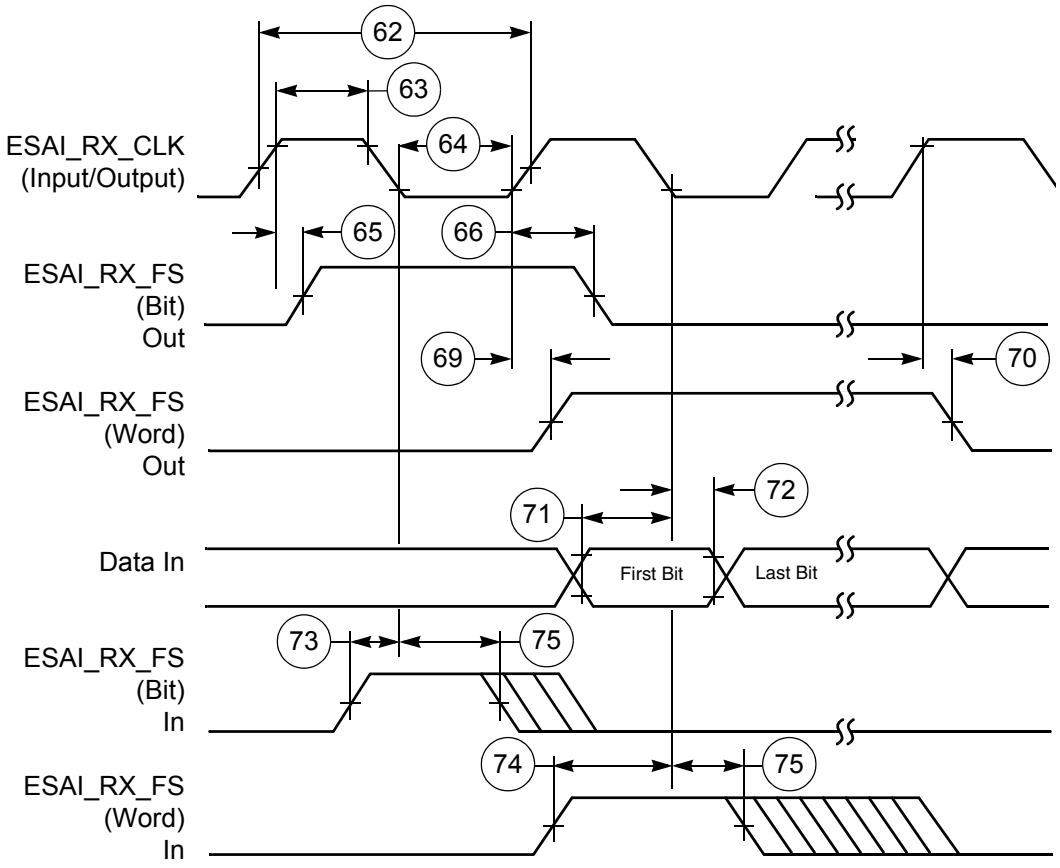

Figure 38. ESAI Receiver Timing

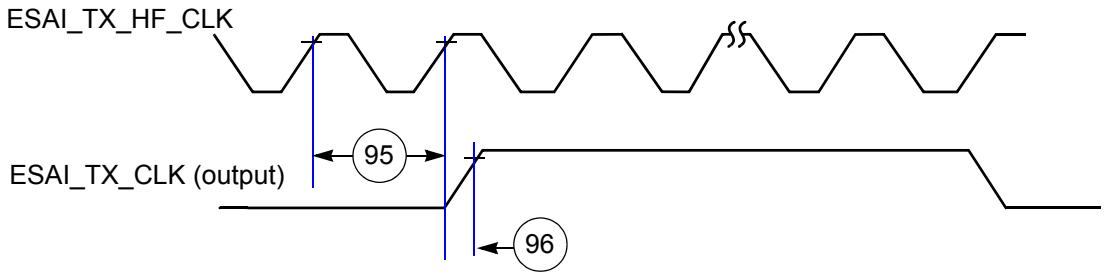

Figure 39. ESAI ESAI_TX_HF_CLK Timing

4.12.4.3 SDR50/SDR104 AC Timing

Figure 42 depicts the timing of SDR50/SDR104, and Table 52 lists the SDR50/SDR104 timing characteristics.

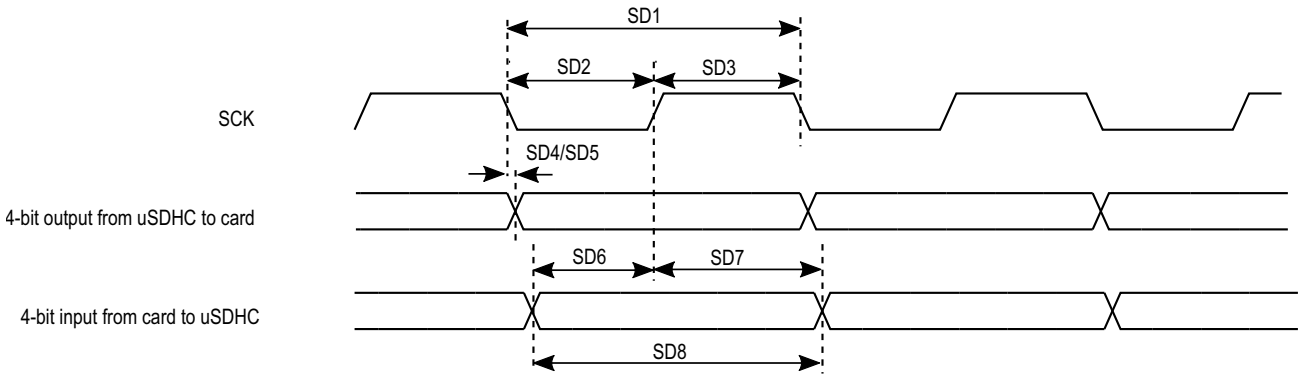

Figure 42. SDR50/SDR104 Timing

Table 52. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]Data window in SDR104 mode is variable.

4.12.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 47 shows MII asynchronous input timings. Table 57 describes the timing parameters (M10–M15) shown in the figure.

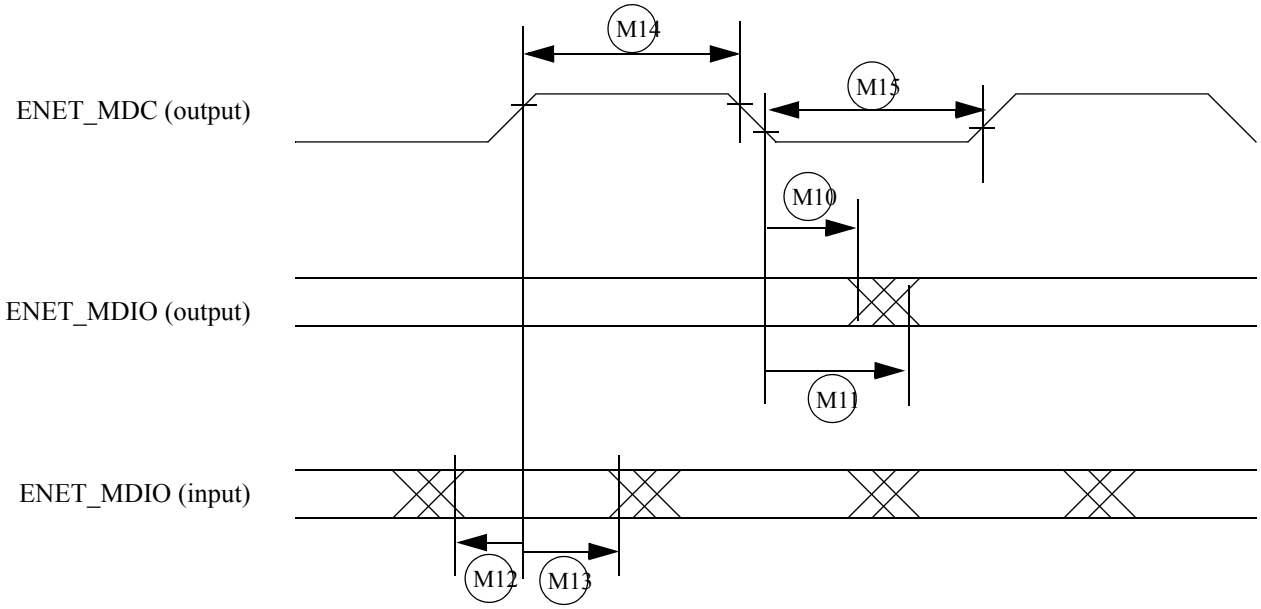

Figure 47. MII Serial Management Channel Timing Diagram

Table 57. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.12.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the RMII_CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0], and ENET_RX_ER.

4.12.7 I²C Bus Characteristics

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

4.12.8 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 49 depicts the timing of the PWM, and Table 59 lists the PWM timing parameters.

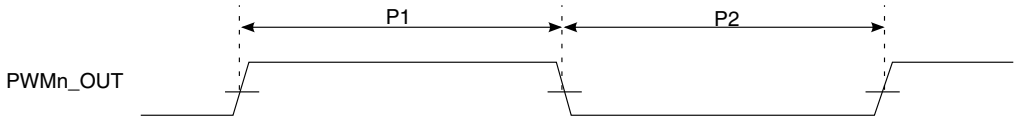

Figure 49. PWM Timing

Table 59. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	66	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

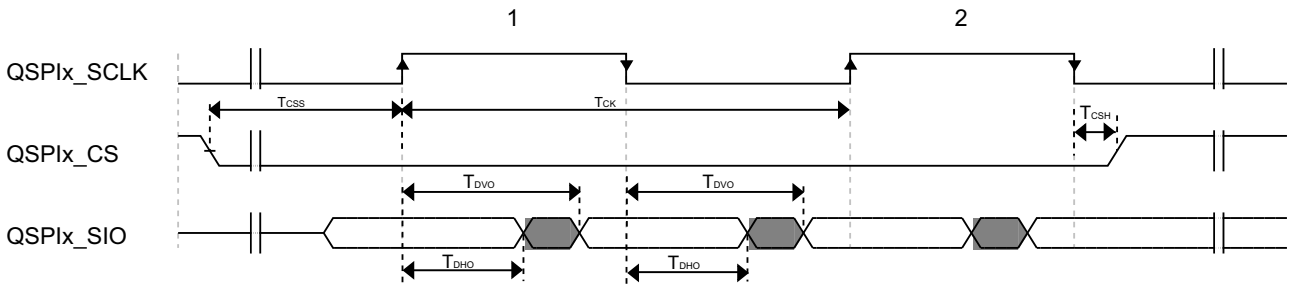

Figure 56. QuadSPI Output/Write Timing (DDR mode)

Table 67. QuadSPI Output/Write Timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	(0.25 x T_{SCLK}) + 2	ns
T_{DHO}	Output data hold time	(0.25 x T_{SCLK}) - 0.5	—	ns
T_{CK}	SCK clock period	20	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6ULL Reference Manual (IMX6ULLRM)* for more details.

4.12.11 SAI/I2S Switching Specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 68. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	2 x t_{sys}	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	4 x t_{sys}	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period

- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

4.13 A/D converter

The following subsections provide information about A/D converter.

4.13.1 12-bit ADC electrical characteristics

4.13.1.1 12-bit ADC operating conditions

Table 76. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	3.0	-	3.6	V	—
	Delta to VDD (VDD-VDDAD)[2]	ΔVDDAD	-100	0	100	mV	—
Ground voltage	Delta to VSS (VSS-VSSAD)	ΔVSSAD	-100	0	100	mV	—
Ref Voltage High	—	V_{REFH}	1.13	V_{DDAD}	V_{DDAD}	V	—
Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	—
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	8/10/12 bit modes	C_{ADIN}	—	1.5	2	pF	—
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	—	5	7	kohms	—
	ADLPC=0, ADHSC=0		—	12.5	15	kohms	—
	ADLPC=1, ADHSC=0		—	25	30	kohms	—
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	—	—	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							

7 Revision History

Table 96 provides a revision history for this data sheet.

Table 96. i.MX 6ULL Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
1.2	09/2017	• Updated the part numbers and added a new part number (MCIMX6Y2DVK09AB) in the Table 1, "Ordering Information" • Updated the silicon revision number in the Figure 1, "Part Number Nomenclature—i.MX 6ULL" • Updated the GPIO1_IO09 signal name in the Table 85, "SD/MMC Boot through USDHC1" and added a footnote • Updated the NAND_ALE signal name in the Table 86, "SD/MMC Boot through USDHC2" and added a footnote
1.1	05/2017	• Changed terminology from “floating” to “not connected” • Changed the LV-DDR3 to DDR3L in the Section 1.2, “Features" • Added a footnote regarding maximum voltage allowance in the Table 7, "Absolute Maximum Ratings" • Updated the minimum value of VDD_SOC_CAP in the Low Power Run Mode: LDO Enabled from the Table 10, "Operating Ranges" • Removed the LPSR mode in the Section 4.1.6, “Power Modes" • Removed a note in the Section 4.2.1, “Power-Up Sequence" • Replaced the MMDC compatible information with a cross reference in the Section 4.6.3, “DDR I/O DC Parameters" and Section 4.7.2, “DDR I/O AC Parameters" • Removed the Section 4.9.4, “DDR SDRAM Specific Parameters (DDR3 and LPDDR2)” • Added a new Section 4.10, “Multi-Mode DDR Controller (MMDC)" • Changed SD3 min to 1.7 ns in the Table 51, "eMMC4.4/4.41 Interface Timing Specification"
1	04/2017	• Added two new part numbers in the Table 1, "Ordering Information" • Updated the Part differentiator number 3 to Reserved, removed 300 MHz from frequency, and added 900 MHz in the Figure 1, "Part Number Nomenclature—i.MX 6ULL" • Updated the DDR I/O supply voltage and added a table not in the Table 7, "Absolute Maximum Ratings" • Updated Table 10, "Operating Ranges" • Added Max. current for VDD_SOC_IN at 900 MHz in the Table 13, "Maximum Supply Currents" • Updated the LDO_2P5 of the LOW POWER IDLE: LDO Bypassed row in the Table 15, "Low Power Mode Current and Power Consumption" • Updated the Figure 18, "Asynchronous A/D Muxed Write Access" • Added a new Section 4.12.9.1, “LCDIF Signal Mapping" • Added a note in the Section 4.2.1, “Power-Up Sequence" • Updated VDD_HIGH_CAP pin assignment in the Table 90, "14 x 14 mm Supplies Contact Assignment" • Updated VDD_HIGH_CAP pin name in the Table 92, "14 x 14 mm, 0.8 mm Pitch, Ball Map"
0	09/2016	• Initial public release