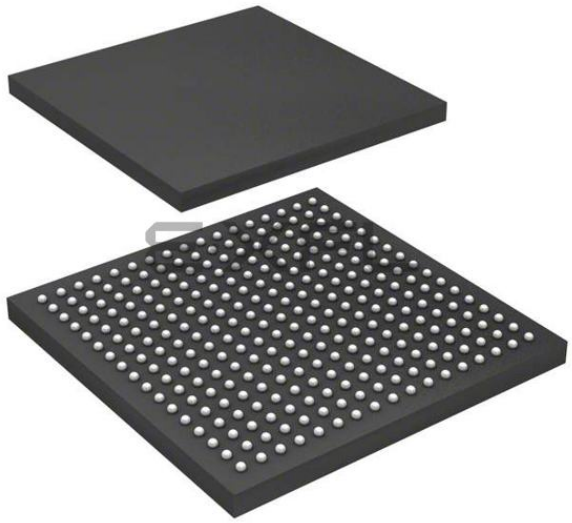

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	900MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Electrophoretic, LCD
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6y2dvm09aa

The i.MX 6ULL processors are specifically useful for applications such as:

- Telematics
- Audio playback
- Connected devices
- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Portable medical and health care
- IP phones
- Smart appliances
- eReaders

The features of the i.MX 6ULL processors include:

- Single-core Arm Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, an Electrophoretic Display (EPD) controller, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- 2x Ethernet interfaces—2x 10/100 Mbps Ethernet controllers.
- Human-machine interface—Each processor supports one digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: two high-speed USB on-the-go with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), two 12-bit ADC modules with up to 10 total input channels and two CAN ports.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, AES-128 encryption, SHA-1, SHA-256 HW acceleration engine, and secure software downloads. The security features are discussed in the *i.MX 6ULL Security Reference Manual* (IMX6ULLSRM).

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6Y2DVM05AA MCIMX6Y2DVM05AB	Features supports: • 528 MHz, commercial grade for general purpose • Basic security • With LCD/CSI • CAN x2 • Ethernet x2 • USB OTG x2 • ADC x2 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	14 x 14 mm, 0.8 pitch MAPBGA	0 to +95
MCIMX6Y1DVK05AA MCIMX6Y1DVK05AB	Features supports: • 528 MHz, commercial grade for general purpose • Basic security • No LCD/CSI • CAN x1 • Ethernet x1 • USB OTG x2 • ADC x1 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	9 x 9 mm, 0.5 pitch MAPBGA	0 to +95
MCIMX6Y7DVK05AA MCIMX6Y7DVK05AB	Features supports: • 528 MHz, commercial grade for general purpose • Basic security • With LCD/CSI • EPDC • No CAN • Ethernet x1 • USB OTG x2 • ADC x2 • UART x4 • SAI x3 • ESAI x1 • Timer x4 • PWM x4 • I2C x4 • SPI x4	9 x 9 mm, 0.5 pitch MAPBGA	0 to +95

  - Cortex-A7 NEON Media Processing Engine (MPE) Co-processor
- General Interrupt Controller (GIC) with 128 interrupts support
- Global Timer
- Snoop Control Unit (SCU)
- 128 KB unified I/D L2 cache
- Single Master AXI bus interface output of L2 cache
- Frequency of the core (including Neon and L1 cache), as per Table 10, "Operating Ranges," on page 24.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
  - 32 double-precision VFPv3 floating point registers

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia/shared, fast access RAM (OCRAM, 128 KB)
- External memory interfaces: The i.MX 6ULL processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
  - 16-bit LP-DDR2-800, 16-bit DDR3-800 and DDR3L-800
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bits.
  - 16/8-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.

Each i.MX 6ULL processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays:
  - One parallel display port, support max 85 MHz display clock and up to WXGA (1366 x 768) at 60 Hz
  - Support 24-bit, 18-bit, 16-bit, and 8-bit parallel display
  - Electrophoretic display controller support direct-driver for E-Ink EPD panel, with up to 2048x1536 resolution at 106 Hz
- Camera sensors:
  - One parallel camera port, up to 24 bit and 133.3 MHz pixel clock
  - Support 24-bit, 16-bit, 10-bit, and 8-bit input
  - Support BT.656 interface
- Expansion cards:
  - Two MMC/SD/SDIO card ports all supporting:

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core Supply Voltage	VDDSOC_IN	-0.3	1.6	V
Internal Supply Voltage	VDDARM_CAP VDDSOC_CAP	-0.3	1.4	V
GPIO Supply Voltage	NVCC_CSI NVCC_ENET NVCC_GPIO NVCC_UART NVCC_LCD NVCC_NAND NVCC_SD1	-0.5	3.7	V
DDR IO Supply Voltage	NVCC_DRAM	-0.4	1.975[1]	V
VDD_SNVS_IN Supply Voltage	VDD_SNVS_IN	-0.3	3.6	V
VDDHIGH_IN Supply voltage	VDD_HIGH_IN	-0.3	3.7	V
USB VBUS	USB_OTG1_VBUS USB_OTG2_VBUS	—	5.5	V
Input voltage on USB_OTG_DP and USB_OTG_DN pins	USB_OTG1_DP/USB_OTG1_DN USB_OTG2_DP/USB_OTG2_DN	-0.3	3.63	V
Input/Output Voltage Range	$V_{in/Vout}$	-0.5	OVDD+0.3[2]	V
ESD damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	Vesd	 — —	 2000 500	V
Storage Temperature Range	TSTORAGE	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575 V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 14 x 14 mm (VM) Package Thermal Resistance

Table 8 displays the 14 x 14 mm (VM) package thermal resistance data.

Table 8. 14 x 14 (VM) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural convection	Single-layer board (1s)	$R_{\theta JA}$	58.4	°C/W	1,2
Junction to Ambient Natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	37.6	°C/W	1,2,3

Table 8. 14 x 14 (VM) Thermal Resistance Data (continued)

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	48.6	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	32.9	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	21.8	°C/W	4
Junction to Case	—	$R_{\theta JC}$	19.3	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2.3	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB}	12.0	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB

4.1.2.2 9 x 9 MM (VK) Package Thermal Resistance

Table 9 displays the 9 x 9 MM (VK) thermal resistance data.

Table 9. 9 x 9 MM (VK) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single-layer board (1s)	$R_{\theta JA}$	65.6	°C/W	1,2
Junction to Ambient Natural Convection	Four-layer board (2s2p)	$R_{\theta JA}$	36.2	°C/W	1,2,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	51.2	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	31.8	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	17.1	°C/W	4
Junction to Case	—	$R_{\theta JC}$	14.5	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	0.6	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB_CSB}	11.1	°C/W	7

2 In setting VDD_SNVS_IN voltage with regards to Charging Currents and RTC, refer to the *i.MX 6ULL Hardware Development Guide* (IMX6ULLHDG).

Table 11 shows on-chip LDO regulators that can supply on-chip loads.

Table 11. On-Chip LDOs[1] and their On-Chip Loads

Voltage Source	Load	Comment
VDD_HIGH_CAP	NVCC_DRAM_2P5	Board-level connection to VDD_HIGH_CAP

1 On-chip LDOs are designed to supply i.MX 6ULL loads and must not be used to supply external loads.

4.1.4 External Clock Sources

Each i.MX 6ULL processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 12 shows the interface frequency requirements.

Table 12. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX 6ULL Applications Processors* (IMX6ULLHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 12 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

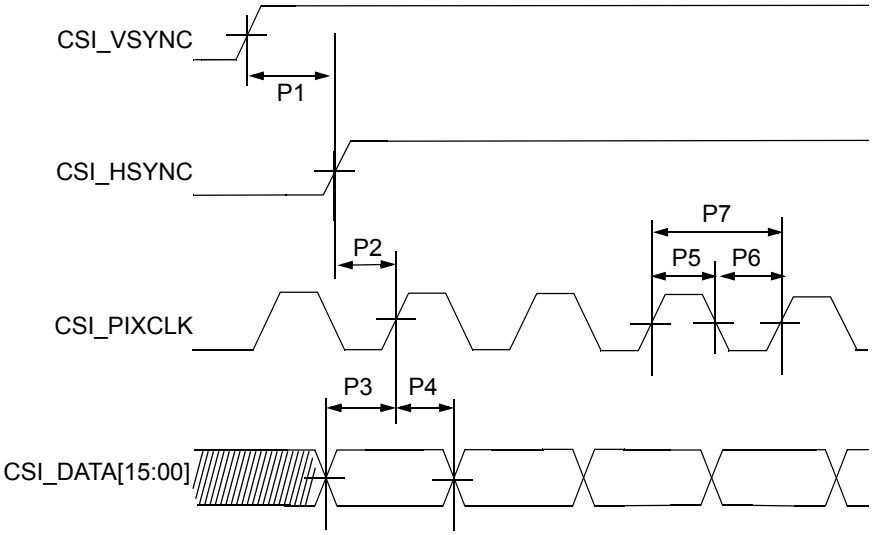

Figure 32. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

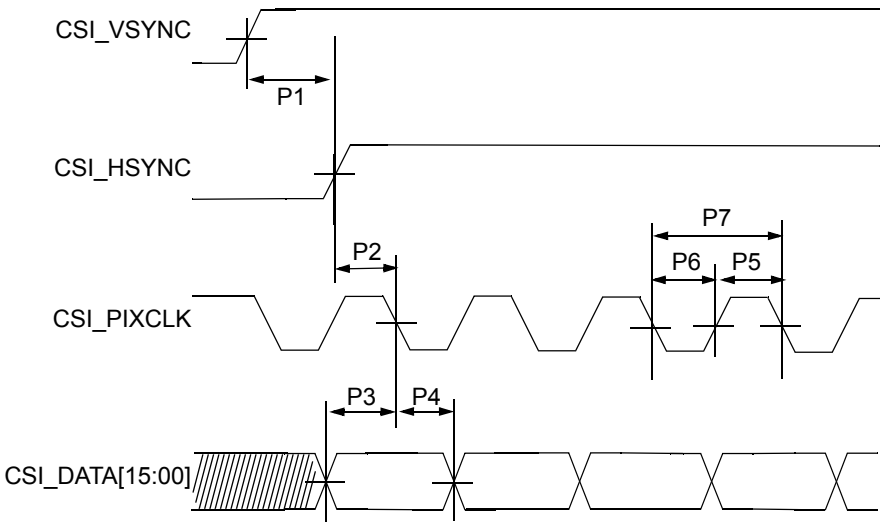

Figure 33. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 45. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns

Table 49. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
64	Clock low period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before ESAI_RX_CLK falling edge	— —	— —	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after ESAI_RX_CLK falling edge	— —	— —	6.0 0.0	— —	x ck i ck s	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 50. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.4.2 eMMC4.4/4.41 (Dual Data Rate) AC Timing

Figure 41 depicts the timing of eMMC4.4/4.41. Table 51 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

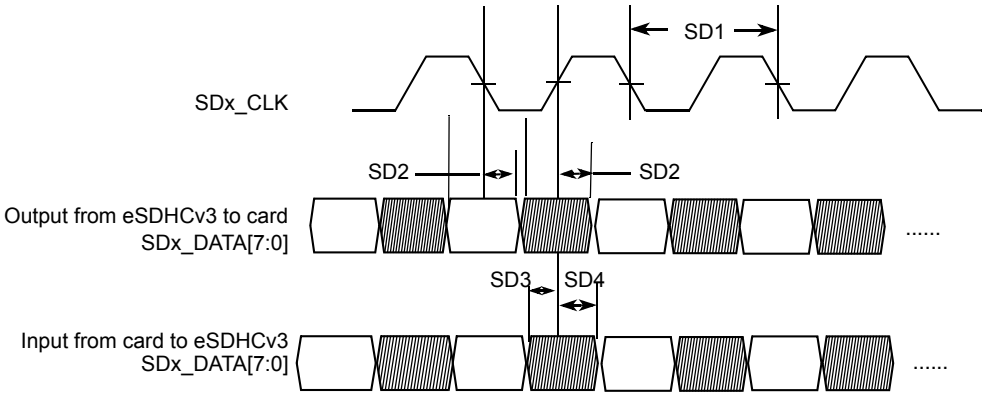

Figure 41. eMMC4.4/4.41 Timing

Table 51. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.12.4.3 SDR50/SDR104 AC Timing

Figure 42 depicts the timing of SDR50/SDR104, and Table 52 lists the SDR50/SDR104 timing characteristics.

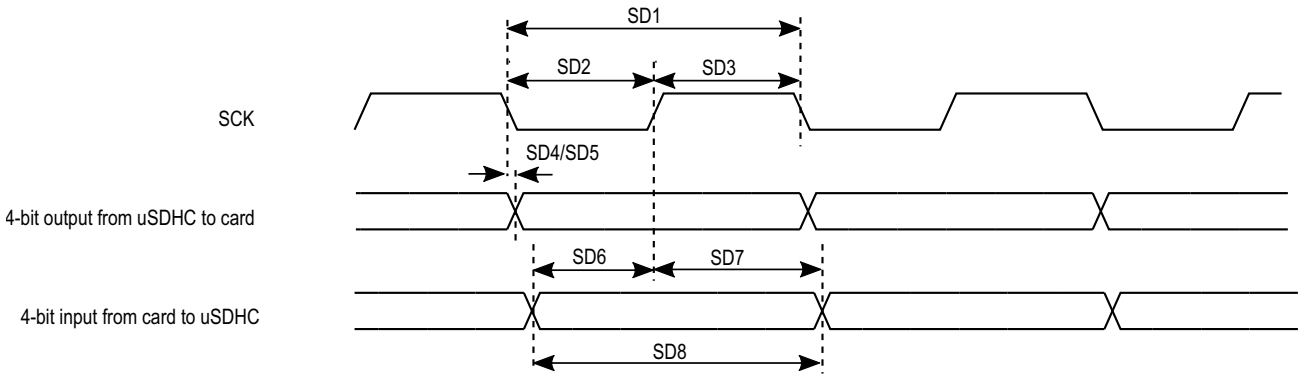

Figure 42. SDR50/SDR104 Timing

Table 52. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]Data window in SDR104 mode is variable.

4.12.9 LCD Controller (LCDIF) Parameters

Figure 50 shows the LCDIF timing and Table 60 lists the timing parameters.

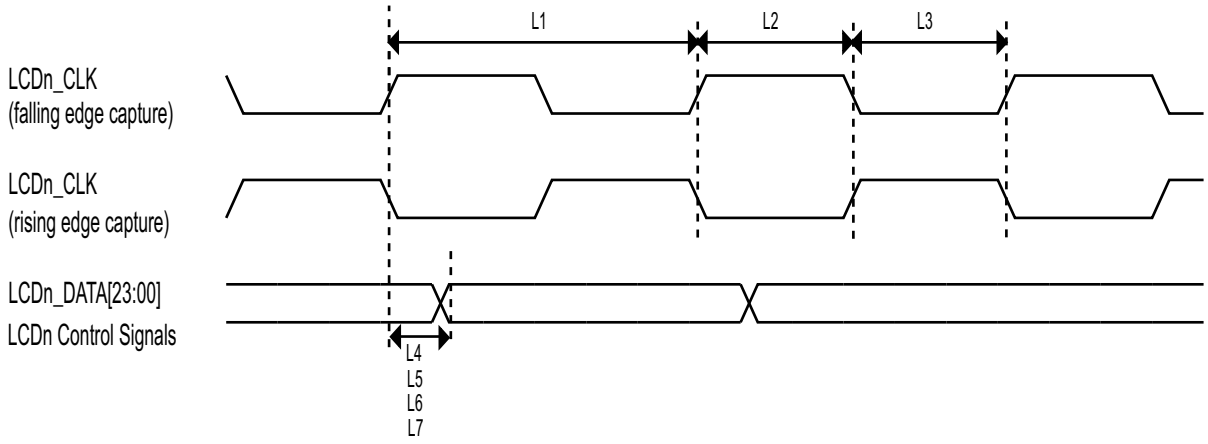

Figure 50. LCD Timing

Table 60. LCD Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	150	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.12.9.1 LCDIF Signal Mapping

Table 61 lists the details about the mapping signals.

Table 61. LCD Timing Parameters

Pin name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	24-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_RS	—	—	—	—	CCIR_CLK
LCD_VSYNC* (Two options)	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	—
LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	—
LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	—

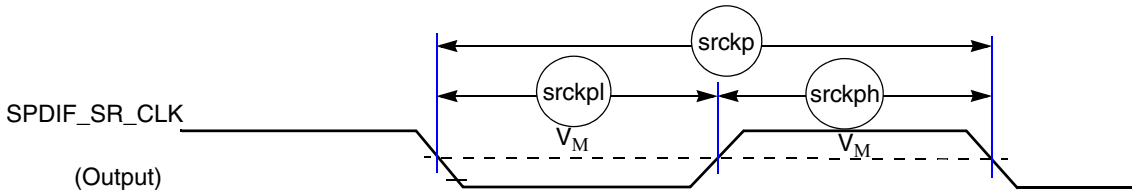

Figure 63. SPDIF_SR_CLK Timing Diagram

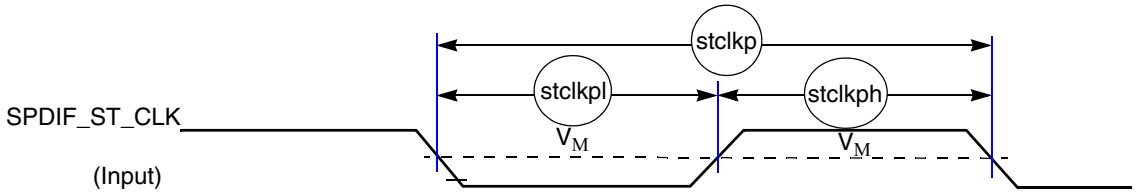

Figure 64. SPDIF_ST_CLK Timing Diagram

4.12.14 UART I/O Configuration and Timing Parameters

4.12.14.1 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.14.1.1 UART Transmitter

Figure 65 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 72 lists the UART RS-232 serial mode transmits timing characteristics.

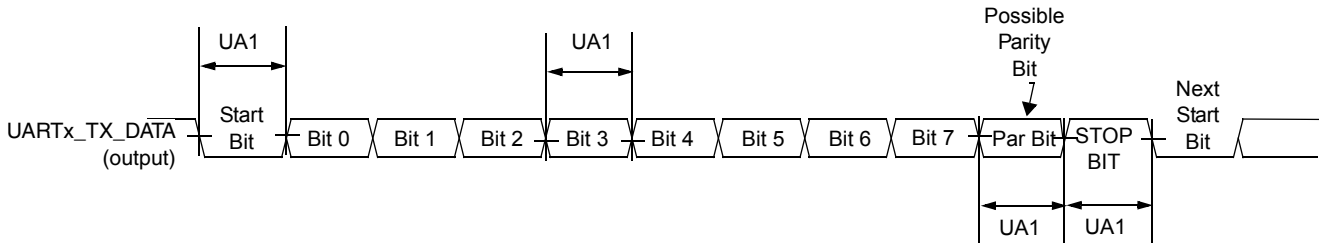

Figure 65. UART RS-232 Serial Mode Transmit Timing Diagram

Table 72. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

Table 81. SPI Boot through ECSPI2 (continued)

LCD_VSYNC	ecspi2.SS2	Alt 8				Yes	
LCD_RESET	ecspi2.SS3	Alt 8					Yes

Table 82. SPI Boot through ECSPI3

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4[5:4]=01b	BOOT_CFG4[5:4]=10b	BOOT_CFG4 [5:4]=11b
UART2_RTS_B	ecspi3.MISO	Alt 8	Yes				
UART2_CTS_B	ecspi3.MOSI	Alt 8	Yes				
UART2_RX_DATA	ecspi3.SCLK	Alt 8	Yes				
UART2_TX_DATA	ecspi3.SS0	Alt 8		Yes			
NAND_ALE	ecspi3.SS1	Alt 8			Yes		
NAND_RE_B	ecspi3.SS2	Alt 8				Yes	
NAND_WE_B	ecspi3.SS3	Alt 8					Yes

Table 83. SPI Boot through ECSPI4

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4[5:4]=01b	BOOT_CFG4[5:4]=10b	BOOT_CFG 4[5:4]=11b
ENET2_TX_CLK	ecspi4.MISO	Alt 3	Yes				
ENET2_TX_EN	ecspi4.MOSI	Alt 3	Yes				
ENET2_TX_DATA1	ecspi4.SCLK	Alt 3	Yes				
ENET2_RX_ER	ecspi4.SS0	Alt 3		Yes			
NAND_DATA01	ecspi4.SS1	Alt 8			Yes		
NAND_DATA02	ecspi4.SS2	Alt 8				Yes	
NAND_DATA03	ecspi4.SS3	Alt 8					Yes

Table 84. NAND Boot through GPMI

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_CLE	rawnand.CLE	Alt 0	Yes		
NAND_ALE	rawnand.ALE	Alt 0	Yes		
NAND_WP_B	rawnand.WP_B	Alt 0	Yes		
NAND_READY_B	rawnand.READY_B	Alt 0	Yes		
NAND_CE0_B	rawnand.CE0_B	Alt 0	Yes		
NAND_CE1_B	rawnand.CE1_B	Alt 0		Yes	Yes
NAND_RE_B	rawnand.RE_B	Alt 0	Yes		

Table 86. SD/MMC Boot through USDHC2

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)
NAND_RE_B	usdhc2.CLK	Alt 1	Yes			
NAND_WE_B	usdhc2.CMD	Alt 1	Yes			
NAND_DATA00	usdhc2.DATA0	Alt 1	Yes			
NAND_DATA01	usdhc2.DATA1	Alt 1		Yes	Yes	
NAND_DATA02	usdhc2.DATA2	Alt 1		Yes	Yes	
NAND_DATA03	usdhc2.DATA3	Alt 1	Yes			
NAND_DATA04	usdhc2.DATA4	Alt 1			Yes	
NAND_DATA05	usdhc2.DATA5	Alt 1			Yes	
NAND_DATA06	usdhc2.DATA6	Alt 1			Yes	
NAND_DATA07	usdhc2.DATA7	Alt 1			Yes	
NAND_ALE	NAND_ALE[1]	Alt 5				Yes
GPIO1_IO08	usdhc2.VSELECT	Alt 4				Yes

1 The Boot ROM uses NAND_ALE to implement SD2_RESET_B.

Table 87. NOR/OneNAND Boot through EIM

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
CSI_DATA00	weim.AD[0]	Alt 4	Yes		
CSI_DATA01	weim.AD[1]	Alt 4	Yes		
CSI_DATA02	weim.AD[2]	Alt 4	Yes		
CSI_DATA03	weim.AD[3]	Alt 4	Yes		
CSI_DATA04	weim.AD[4]	Alt 4	Yes		
CSI_DATA05	weim.AD[5]	Alt 4	Yes		
CSI_DATA06	weim.AD[6]	Alt 4	Yes		
CSI_DATA07	weim.AD[7]	Alt 4	Yes		
NAND_DATA00	weim.AD[8]	Alt 4	Yes		
NAND_DATA01	weim.AD[9]	Alt 4	Yes		
NAND_DATA02	weim.AD[10]	Alt 4	Yes		
NAND_DATA03	weim.AD[11]	Alt 4	Yes		
NAND_DATA04	weim.AD[12]	Alt 4	Yes		
NAND_DATA05	weim.AD[13]	Alt 4	Yes		
NAND_DATA06	weim.AD[14]	Alt 4	Yes		

6.1.2 14 x 14 mm Supplies Contact Assignments and Functional Contact Assignments

Table 90 shows the device connection list for ground, sense, and reference contact signals.

Table 90. 14 x 14 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	M13	—
DRAM_VREF	P4	—
GPANIO	R13	—
NGND_KEL0	M12	—
NVCC_CSI	F4	—
NVCC_DRAM	G6, H6, J6, K6, L6, M6	—
NVCC_DRAM_2P5	N6	—
NVCC_ENET	F13	—
NVCC_GPIO	J13	—
NVCC_LCD	E13	—
NVCC_NAND	E7	—
NVCC_PLL	P13	—
NVCC_SD1	C4	—
NVCC_UART	H13	—
VDD_ARM_CAP	G9, G10, G11, H11	—
VDD_HIGH_CAP	R14, R15	—
VDD_HIGH_IN	N13	—
VDD_SNVS_CAP	N12	—
VDD_SNVS_IN	P12	—
VDD_SOC_CAP	G8, H8, J8, J11, K8, K11, L8, L9, L10, L11	—
VDD_SOC_IN	H9, H10, J9, J10, K9, 10	—
VDD_USB_CAP	R12	—
VDDA_ADC_3P3	L13	—
VSS	A1, A17, C3, C7, C11, C15, E8, E11, F6, F7, F8, F9, F10,F11, F12, G3, G5, G7, G12, G15, H7, H12, J5, J7, J12, K7, K12, L3, L7, L12, M7, M8, M9, M10, M11, N3, N5, R3, R5, R7, R11, R16, R17, T14, U1, U14, U17	—

Table 91. 14 x 14 mm Functional Contact Assignments (continued)

JTAG_MOD	P15	NVCC_GPIO	SJC	ALT0	SJC_MOD	Input	100 kΩ pull-up
JTAG_TCK	M14	NVCC_GPIO	SJC	ALT0	SJC_TCK	Input	47 kΩ pull-up
JTAG_TDI	N16	NVCC_GPIO	SJC	ALT0	SJC_TDI	Input	47 kΩ pull-up
JTAG_TDO	N15	NVCC_GPIO	SJC	ALT0	SJC_TDO	Output	Keeper
JTAG_TMS	P14	NVCC_GPIO	SJC	ALT0	SJC_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	N14	NVCC_GPIO	SJC	ALT0	SJC_TRSTB	Input	47 kΩ pull-up
LCD_CLK	A8	NVCC_LCD	GPIO	ALT5	GPIO3_IO0	Input	Keeper
LCD_DATA00	B9	NVCC_LCD	GPIO	ALT5	GPIO3_IO5	Input	Keeper
LCD_DATA01	A9	NVCC_LCD	GPIO	ALT5	GPIO3_IO6	Input	Keeper
LCD_DATA02	E10	NVCC_LCD	GPIO	ALT5	GPIO3_IO7	Input	Keeper
LCD_DATA03	D10	NVCC_LCD	GPIO	ALT5	GPIO3_IO8	Input	Keeper
LCD_DATA04	C10	NVCC_LCD	GPIO	ALT5	GPIO3_IO9	Input	Keeper
LCD_DATA05	B10	NVCC_LCD	GPIO	ALT5	GPIO3_IO10	Input	Keeper
LCD_DATA06	A10	NVCC_LCD	GPIO	ALT5	GPIO3_IO11	Input	Keeper
LCD_DATA07	D11	NVCC_LCD	GPIO	ALT5	GPIO3_IO12	Input	Keeper
LCD_DATA08	B11	NVCC_LCD	GPIO	ALT5	GPIO3_IO13	Input	Keeper
LCD_DATA09	A11	NVCC_LCD	GPIO	ALT5	GPIO3_IO14	Input	Keeper
LCD_DATA10	E12	NVCC_LCD	GPIO	ALT5	GPIO3_IO15	Input	Keeper
LCD_DATA11	D12	NVCC_LCD	GPIO	ALT5	GPIO3_IO16	Input	Keeper
LCD_DATA12	C12	NVCC_LCD	GPIO	ALT5	GPIO3_IO17	Input	Keeper
LCD_DATA13	B12	NVCC_LCD	GPIO	ALT5	GPIO3_IO18	Input	Keeper
LCD_DATA14	A12	NVCC_LCD	GPIO	ALT5	GPIO3_IO19	Input	Keeper
LCD_DATA15	D13	NVCC_LCD	GPIO	ALT5	GPIO3_IO20	Input	Keeper
LCD_DATA16	C13	NVCC_LCD	GPIO	ALT5	GPIO3_IO21	Input	Keeper
LCD_DATA17	B13	NVCC_LCD	GPIO	ALT5	GPIO3_IO22	Input	Keeper
LCD_DATA18	A13	NVCC_LCD	GPIO	ALT5	GPIO3_IO23	Input	Keeper
LCD_DATA19	D14	NVCC_LCD	GPIO	ALT5	GPIO3_IO24	Input	Keeper
LCD_DATA20	C14	NVCC_LCD	GPIO	ALT5	GPIO3_IO25	Input	Keeper
LCD_DATA21	B14	NVCC_LCD	GPIO	ALT5	GPIO3_IO26	Input	Keeper
LCD_DATA22	A14	NVCC_LCD	GPIO	ALT5	GPIO3_IO27	Input	Keeper
LCD_DATA23	B16	NVCC_LCD	GPIO	ALT5	GPIO3_IO28	Input	Keeper

Table 91. 14 x 14 mm Functional Contact Assignments (continued)

UART1_TX_DATA	K14	NVCC_UART	GPIO	ALT5	GPIO1_IO16	Input	Keeper
UART2_CTS_B	J15	NVCC_UART	GPIO	ALT5	GPIO1_IO22	Input	Keeper
UART2_RTS_B	H14	NVCC_UART	GPIO	ALT5	GPIO1_IO23	Input	Keeper
UART2_RX_DATA	J16	NVCC_UART	GPIO	ALT5	GPIO1_IO21	Input	Keeper
UART2_TX_DATA	J17	NVCC_UART	GPIO	ALT5	GPIO1_IO20	Input	Keeper
UART3_CTS_B	H15	NVCC_UART	GPIO	ALT5	GPIO1_IO26	Input	Keeper
UART3_RTS_B	G14	NVCC_UART	GPIO	ALT5	GPIO1_IO27	Input	Keeper
UART3_RX_DATA	H16	NVCC_UART	GPIO	ALT5	GPIO1_IO25	Input	Keeper
UART3_TX_DATA	H17	NVCC_UART	GPIO	ALT5	GPIO1_IO24	Input	Keeper
UART4_RX_DATA	G16	NVCC_UART	GPIO	ALT5	GPIO1_IO29	Input	Keeper
UART4_TX_DATA	G17	NVCC_UART	GPIO	ALT5	GPIO1_IO28	Input	Keeper
UART5_RX_DATA	G13	NVCC_UART	GPIO	ALT5	GPIO1_IO31	Input	Keeper
UART5_TX_DATA	F17	NVCC_UART	GPIO	ALT5	GPIO1_IO30	Input	Keeper
USB_OTG1_CHD_B	U16	OPEN DRAIN	GPIO	—	USB_OTG1_CHD_B	—	—
USB_OTG1_DN	T15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DN	—	—
USB_OTG1_DP	U15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DP	—	—
USB_OTG1_VBUS	T12	USB_VBUS	VBUS POWER	—	USB_OTG1_VBUS	—	—
USB_OTG2_DN	T13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DN	—	—
USB_OTG2_DP	U13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DP	—	—
USB_OTG2_VBUS	U12	USB_VBUS	VBUS POWER	—	USB_OTG2_VBUS	—	—
XTALI	T16	NVCC_PLL	ANALOG	—	XTALI	—	—
XTALO	T17	NVCC_PLL	ANALOG	—	XTALO	—	—

[1] SNVS_TAMPER0 to SNVS_TAMPER9 can be configured as GPIO or tamper detection pin, it is depending on the fuse setting TAMPER_PIN_DISABLE[1:0]. When the pad is configured as GPIO, the value is keeper out of reset.

[2] SNVS_TAMPER0 to SNVS_TAMPER9 is input unconnected in the following conditions.

—SNVS low power mode when configured as GPIO

—Tamper functions are not used when configured as TAMPER detection pins

It is required to connect external 1M Ohm pull-up or pull-down resistors to the pad to avoid the undesired leakage under two conditions above.

Table 92. 14 x 14 mm, 0.8 mm Pitch, Ball Map (continued)

P	N	M	L	K	J	H
DRAM_SDCLK0_P	DRAM_ODT0	DRAM_SDBA0	DRAM_ADDR05	DRAM_ADDR02	DRAM_SDWE_B	DRAM_SDBA1
DRAM_SDCLK0_N	DRAM_CS0_B	DRAM_ADDR03	DRAM_ADDR09	DRAM_SDBA2	DRAM_CAS_B	DRAM_ADDR01
DRAM_DATA13	VSS	DRAM_SDCKE0	VSS	DRAM_ADDR11	DRAM_SDCKE1	DRAM_ADDR13
DRAM_VREF	DRAM_ZQPAD	DRAM_ADDR10	DRAM_ADDR12	DRAM_ADDR04	DRAM_ADDR08	DRAM_ADDR07
DRAM_DATA12	VSS	DRAM_RAS_B	DRAM_ADDR00	DRAM_ADDR15	VSS	DRAM_CS1_B
DRAM_SDQS0_P	NVCC_DRAM_2P5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
DRAM_SDQS0_N	TEST_MODE	VSS	VSS	VSS	VSS	VSS
POR_B	SNVS_TAMPER5	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER4	SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN
SNVS_TAMPER3	SNVS_TAMPER7	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN
SNVS_TAMPER2	SNVS_TAMPER6	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP
VDD_SNVS_IN	VDD_SNVS_CAP	NGND_KEL0	VSS	VSS	VSS	VSS
NVCC_PLL	VDD_HIGH_IN	ADC_VREFH	VDDA_ADC_3P3	GPIO1_IO00	NVCC_GPIO	NVCC_UART
JTAG_TMS	JTAG_TRST_B	JTAG_TCK	GPIO1_IO02	UART1_TX_DATA	UART1_RTS_B	UART2_RTS_B
JTAG_MOD	JTAG_TDO	GPIO1_IO09	GPIO1_IO01	UART1_CTS_B	UART2_CTS_B	UART3_CTS_B
CCM_CLK1_N	JTAG_TDI	GPIO1_IO04	GPIO1_IO07	UART1_RX_DATA	UART2_RX_DATA	UART3_RX_DATA
CCM_CLK1_P	GPIO1_IO08	GPIO1_IO05	GPIO1_IO03	GPIO1_IO06	UART2_TX_DATA	UART3_TX_DATA
P	N	M	L	K	J	H

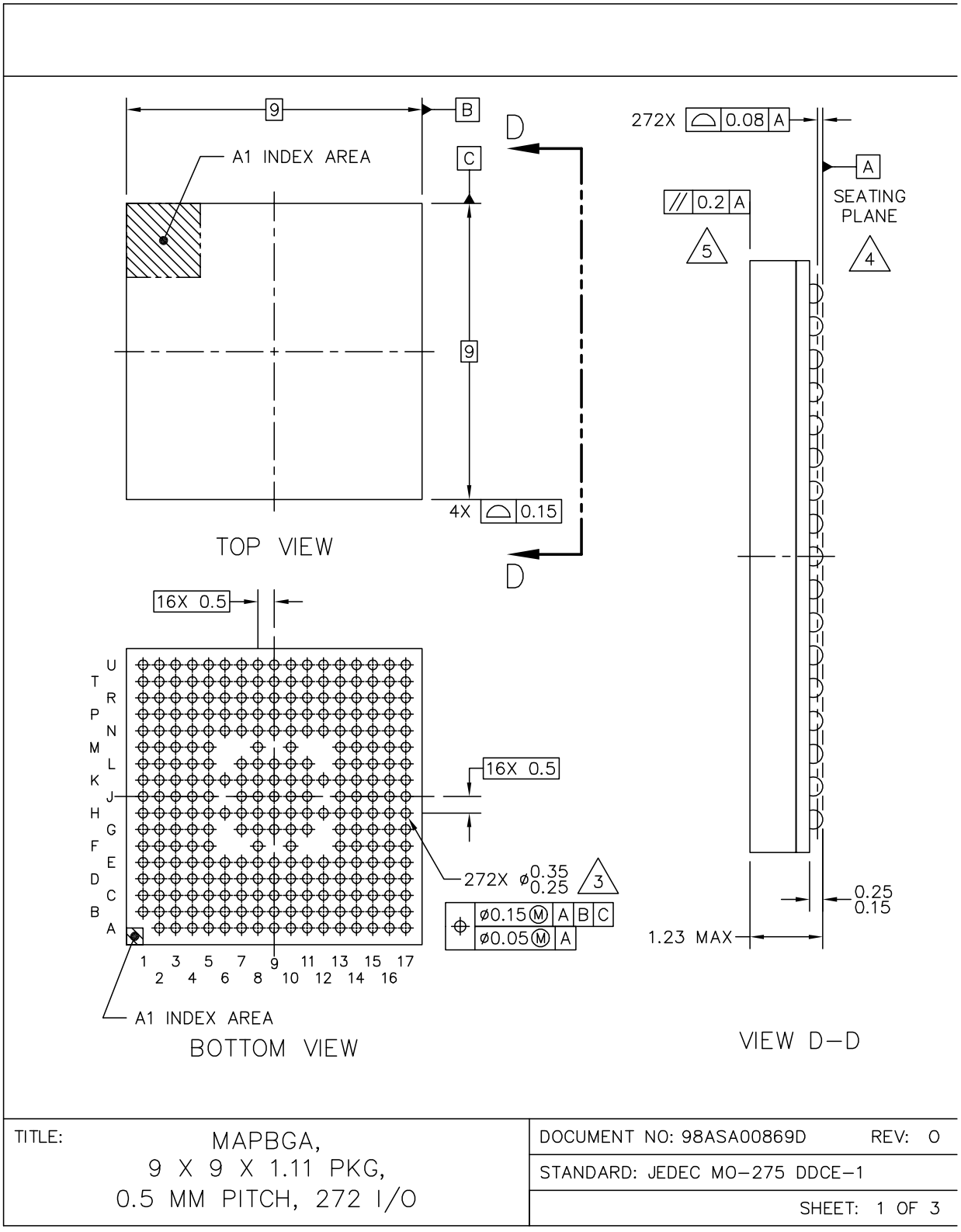

Figure 71. 9 x 9 mm BGA, Case x Package Top, Bottom, and Side Views

Table 94 shows an alpha-sorted list of functional contact assignments for the 9 x 9 mm package.

Table 94. 9 x 9 mm Functional Contact Assignments

Ball Name	9x9 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
BOOT_MODE0	T8	VDD_SNVS_IN	GPIO	ALT5	GPIO5_IO10	Input	100 kΩ pull-down
BOOT_MODE1	U8	VDD_SNVS_IN	GPIO	ALT5	GPIO5_IO11	Input	100 kΩ pull-down
CCM_CLK1_N	U16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_N	—	—
CCM_CLK1_P	T16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_P	—	—
CCM_PMIC_STBY_REQ	U7	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_VSTBY_REQ	Output	—
CSI_DATA00	C3	NVCC_CSI	GPIO	ALT5	GPIO4_IO21	Input	Keeper
CSI_DATA01	D4	NVCC_CSI	GPIO	ALT5	GPIO4_IO22	Input	Keeper
CSI_DATA02	B2	NVCC_CSI	GPIO	ALT5	GPIO4_IO23	Input	Keeper
CSI_DATA03	D1	NVCC_CSI	GPIO	ALT5	GPIO4_IO24	Input	Keeper
CSI_DATA04	C4	NVCC_CSI	GPIO	ALT5	GPIO4_IO25	Input	Keeper
CSI_DATA05	B3	NVCC_CSI	GPIO	ALT5	GPIO4_IO26	Input	Keeper
CSI_DATA06	A3	NVCC_CSI	GPIO	ALT5	GPIO4_IO27	Input	Keeper
CSI_DATA07	C2	NVCC_CSI	GPIO	ALT5	GPIO4_IO28	Input	Keeper
CSI_HSYNC	D2	NVCC_CSI	GPIO	ALT5	GPIO4_IO20	Input	Keeper
CSI_MCLK	C1	NVCC_CSI	GPIO	ALT5	GPIO4_IO17	Input	Keeper
CSI_PIXCLK	D5	NVCC_CSI	GPIO	ALT5	GPIO4_IO18	Input	Keeper
CSI_VSYNC	D3	NVCC_CSI	GPIO	ALT5	GPIO4_IO19	Input	Keeper
DRAM_ADDR00	G1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	G2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	100 kΩ pull-up
DRAM_ADDR02	H1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	100 kΩ pull-up
DRAM_ADDR03	J2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	100 kΩ pull-up
DRAM_ADDR04	M4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	100 kΩ pull-up
DRAM_ADDR05	H2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	100 kΩ pull-up
DRAM_ADDR06	E4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	100 kΩ pull-up