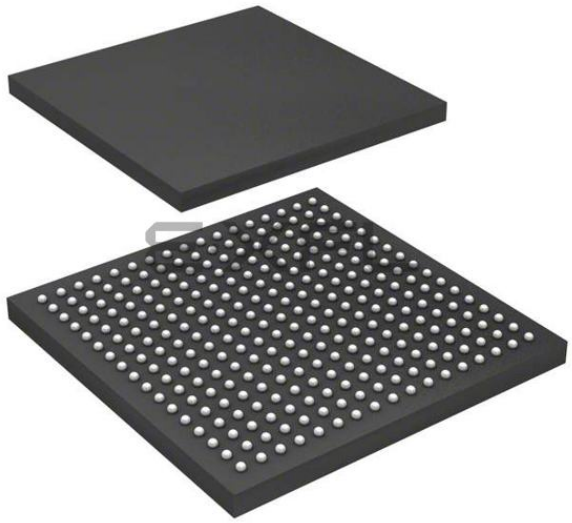

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	900MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Electrophoretic, LCD
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6y2dvm09ab

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6ULL processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6ULL processor system.

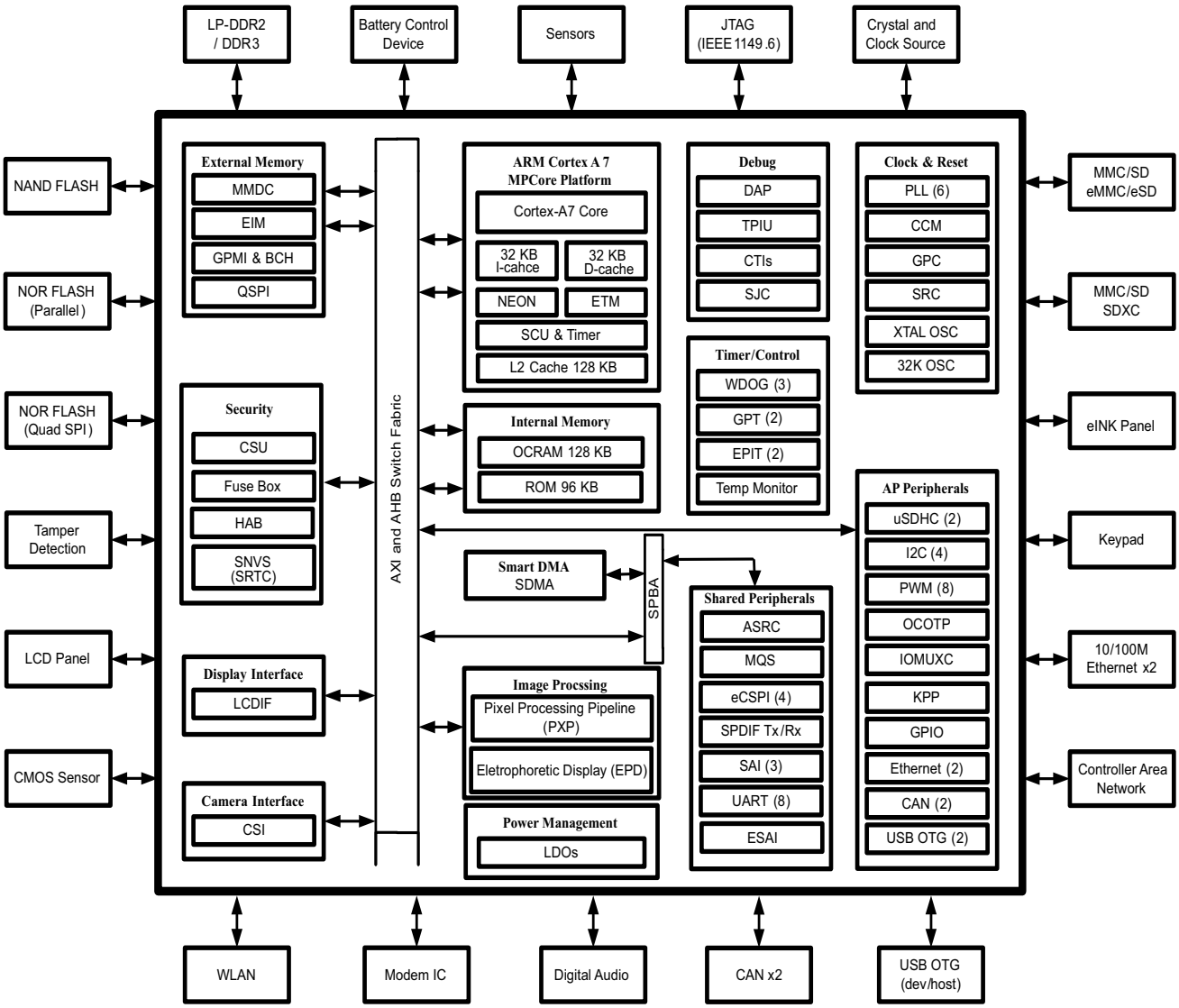

Figure 2. i.MX 6ULL System Block Diagram

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPDC	Electrophoretic Display Controller	Multimedia Peripherals	The EPDC is a feature-rich, low power, and high performance direct-drive active matrix EPD controller. It is specially designed to drive E-INK^{TM} EPD panels, supporting a wide variety of TFT backplanes.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.
RNGB	Random Number Generator	Security	Random number generating module.
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6ULL processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6ULL Chip-Level Conditions

For these characteristics	Topic appears
Absolute Maximum Ratings	on page 22
Thermal Resistance	on page 22
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximum Supply Currents	on page 27
Power Modes	on page 28
USB PHY Current Consumption	on page 31

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core Supply Voltage	VDDSOC_IN	-0.3	1.6	V
Internal Supply Voltage	VDDARM_CAP VDDSOC_CAP	-0.3	1.4	V
GPIO Supply Voltage	NVCC_CSI NVCC_ENET NVCC_GPIO NVCC_UART NVCC_LCD NVCC_NAND NVCC_SD1	-0.5	3.7	V
DDR IO Supply Voltage	NVCC_DRAM	-0.4	1.975[1]	V
VDD_SNVS_IN Supply Voltage	VDD_SNVS_IN	-0.3	3.6	V
VDDHIGH_IN Supply voltage	VDD_HIGH_IN	-0.3	3.7	V
USB VBUS	USB_OTG1_VBUS USB_OTG2_VBUS	—	5.5	V
Input voltage on USB_OTG_DP and USB_OTG_DN pins	USB_OTG1_DP/USB_OTG1_DN USB_OTG2_DP/USB_OTG2_DN	-0.3	3.63	V
Input/Output Voltage Range	$V_{in/Vout}$	-0.5	OVDD+0.3[2]	V
ESD damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	Vesd	 — —	 2000 500	V
Storage Temperature Range	TSTORAGE	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575 V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 14 x 14 mm (VM) Package Thermal Resistance

Table 8 displays the 14 x 14 mm (VM) package thermal resistance data.

Table 8. 14 x 14 (VM) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural convection	Single-layer board (1s)	$R_{\theta JA}$	58.4	°C/W	1,2
Junction to Ambient Natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	37.6	°C/W	1,2,3

Table 8. 14 x 14 (VM) Thermal Resistance Data (continued)

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	48.6	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	32.9	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	21.8	°C/W	4
Junction to Case	—	$R_{\theta JC}$	19.3	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2.3	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB}	12.0	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB

4.1.2.2 9 x 9 MM (VK) Package Thermal Resistance

Table 9 displays the 9 x 9 MM (VK) thermal resistance data.

Table 9. 9 x 9 MM (VK) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single-layer board (1s)	$R_{\theta JA}$	65.6	°C/W	1,2
Junction to Ambient Natural Convection	Four-layer board (2s2p)	$R_{\theta JA}$	36.2	°C/W	1,2,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	51.2	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	31.8	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	17.1	°C/W	4
Junction to Case	—	$R_{\theta JC}$	14.5	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	0.6	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB_CSB}	11.1	°C/W	7

regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB VBUS supply, when both are present. If only one of the USB VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX 6ULL Applications Processors* (IMX6ULLHDG).

For additional information, see the *i.MX 6ULL Reference Manual* (IMX6ULLRM).

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 17. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 18. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 19. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 20. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 Arm PLL

Table 21. Arm PLL's Electrical Parameters

Parameter	Value
Clock output range	648 MHz ~ 1296 MHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement an oscillator. The oscillator is powered from NVCC_PLL.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the backup battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from the VDD_HIGH_IN/VDD_SNVS_IN. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when

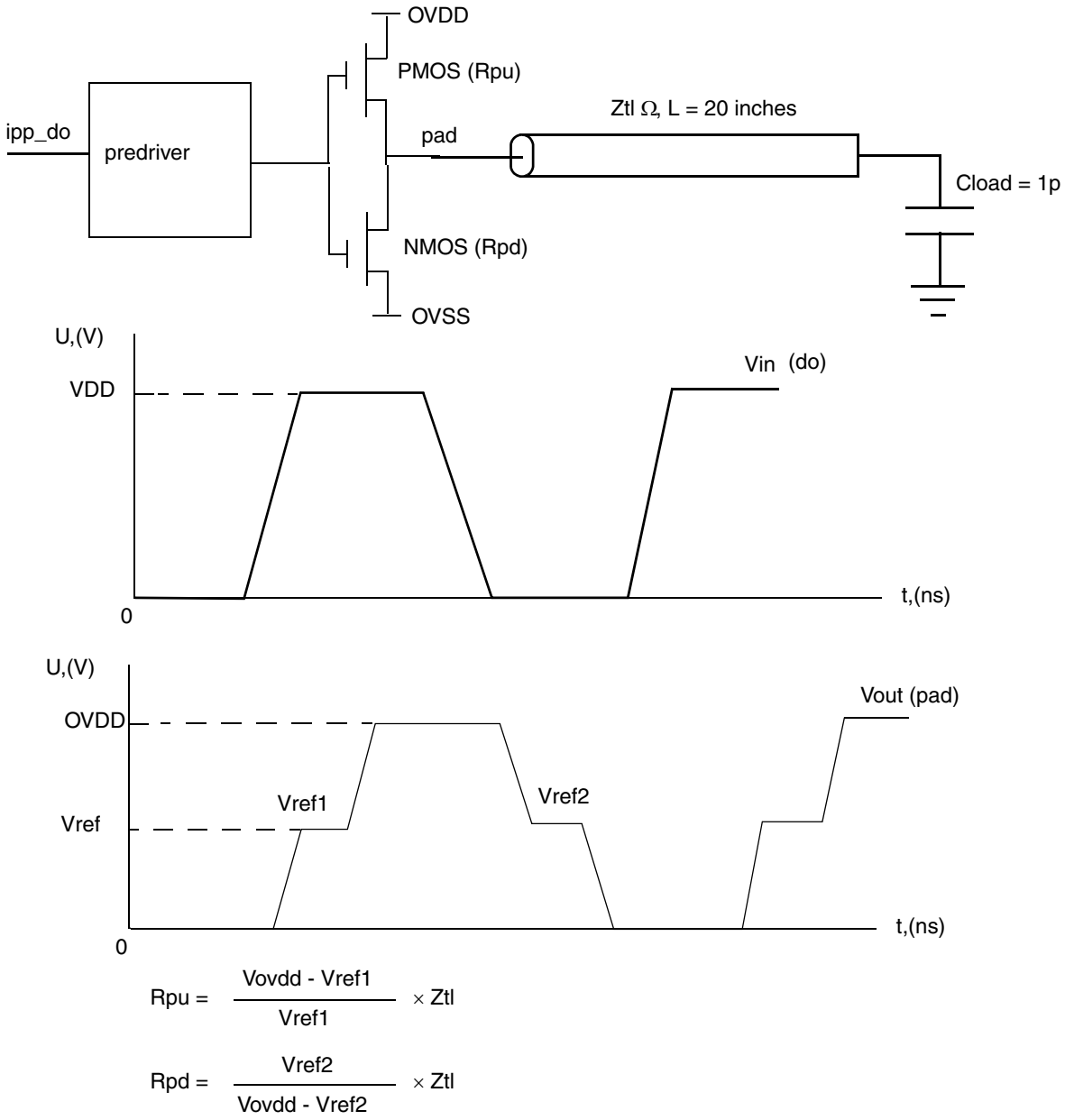

Figure 6. Impedance Matching Load for Measurement

4.8.1 Single Voltage GPIO Output Buffer Impedance

Table 33 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 39. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to EIM_CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to EIM_WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to EIM_OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to EIM_EBx_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to EIM_LBA_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	EIM_WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	EIM_WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

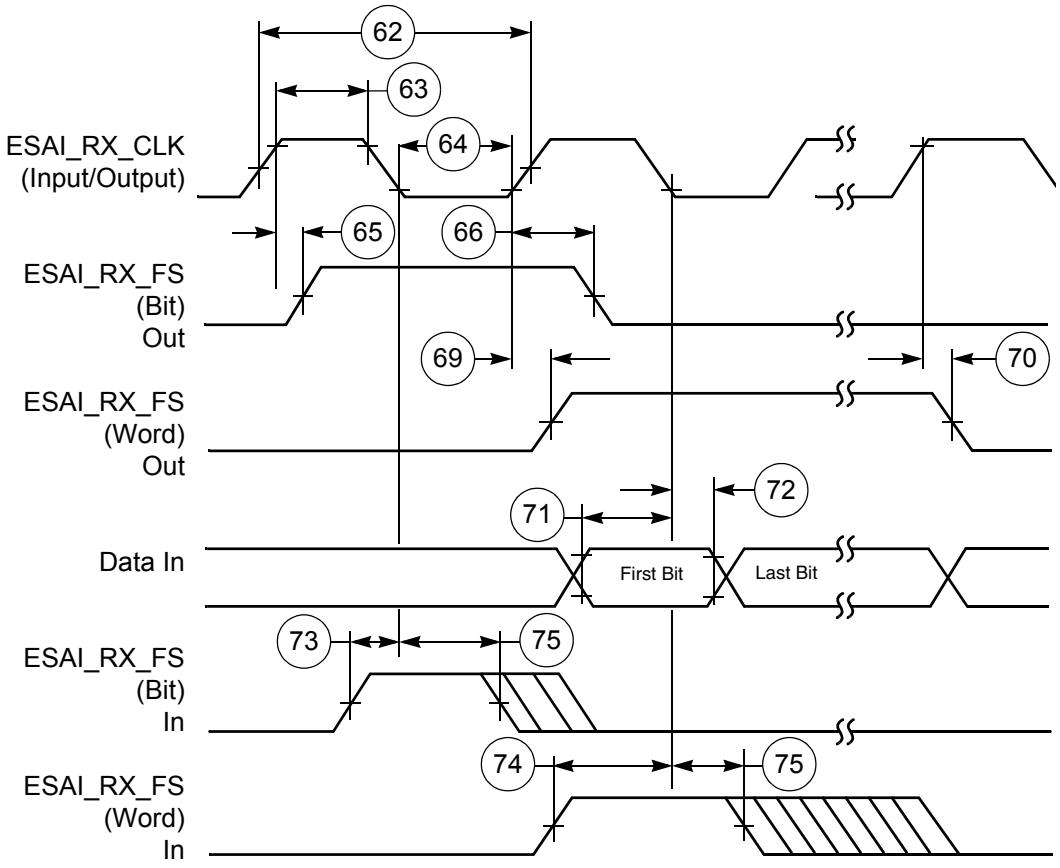

Figure 38. ESAI Receiver Timing

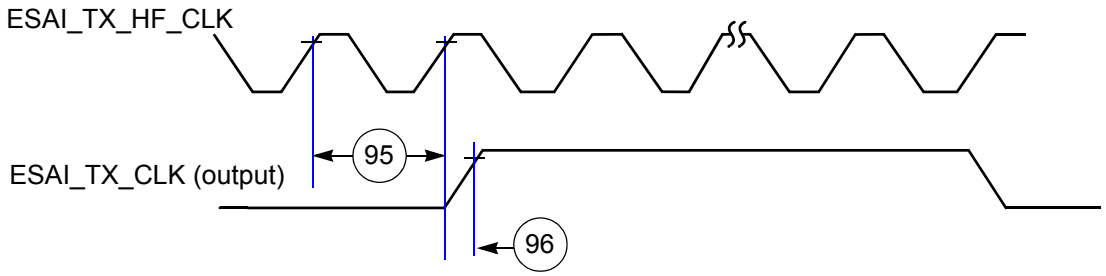

Figure 39. ESAI ESAI_TX_HF_CLK Timing

Table 50. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.4.2 eMMC4.4/4.41 (Dual Data Rate) AC Timing

Figure 41 depicts the timing of eMMC4.4/4.41. Table 51 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

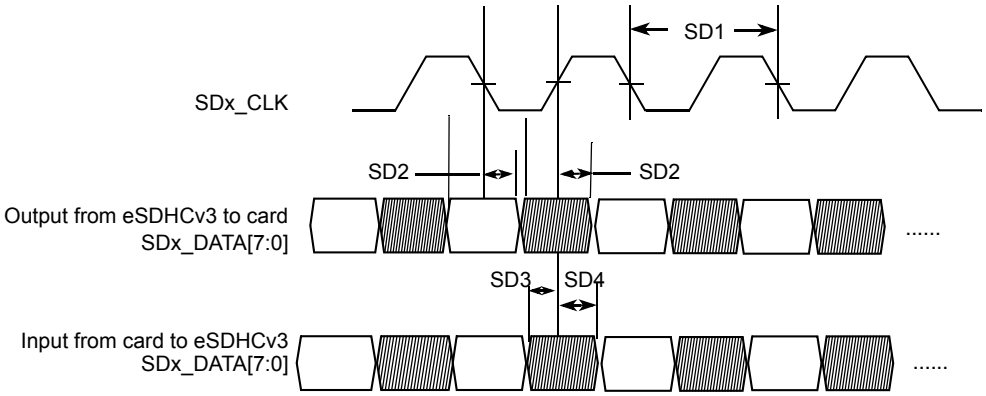

Figure 41. eMMC4.4/4.41 Timing

Table 51. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.12.10.2 DDR Mode

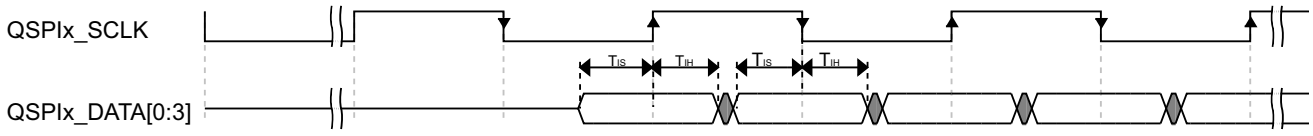

Figure 54. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 65. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

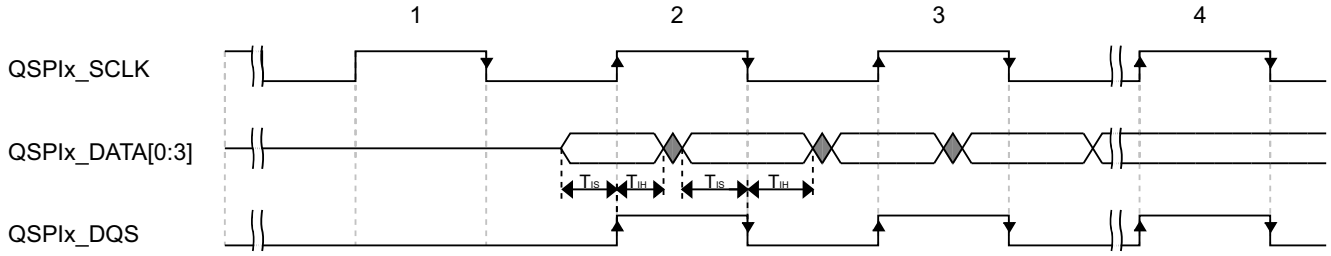

Figure 55. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Table 66. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

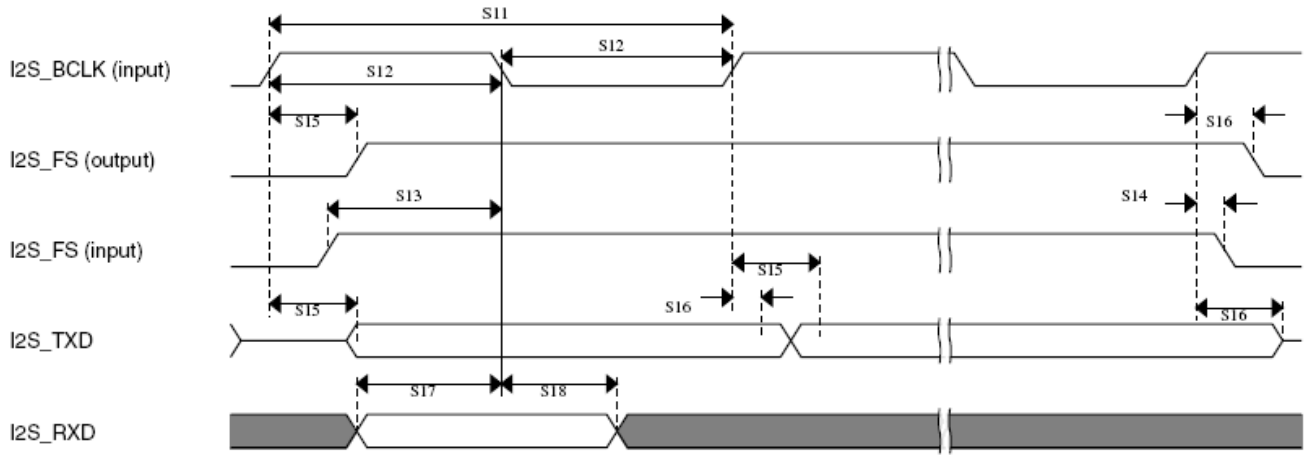

Figure 58. SAI Timing — Slave Modes

4.12.12 SCAN JTAG Controller (SJC) Timing Parameters

Figure 59 depicts the SJC test clock input timing. Figure 60 depicts the SJC boundary scan timing. Figure 61 depicts the SJC test access port. Signal parameters are listed in Table 70.

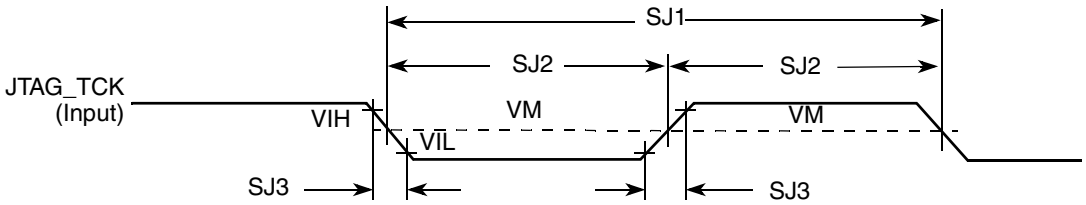

Figure 59. Test Clock Input Timing Diagram

Table 79. QSPI Boot trough QSPI (continued)

NAND_READY_B	qspi.A_DATA[0]	Alt2	Yes	Yes					
NAND_CE0_B	qspi.A_DATA[1]	Alt2	Yes	Yes					
NAND_CE1_B	qspi.A_DATA[2]	Alt2	Yes	Yes					
NAND_CLE	qspi.A_DATA[3]	Alt2	Yes	Yes					
NAND_DATA05	qspi.B_DATA[3]	Alt2					Yes		
NAND_DATA04	qspi.B_DATA[2]	Alt2					Yes		
NAND_DATA03	qspi.B_DATA[1]	Alt2					Yes		
NAND_DATA02	qspi.B_DATA[0]	Alt2					Yes		
NAND_WE_B	qspi.B_SS0_B	Alt2					Yes		
NAND_RE_B	qspi.B_SCLK	Alt2					Yes		
NAND_DATA07	qspi.A_SS1_B	Alt2				Yes			
NAND_ALE	qspi.A_DQS	Alt2			Yes				
NAND_DATA00	qspi.B_SS1_B	Alt2							Yes
NAND_DATA01	qspi.B_DQS	Alt2						Yes	

Table 80. SPI Boot through ECSPI1

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4 [5:4]=01b	BOOT_CFG4 [5:4]=10b	BOOT_CFG4 [5:4]=11b
CSI_DATA07	ecspi1.MISO	Alt 3	Yes				
CSI_DATA06	ecspi1.MOSI	Alt 3	Yes				
CSI_DATA04	ecspi1.SCLK	Alt 3	Yes				
CSI_DATA05	ecspi1.SS0	Alt 3		Yes			
LCD_DATA05	ecspi1.SS1	Alt 8			Yes		
LCD_DATA06	ecspi1.SS2	Alt 8				Yes	
LCD_DATA07	ecspi1.SS3	Alt 8					Yes

Table 81. SPI Boot through ECSPI2

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG 4[5:4]=00b	BOOT_CFG4 [5:4]=01b	BOOT_CFG4 [5:4]=10b	BOOT_CFG4 [5:4]=11b
CSI_DATA03	ecspi2.MISO	Alt 3	Yes				
CSI_DATA02	ecspi2.MOSI	Alt 3	Yes				
CSI_DATA00	ecspi2.SCLK	Alt 3	Yes				
CSI_DATA01	ecspi2.SS0	Alt 3		Yes			
LCD_HSYNC	ecspi2.SS1	Alt 8			Yes		

Table 86. SD/MMC Boot through USDHC2

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)
NAND_RE_B	usdhc2.CLK	Alt 1	Yes			
NAND_WE_B	usdhc2.CMD	Alt 1	Yes			
NAND_DATA00	usdhc2.DATA0	Alt 1	Yes			
NAND_DATA01	usdhc2.DATA1	Alt 1		Yes	Yes	
NAND_DATA02	usdhc2.DATA2	Alt 1		Yes	Yes	
NAND_DATA03	usdhc2.DATA3	Alt 1	Yes			
NAND_DATA04	usdhc2.DATA4	Alt 1			Yes	
NAND_DATA05	usdhc2.DATA5	Alt 1			Yes	
NAND_DATA06	usdhc2.DATA6	Alt 1			Yes	
NAND_DATA07	usdhc2.DATA7	Alt 1			Yes	
NAND_ALE	NAND_ALE[1]	Alt 5				Yes
GPIO1_IO08	usdhc2.VSELECT	Alt 4				Yes

1 The Boot ROM uses NAND_ALE to implement SD2_RESET_B.

Table 87. NOR/OneNAND Boot through EIM

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
CSI_DATA00	weim.AD[0]	Alt 4	Yes		
CSI_DATA01	weim.AD[1]	Alt 4	Yes		
CSI_DATA02	weim.AD[2]	Alt 4	Yes		
CSI_DATA03	weim.AD[3]	Alt 4	Yes		
CSI_DATA04	weim.AD[4]	Alt 4	Yes		
CSI_DATA05	weim.AD[5]	Alt 4	Yes		
CSI_DATA06	weim.AD[6]	Alt 4	Yes		
CSI_DATA07	weim.AD[7]	Alt 4	Yes		
NAND_DATA00	weim.AD[8]	Alt 4	Yes		
NAND_DATA01	weim.AD[9]	Alt 4	Yes		
NAND_DATA02	weim.AD[10]	Alt 4	Yes		
NAND_DATA03	weim.AD[11]	Alt 4	Yes		
NAND_DATA04	weim.AD[12]	Alt 4	Yes		
NAND_DATA05	weim.AD[13]	Alt 4	Yes		
NAND_DATA06	weim.AD[14]	Alt 4	Yes		

Table 87. NOR/OneNAND Boot through EIM (continued)

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
NAND_DATA07	weim.AD[15]	Alt 4	Yes		
NAND_CLE	weim.ADDR[16]	Alt 4		Yes	Yes
NAND_ALE	weim.ADDR[17]	Alt 4		Yes	Yes
NAND_CE1_B	weim.ADDR[18]	Alt 4		Yes	Yes
SD1_CMD	weim.ADDR[19]	Alt 4		Yes	Yes
SD1_CLK	weim.ADDR[20]	Alt 4		Yes	Yes
SD1_DATA0	weim.ADDR[21]	Alt 4		Yes	Yes
SD1_DATA1	weim.ADDR[22]	Alt 4		Yes	Yes
SD1_DATA2	weim.ADDR[23]	Alt 4		Yes	Yes
SD1_DATA3	weim.ADDR[24]	Alt 4		Yes	Yes
ENET2_RXER	weim.ADDR[25]	Alt 4		Yes	Yes
ENET2_CRS_DV	weim.ADDR[26]	Alt 4		Yes	Yes
CSI_MCLK	weim.CS0_B	Alt 4	Yes		
LCD_DATA08	weim.DATA[0]	Alt 4		Yes	
LCD_DATA09	weim.DATA[1]	Alt 4		Yes	
LCD_DATA10	weim.DATA[2]	Alt 4		Yes	
LCD_DATA11	weim.DATA[3]	Alt 4		Yes	
LCD_DATA12	weim.DATA[4]	Alt 4		Yes	
LCD_DATA13	weim.DATA[5]	Alt 4		Yes	
LCD_DATA14	weim.DATA[6]	Alt 4		Yes	
LCD_DATA15	weim.DATA[7]	Alt 4		Yes	
LCD_DATA16	weim.DATA[8]	Alt 4		Yes	
LCD_DATA17	weim.DATA[9]	Alt 4		Yes	
LCD_DATA18	weim.DATA[10]	Alt 4		Yes	
LCD_DATA19	weim.DATA[11]	Alt 4		Yes	
LCD_DATA20	weim.DATA[12]	Alt 4		Yes	
LCD_DATA21	weim.DATA[13]	Alt 4		Yes	
LCD_DATA22	weim.DATA[14]	Alt 4		Yes	
LCD_DATA23	weim.DATA[15]	Alt 4		Yes	
NAND_RE_B	weim.EB_B[0]	Alt 4		Yes	Yes
NAND_WE_B	weim.EB_B[1]	Alt 4		Yes	Yes
CSI_HSYNC	weim.LBA_B	Alt 4	Yes		

Table 91. 14 x 14 mm Functional Contact Assignments (continued)

DRAM_DATA09	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	R1	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	T7	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	T3	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	N1	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	F1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	M5	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	G4	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	M1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	K2	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	M3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	J3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	P2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	P1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	P7	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

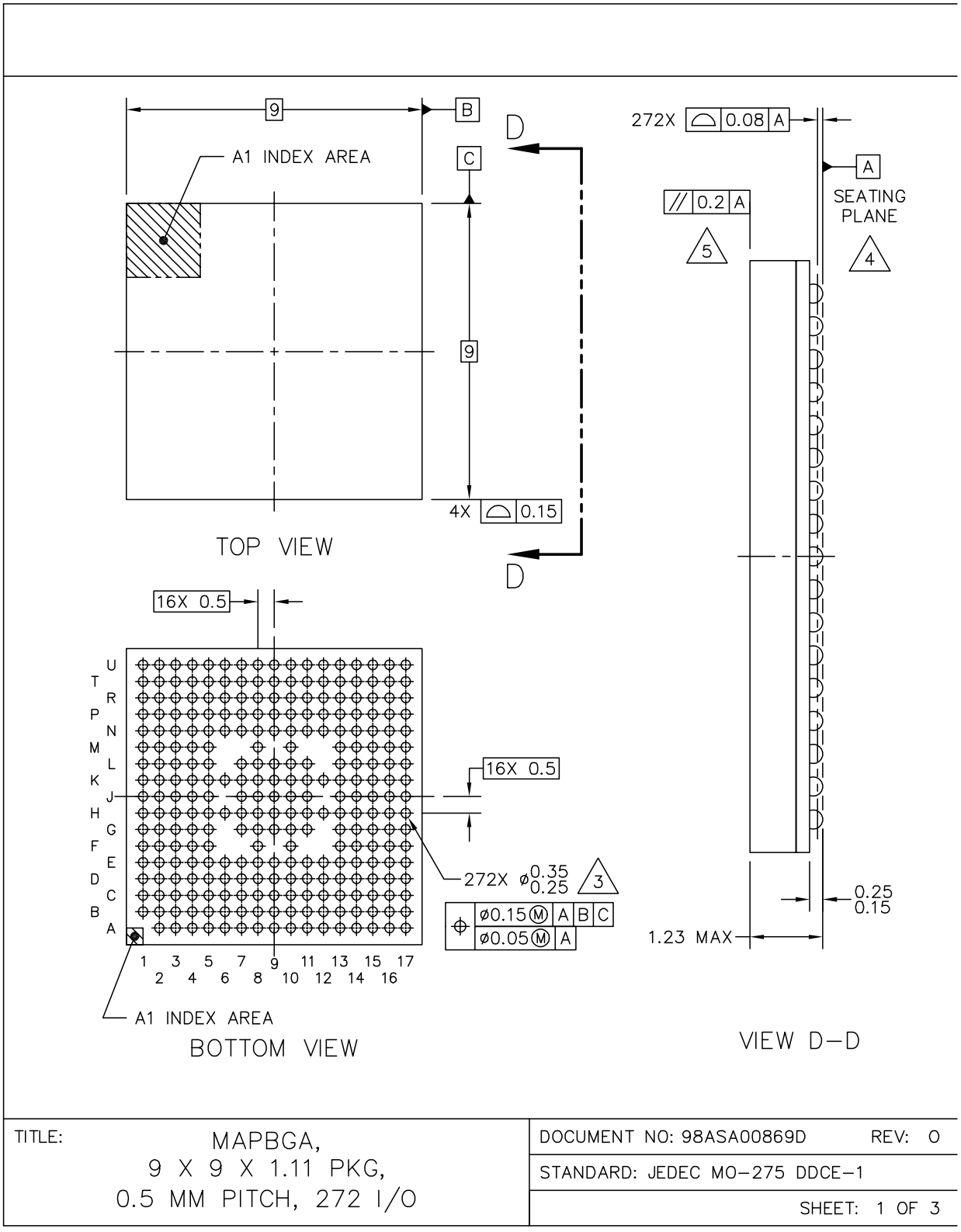

Figure 71. 9 x 9 mm BGA, Case x Package Top, Bottom, and Side Views

Table 94. 9 x 9 mm Functional Contact Assignments (continued)

DRAM_SDQS0_P	P5	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	100 kΩ pull-down
DRAM_SDQS1_N	N4	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	100 kΩ pull-down
DRAM_SDQS1_P	N3	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_N	Input	100 kΩ pull-down
DRAM_SDWE_B	F4	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	100 kΩ pull-up
DRAM_ZQPAD	T2	NVCC_DRAM	GPIO	—	DRAM_ZQPAD	Input	Keeper
ENET1_RX_DATA0	G17	NVCC_ENET	GPIO	ALT5	GPIO2_IO0	Input	Keeper
ENET1_RX_DATA1	F16	NVCC_ENET	GPIO	ALT5	GPIO2_IO1	Input	Keeper
ENET1_RX_EN	G16	NVCC_ENET	GPIO	ALT5	GPIO2_IO2	Input	Keeper
ENET1_RX_ER	G14	NVCC_ENET	GPIO	ALT5	GPIO2_IO7	Input	Keeper
ENET1_TX_CLK	G15	NVCC_ENET	GPIO	ALT5	GPIO2_IO6	Input	Keeper
ENET1_TX_DATA0	E16	NVCC_ENET	GPIO	ALT5	GPIO2_IO3	Input	Keeper
ENET1_TX_DATA1	F13	NVCC_ENET	GPIO	ALT5	GPIO2_IO4	Input	Keeper
ENET1_TX_EN	F15	NVCC_ENET	GPIO	ALT5	GPIO2_IO5	Input	Keeper
ENET2_RX_DATA0	E17	NVCC_ENET	GPIO	ALT5	GPIO2_IO8	Input	Keeper
ENET2_RX_DATA1	D17	NVCC_ENET	GPIO	ALT5	GPIO2_IO9	Input	Keeper
ENET2_RX_EN	D16	NVCC_ENET	GPIO	ALT5	GPIO2_IO10	Input	Keeper
ENET2_RX_ER	H13	NVCC_ENET	GPIO	ALT5	GPIO2_IO15	Input	Keeper
ENET2_TX_CLK	H14	NVCC_ENET	GPIO	ALT5	GPIO2_IO14	Input	Keeper
ENET2_TX_DATA0	E14	NVCC_ENET	GPIO	ALT5	GPIO2_IO11	Input	Keeper
ENET2_TX_DATA1	F14	NVCC_ENET	GPIO	ALT5	GPIO2_IO12	Input	Keeper
ENET2_TX_EN	E15	NVCC_ENET	GPIO	ALT5	GPIO2_IO13	Input	Keeper
GPIO1_IO00	M14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	M15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	M16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	N16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	N17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	P15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	N15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	N14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	P14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	P16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper