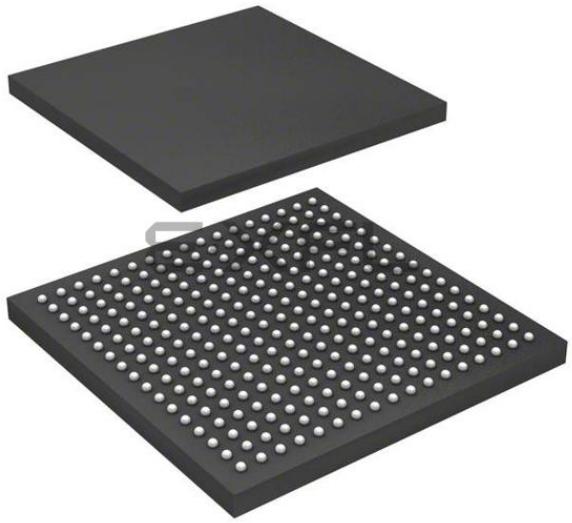

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	900MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Electrophoretic, LCD
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	A-HAB, ARM TZ, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6y7dvm09aa

Table 10. Operating Ranges (continued)

Low Power Run Mode: LDO Bypassed	VDD_SOC_IN	All PLL bypassed, all clocks running at 24 MHz or below.	0.925	—	1.3	V	—
SUSPEND (DSM) Mode	VDD_SOC_IN	—	0.9	—	1.3	V	Refer to Table 15 Low Power Mode Current and Power Consumption on page -29
VDD_HIGH internal regulator	VDD_HIGH_IN	—	2.80	—	3.6	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[2]	—	2.40	—	3.6	V	Can be combined with VDDHIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS	—	4.40	—	5.5	V	—
	USB_OTG2_VBUS	—	4.40	—	5.5	V	—
DDR I/O supply	NVCC_DRAM	LPDDR2	1.14	1.2	1.3	V	—
		DDR3L	1.28	1.35	1.45	V	—
		DDR3	1.43	1.5	1.575	V	—
	NVCC_DRAM2P5	—	2.25	2.5	2.75	V	—
GPIO supplies	NVCC_CSI	—	1.65	1.8, 2.8, 3.3	3.6	V	All digital I/O supplies (NVCC_xxxx) must be powered (unless otherwise specified in this data sheet) under normal conditions whether the associated I/O pins are in use or not.
	NVCC_ENET						
	NVCC_GPIO						
	NVCC_UART						
	NVCC_LCD						
	NVCC_NAND						
	NVCC_SD1						
A/D converter	VDDA_ADC_3P3	—	3.0	3.15	3.6	V	VDDA_ADC_3P3 must be powered when chip is in RUN mode, IDLE mode, or SUSPEND mode. VDDA_ADC_3P3 should not be powered when chip is in SNVS mode.
Temperature Operating Ranges							
Junction temperature	TJ	Standard Commercial	0	—	95	°C	See *i.MX 6ULL Product Lifetime Usage Estimates* for information on product lifetime (power-on years) for this processor.

[1] Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This result in an optimized power/speed ratio.

— At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
— Higher accuracy than ring oscillator
— If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum Supply Currents

The data shown in Table 13 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

See the i.MX 6ULL Power Consumption Measurement Application Note (AN4581) for more details on typical power consumption under various use case definitions.

Table 13. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_SOC_IN	900 MHz Arm clock based on Dhrystone test	500	mA
VDD_HIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	500[2]	μA
USB_OTG1_VBUS USB_OTG2_VBUS	—	50[3]	mA
VDDA_ADC_3P3	100 Ohm maximum loading for touch panel	35	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	(See[4])	—
NVCC_DRAM_2P5	—	50	mA
NVCC_GPIO	N=16	Use maximum IO Equation[5]	—
NVCC_UART	N=16	Use maximum IO equation[5]	—
NVCC_ENET	N=16	Use maximum IO equation[5]	—
NVCC_LCD	N=29	Use maximum IO equation[5]	—
NVCC_NAND	N=17	Use maximum IO equation[5]	—
NVCC_SD	N=6	Use maximum IO equation[5]	—
NVCC_CSI	N=12	Use maximum IO equation[5]	—
MISC			
DRAM_VREF	—	1	mA

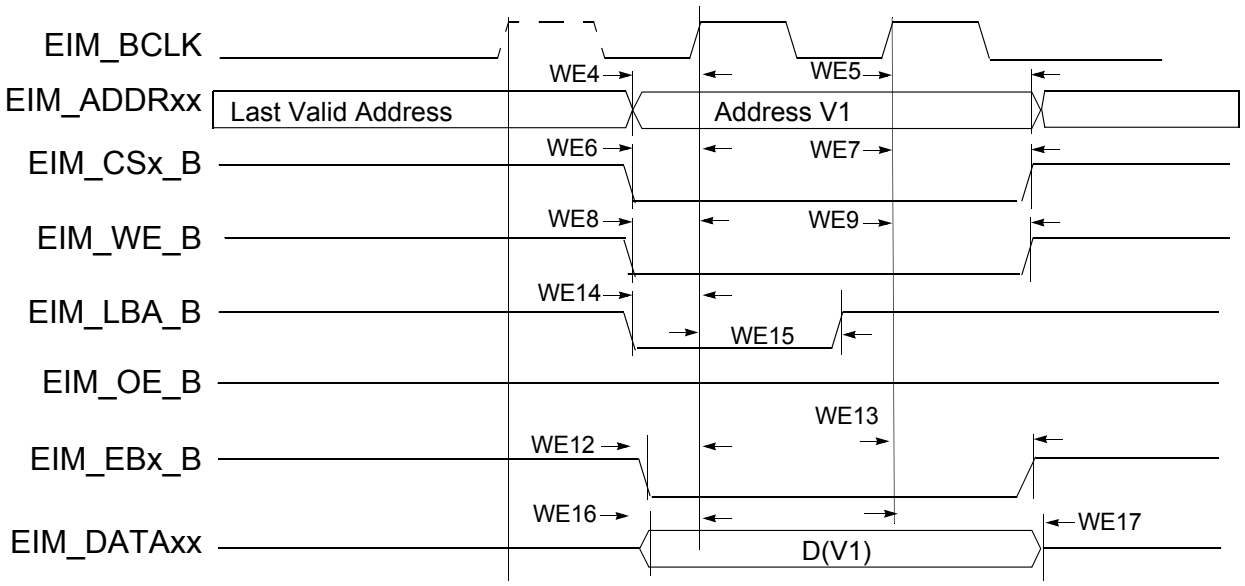

Figure 12. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

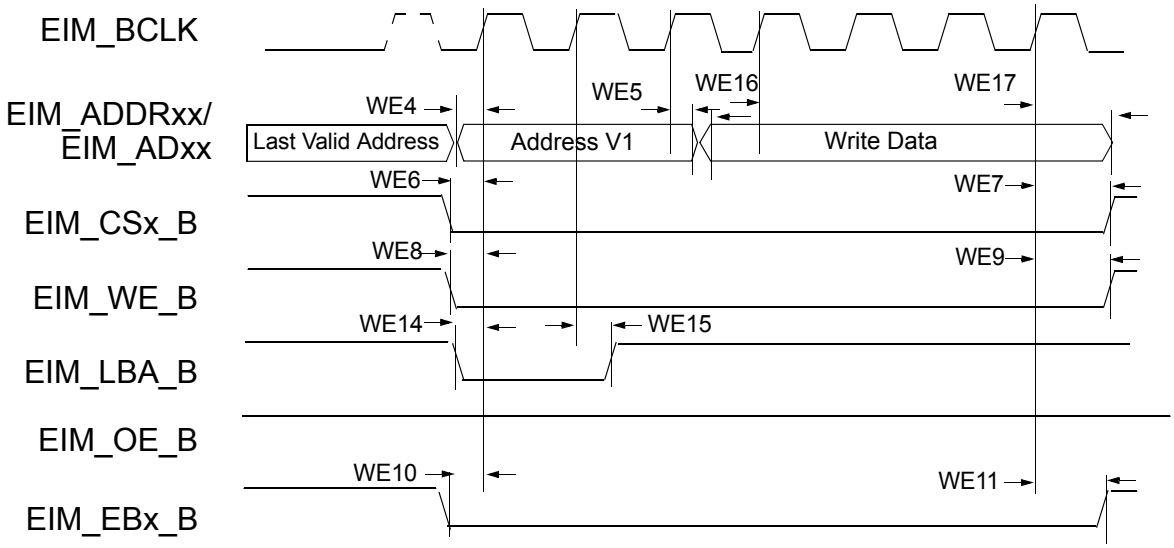

Figure 13. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

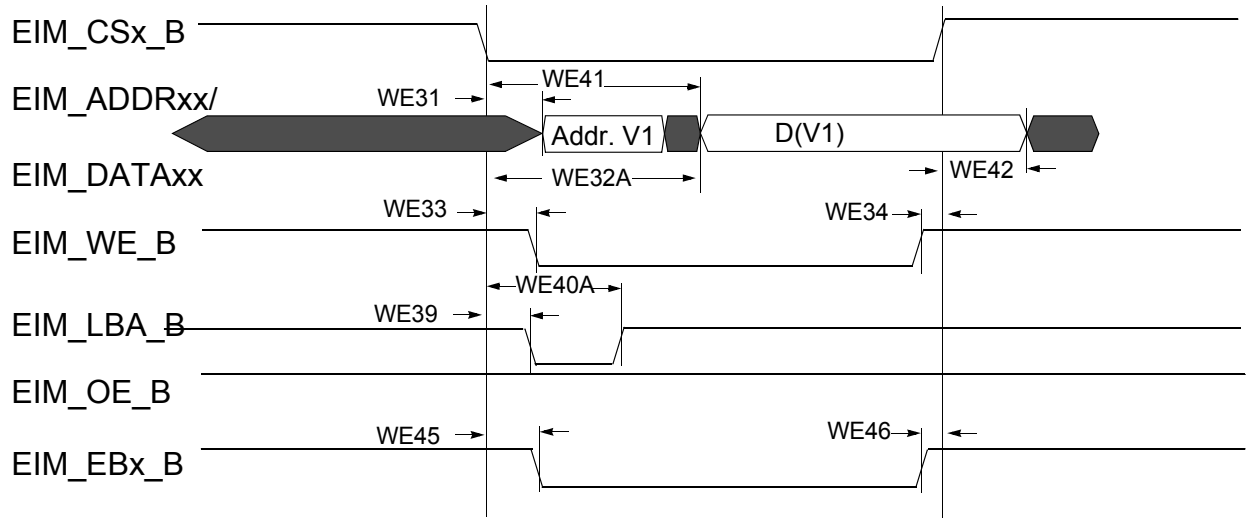

Figure 18. Asynchronous A/D Muxed Write Access

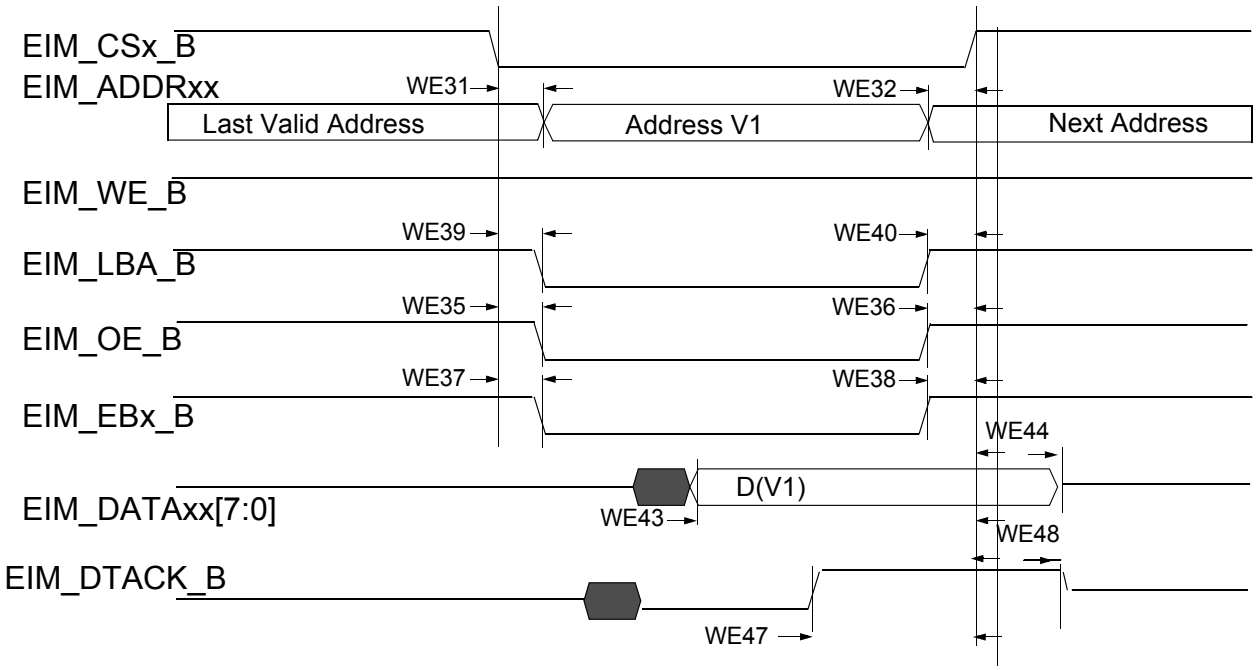

Figure 19. DTACK Mode Read Access (DAP=0)

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip to Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
MAXDTI	MAXIMUM delay from EIM_DTACK_B to its internal FF + 2 cycles for synchronization	10	—	—	—
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B Invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the *i.MX 6ULL Reference Manual* (IMX6ULLRM).

2 In this table, CSA means WCSA when write operation or RCSA when read operation.

3 In this table, CSN means WCSN when write operation or RCSN when read operation.

4 t is axi_clk cycle time.

5 In this table, ADVN means WADVN when write operation or RADVN when read operation.

6 In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.10 Multi-Mode DDR Controller (MMDC)

The Multi-Mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.10.1 MMDC compatibility with JEDEC-compliant SDRAMs

The i.MX 6ULL MMDC supports the following memory types:

- LPDDR2 SDRAM compliant with JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant with JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6ULL Applications Processor (IMX6ULLHDG)*.

4.10.2 MMDC supported DDR3/DDR3L/LPDDR2 configurations

Table 41 shows the supported DDR3/DDR3L/LPDDR2 configurations:

Table 41. i.MX 6ULL Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	DDR3	DDR3L	LDDDR2
Clock frequency	400 MHz	400 MHz	400 MHz
Bus width	16-bit	16-bit	16-bit
Channel	Single	Single	Single
Chip selects	2	2	2

4.12.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.12.2.1 ECSPI Master Mode Timing

Figure 35 depicts the timing of ECSPI in master mode. Table 47 lists the ECSPI master mode timing characteristics.

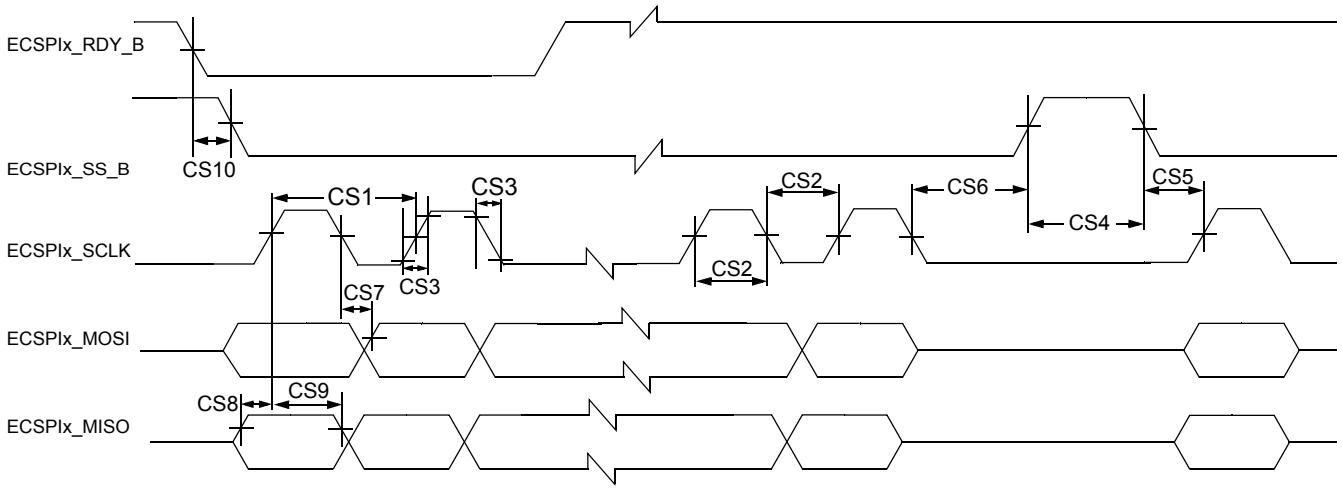

Figure 35. ECSPI Master Mode Timing Diagram

Table 47. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	14	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.7, “I/O AC Parameters”.”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.2.2 ECSPI Slave Mode Timing

Figure 36 depicts the timing of ECSPI in slave mode. Table 48 lists the ECSPI slave mode timing characteristics.

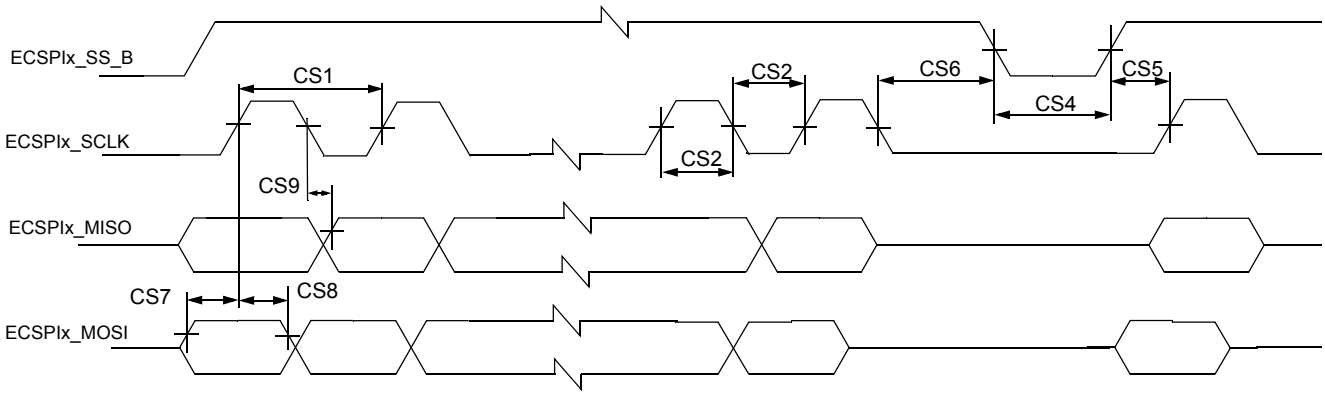

Figure 36. ECSPI Slave Mode Timing Diagram

Table 48. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

4.12.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 49 shows the interface timing values. The number field in the table refers to timing signals found in Figure 37 and Figure 38.

Table 49. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
85	ESAI_TX_CLK rising edge to transmitter #0 drive enable assertion	— —	— —	— —	17.0 11.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
88	ESAI_TX_CLK rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	14.0 9.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
92	ESAI_TX_FS input (wl) to data out enable from high impedance	—	—	—	21.0	—	ns
93	ESAI_TX_FS input (wl) to transmitter #0 drive enable assertion	—	—	—	14.0	—	ns
94	Flag output valid after ESAI_TX_CLK rising edge	—	—	— —	14.0 9.0	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	$2 \times T_C$	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

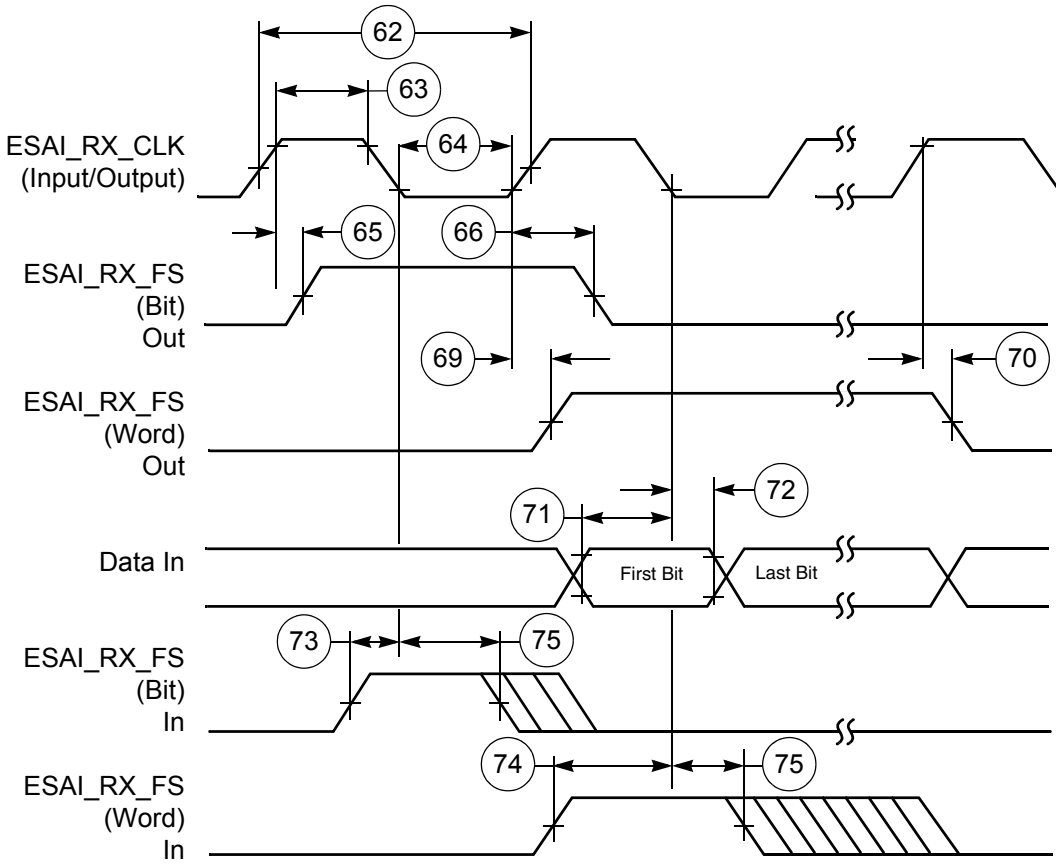

Figure 38. ESAI Receiver Timing

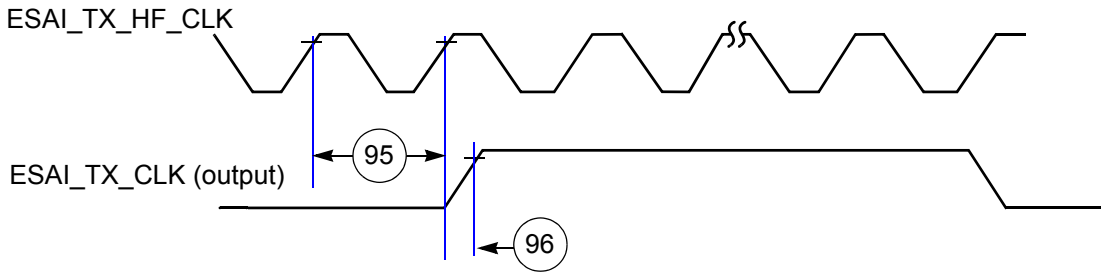

Figure 39. ESAI ESAI_TX_HF_CLK Timing

Figure 48 shows RMII mode timings. Table 58 describes the timing parameters (M16–M21) shown in the figure.

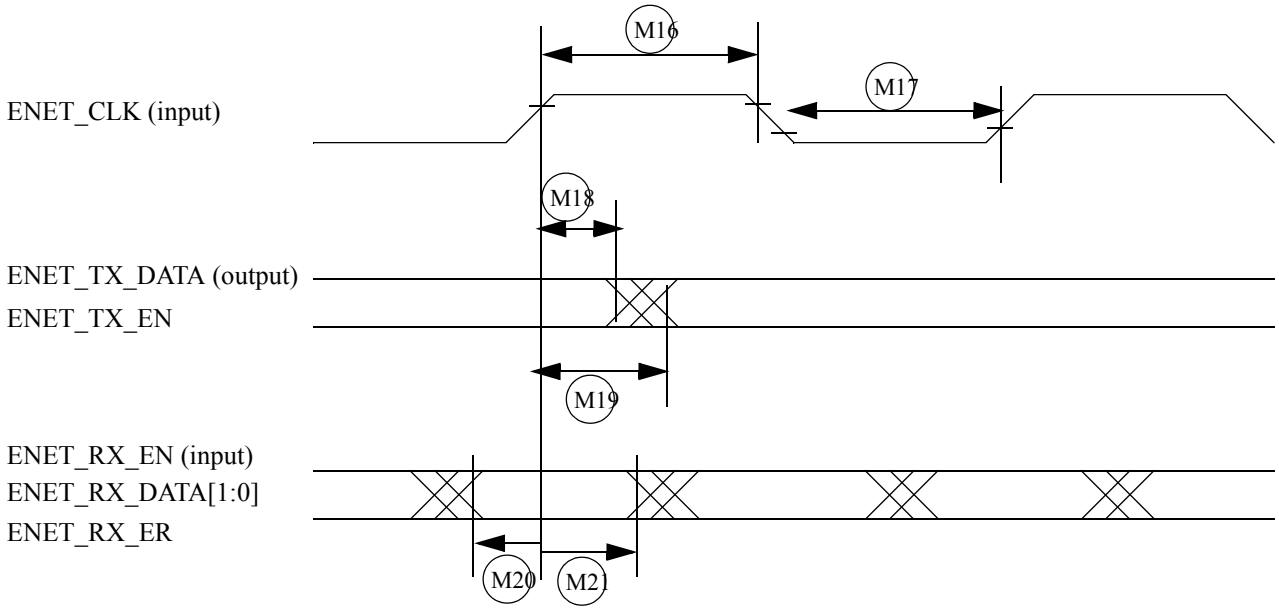

Figure 48. RMII Mode Signal Timing Diagram

Table 58. RMII Signal Timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	13	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	2	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.12.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6ULL Reference Manual* (IMX6ULLRM) to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.12.10 QUAD SPI (QSPI) Timing Parameters

Measurement conditions are with 35 pF load on SCK and SIO pins and input slew rate of 1 V/ns.

4.12.10.1 SDR Mode

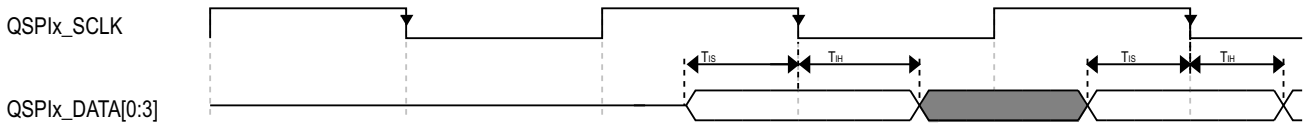

Figure 51. QuadSPI Input/Read Timing (SDR mode with internal sampling)

Table 62. QuadSPI Input Timing (SDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

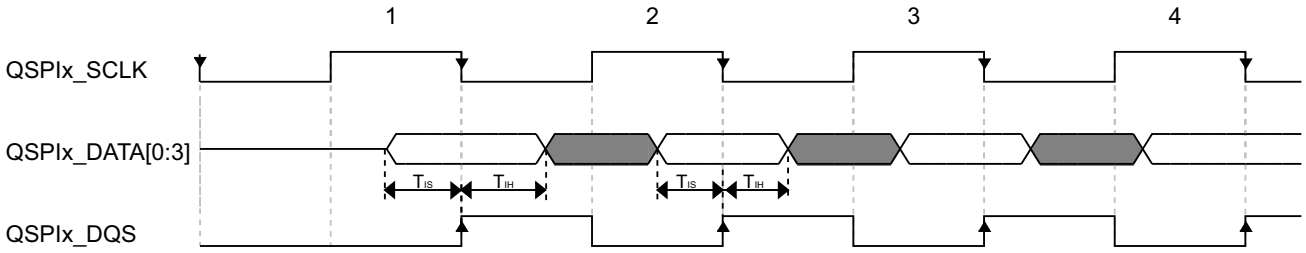

Figure 52. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Table 63. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

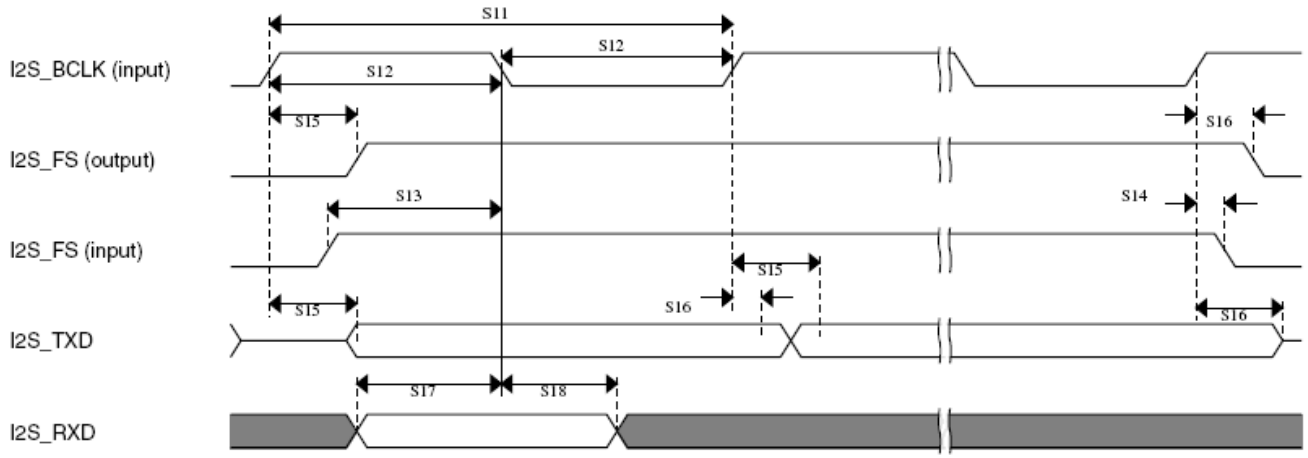

Figure 58. SAI Timing — Slave Modes

4.12.12 SCAN JTAG Controller (SJC) Timing Parameters

Figure 59 depicts the SJC test clock input timing. Figure 60 depicts the SJC boundary scan timing. Figure 61 depicts the SJC test access port. Signal parameters are listed in Table 70.

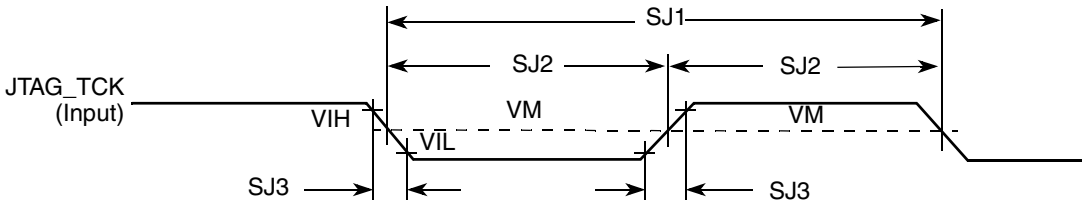

Figure 59. Test Clock Input Timing Diagram

Table 70. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.12.13 SPDIF Timing Parameters

The Sony/Philips Digital Interface Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 71, Figure 63, and Figure 64 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 71. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

Table 76. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	—	40	MHz	—
	ADLPC=0, ADHSC=0 12 bit mode		4	—	30	MHz	—
	ADLPC=1, ADHSC=0 12 bit mode		4	—	20	MHz	—

1 Typical values assume VDDAD = 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential differences

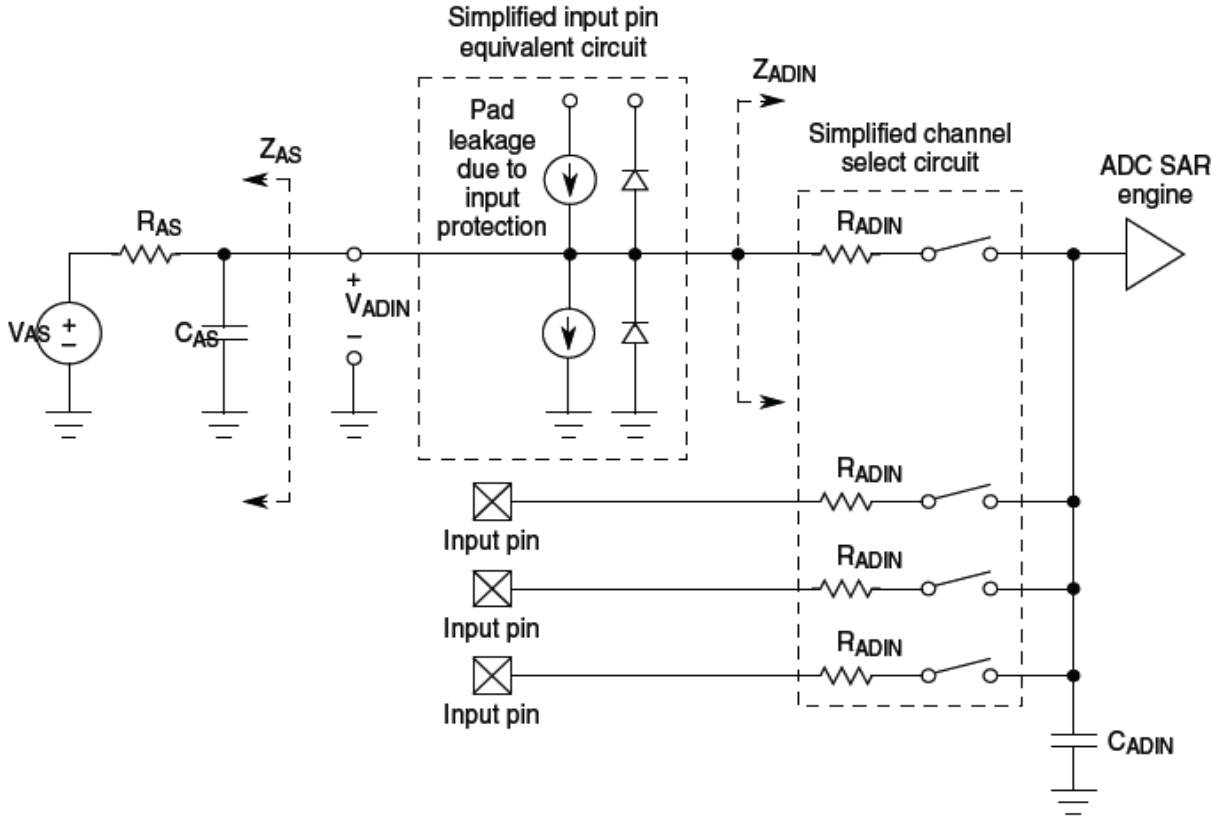

Figure 69. 12-bit ADC Input Impedance Equivalency Diagram

Table 77. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv	—	28	—	cycles	—
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv	—	0.7	—	µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
[P:][C:] Total Unadjusted Error	12 bit mode	TUE	—	4.5	—	LSB 1 LSB = (V_{REFH} - V_{REFL})/2 N	—
	10 bit mode		—	2	—		
	8 bit mode		—	1.5	—		
[P:][C:] Differential Non-Linearity	12 bit mode	DNL	—	1	—	LSB	—
	10bit mode		—	0.5	—		
	8 bit mode		—	0.2	—		

6.1.2 14 x 14 mm Supplies Contact Assignments and Functional Contact Assignments

Table 90 shows the device connection list for ground, sense, and reference contact signals.

Table 90. 14 x 14 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	M13	—
DRAM_VREF	P4	—
GPANIO	R13	—
NGND_KEL0	M12	—
NVCC_CSI	F4	—
NVCC_DRAM	G6, H6, J6, K6, L6, M6	—
NVCC_DRAM_2P5	N6	—
NVCC_ENET	F13	—
NVCC_GPIO	J13	—
NVCC_LCD	E13	—
NVCC_NAND	E7	—
NVCC_PLL	P13	—
NVCC_SD1	C4	—
NVCC_UART	H13	—
VDD_ARM_CAP	G9, G10, G11, H11	—
VDD_HIGH_CAP	R14, R15	—
VDD_HIGH_IN	N13	—
VDD_SNVS_CAP	N12	—
VDD_SNVS_IN	P12	—
VDD_SOC_CAP	G8, H8, J8, J11, K8, K11, L8, L9, L10, L11	—
VDD_SOC_IN	H9, H10, J9, J10, K9, 10	—
VDD_USB_CAP	R12	—
VDDA_ADC_3P3	L13	—
VSS	A1, A17, C3, C7, C11, C15, E8, E11, F6, F7, F8, F9, F10,F11, F12, G3, G5, G7, G12, G15, H7, H12, J5, J7, J12, K7, K12, L3, L7, L12, M7, M8, M9, M10, M11, N3, N5, R3, R5, R7, R11, R16, R17, T14, U1, U14, U17	—

Table 91. 14 x 14 mm Functional Contact Assignments (continued)

UART1_TX_DATA	K14	NVCC_UART	GPIO	ALT5	GPIO1_IO16	Input	Keeper
UART2_CTS_B	J15	NVCC_UART	GPIO	ALT5	GPIO1_IO22	Input	Keeper
UART2_RTS_B	H14	NVCC_UART	GPIO	ALT5	GPIO1_IO23	Input	Keeper
UART2_RX_DATA	J16	NVCC_UART	GPIO	ALT5	GPIO1_IO21	Input	Keeper
UART2_TX_DATA	J17	NVCC_UART	GPIO	ALT5	GPIO1_IO20	Input	Keeper
UART3_CTS_B	H15	NVCC_UART	GPIO	ALT5	GPIO1_IO26	Input	Keeper
UART3_RTS_B	G14	NVCC_UART	GPIO	ALT5	GPIO1_IO27	Input	Keeper
UART3_RX_DATA	H16	NVCC_UART	GPIO	ALT5	GPIO1_IO25	Input	Keeper
UART3_TX_DATA	H17	NVCC_UART	GPIO	ALT5	GPIO1_IO24	Input	Keeper
UART4_RX_DATA	G16	NVCC_UART	GPIO	ALT5	GPIO1_IO29	Input	Keeper
UART4_TX_DATA	G17	NVCC_UART	GPIO	ALT5	GPIO1_IO28	Input	Keeper
UART5_RX_DATA	G13	NVCC_UART	GPIO	ALT5	GPIO1_IO31	Input	Keeper
UART5_TX_DATA	F17	NVCC_UART	GPIO	ALT5	GPIO1_IO30	Input	Keeper
USB_OTG1_CHD_B	U16	OPEN DRAIN	GPIO	—	USB_OTG1_CHD_B	—	—
USB_OTG1_DN	T15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DN	—	—
USB_OTG1_DP	U15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DP	—	—
USB_OTG1_VBUS	T12	USB_VBUS	VBUS POWER	—	USB_OTG1_VBUS	—	—
USB_OTG2_DN	T13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DN	—	—
USB_OTG2_DP	U13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DP	—	—
USB_OTG2_VBUS	U12	USB_VBUS	VBUS POWER	—	USB_OTG2_VBUS	—	—
XTALI	T16	NVCC_PLL	ANALOG	—	XTALI	—	—
XTALO	T17	NVCC_PLL	ANALOG	—	XTALO	—	—

[1] SNVS_TAMPER0 to SNVS_TAMPER9 can be configured as GPIO or tamper detection pin, it is depending on the fuse setting TAMPER_PIN_DISABLE[1:0]. When the pad is configured as GPIO, the value is keeper out of reset.

[2] SNVS_TAMPER0 to SNVS_TAMPER9 is input unconnected in the following conditions.

—SNVS low power mode when configured as GPIO

—Tamper functions are not used when configured as TAMPER detection pins

It is required to connect external 1M Ohm pull-up or pull-down resistors to the pad to avoid the undesired leakage under two conditions above.

6.1.3 14 x 14 mm, 0.8 mm Pitch, Ball Map

Table 92 shows the 14 x 14 mm, 0.8 mm pitch ball map for the i.MX 6ULL.

Table 92. 14 x 14 mm, 0.8 mm Pitch, Ball Map

	A	B	C	D	E	F	G
1	VSS	SD1_DATA2	SD1_CLK	CSI_DATA07	CSI_DATA03	DRAM_ODT1	DRAM_ADDR14
2	SD1_DATA3	SD1_DATA1	SD1_CMD	CSI_DATA06	CSI_DATA02	CSI_VSYNC	DRAM_ADDR06
3	NAND_READY_B	SD1_DATA0	VSS	CSI_DATA05	CSI_DATA01	CSI_HSYNC	VSS
4	NAND_CLE	NAND_ALE	NVCC_SD1	CSI_DATA04	CSI_DATA00	NVCC_CSI	DRAM_RESET
5	NAND_DATA07	NAND_CE1_B	NAND_CE0_B	NAND_WP_B	CSI_PIXCLK	CSI_MCLK	VSS
6	NAND_DATA06	NAND_DATA05	NAND_DATA04	NAND_DATA03	NAND_DQS	VSS	NVCC_DRAM
7	NAND_DATA02	NAND_DATA01	VSS	NAND_DATA00	NVCC_NAND	VSS	VSS
8	LCD_CLK	LCD_ENABLE	NAND_WE_B	NAND_RE_B	VSS	VSS	VDD_SOC_CAP
9	LCD_DATA01	LCD_DATA00	LCD_VSYNC	LCD_HSYNC	LCD_RESET	VSS	VDD_ARM_CAP
10	LCD_DATA06	LCD_DATA05	LCD_DATA04	LCD_DATA03	LCD_DATA02	VSS	VDD_ARM_CAP
11	LCD_DATA09	LCD_DATA08	VSS	LCD_DATA07	VSS	VSS	VDD_ARM_CAP
12	LCD_DATA14	LCD_DATA13	LCD_DATA12	LCD_DATA11	LCD_DATA10	VSS	VSS
13	LCD_DATA18	LCD_DATA17	LCD_DATA16	LCD_DATA15	NVCC_LCD	NVCC_ENET	UART5_RX_DATA
14	LCD_DATA22	LCD_DATA21	LCD_DATA20	LCD_DATA19	ENET1_TX_DATA1	ENET1_TX_CLK	UART3_RTS_B
15	ENET2_TX_DATA0	ENET2_TX_EN	VSS	ENET1_RX_ER	ENET1_TX_DATA0	ENET1_TX_EN	VSS
16	ENET2_TX_DATA1	LCD_DATA23	ENET2_RX_DATA1	ENET2_RX_ER	ENET1_RX_EN	ENET1_RX_DATA0	UART4_RX_DATA
17	VSS	ENET2_RX_EN	ENET2_RX_DATA0	ENET2_TX_CLK	ENET1_RX_DATA1	UART5_TX_DATA	UART4_TX_DATA
	A	B	C	D	E	F	G

6.2.2 9 x 9 mm Supplies Contact Assignments and Functional Contact Assignments

Table 93 shows the device connection list for ground, sense, and reference contact signals.

Table 93. 9 x 9 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	N13	—
DRAM_VREF	T1	—
GPANAIO	T11	—
NGND_KEL0	M10	—
NVCC_CSI	E5	—
NVCC_DRAM	G5, L5, M5, N6	—
NVCC_DRAM_2P5	K6	—
NVCC_ENET	G13	—
NVCC_GPIO	M13	—
NVCC_LCD	E13	—
NVCC_NAND	E11	—
NVCC_PLL	T13	—
NVCC_SD1	E7	—
NVCC_UART	L13	—
VDD_ARM_CAP	G9, G10, G11, H9, H10, H11	—
VDD_HIGH_CAP	U11	—
VDD_HIGH_IN	U15	—
VDD_SNVS_CAP	N12	—
VDD_SNVS_IN	P12	—
VDD_SOC_CAP	G7, G8, H7, H8, J7, J8, K7, K8, L7, L8	—
VDD_SOC_IN	J9, J10, J11, K9, K10, K11, L9, L10, L11	—
VDD_USB_CAP	N11	—
VDDA_ADC_3P3	T17	—
VSS	A2, A7, A12, A17, B1, C15, F1, F3, F8, F10, F17, H6, H12, J3, J15, K12, M1, M3, M8, M17, R3, R9, R12, R15, U1, U6, U13, U17	—

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