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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	·
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf84a-04-p

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.3.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as $000u \ uluu$ (where u = unchanged).

Only the BCF, BSF, SWAPF and MOVWF instructions should be used to alter the STATUS register (Table 7-2), because these instructions do not affect any status bit.

- Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F84A and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.
 - 2: The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.
 - 3: When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
	IRP	RP1	RP0	TO	PD	Z	DC	С
	bit 7					•	•	bit 0
bit 7-6	Unimplem	ented: Mair	ntain as '0'					
bit 5	RP0: Regis	ster Bank Se	elect bits (us	ed for direct	addressin	g)		
	01 = Bank	1 (80h - FF	h)					
	00 = Bank	0 (00h - 7Fi	n)					
bit 4	TO: Time-c	out bit			• ,			
	1 = After p $0 = \text{A WD}^2$	ower-up, CI T time-out o	CRWDT INStru	ction, or SL	EEP Instruc	tion		
bit 3	PD: Power	-down bit						
	1 = After p	ower-up or	by the CLRW	DT instruction	on			
	0 = By exe	ecution of the	e SLEEP ins	truction				
bit 2	Z: Zero bit							
	1 = The re	esult of an ar	ithmetic or l	ogic operati	on is zero			
	0 = The re	esult of an ar	ithmetic or l	ogic operati	on is not ze	ero		
bit 1	DC: Digit c is reversed	arry/borrow I)	bit (ADDWF, A	ADDLW,SUB	LW,SUBWF	instructions)	(for borrow,	the polarity
	1 = A carr 0 = No car	y-out from th rry-out from	ne 4th low or the 4th low o	der bit of th order bit of t	e result oco he result	curred		
bit 0	C : Carry/b reversed)	orrow bit (A)	DDWF, ADDL	W,SUBLW,S	UBWF ins	tructions) (fo	r borrow, the	e polarity is
	 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred 							
	Note:	A subtractio	on is execute	ed by adding	g the two's	complement	of the secor	nd operand.
		bit of the sc	ource registe	r.			ior the high	
	Legend:							
	R = Reada	ble bit	W = W	ritable bit	U = Uni	mplemented	bit, read as	'0'
	- n = Value a	at POR	'1' = Bit	is set	'0' = Bit i	s cleared	x = Bit is ur	nknown

4.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PIC[®] Mid-Range Reference Manual (DS33023).

4.1 PORTA and TRISA Registers

PORTA is a 5-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Note:	On a Power-on Reset, these pins are con-
	figured as inputs and read as '0'.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read. This value is modified and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

BCF	STATUS, RPO	;	
CLRF	PORTA	;	Initialize PORTA by
		;	clearing output
		;	data latches
BSF	STATUS, RPO	;	Select Bank 1
MOVLW	0x0F	;	Value used to
		;	initialize data
		;	direction
MOVWF	TRISA	;	Set RA<3:0> as inputs
		;	RA4 as output
		;	TRISA<7:5> are always
		;	read as '0'.

FIGURE 4-1:

BLOCK DIAGRAM OF PINS RA3:RA0



FIGURE 4-2:

BLOCK DIAGRAM OF PIN RA4



5.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution).

Note: To avoid an unintended device RESET, a specific instruction sequence (shown in the PIC[®] Mid-Range Reference Manual, DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

5.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut-off during SLEEP.





TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
01h	TMR0	Timer0	ïmer0 Module Register							xxxx xxxx	uuuu uuuu
0Bh,8Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	_	-		PORTA	Data Dire	ection Re	1 1111	1 1111		

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

6.2 Oscillator Configurations

6.2.1 OSCILLATOR TYPES

The PIC16F84A can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

6.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP, or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 6-1).

FIGURE 6-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



- Note 1: See Table 6-1 for recommended values of C1 and C2.
 - **2:** A series resistor (Rs) may be required for AT strip cut crystals.

The PIC16F84A oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP, or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 6-2).



TABLE 6-1:CAPACITOR SELECTION FOR
CERAMIC RESONATORS

Ranges Tested:							
Mode	Freq	OSC1/C1	OSC2/C2				
ХТ	455 kHz 2.0 MHz 4.0 MHz	47 - 100 pF 15 - 33 pF 15 - 33 pF	47 - 100 pF 15 - 33 pF 15 - 33 pF				
HS	8.0 MHz 10.0 MHz	15 - 33 pF 15 - 33 pF	15 - 33 pF 15 - 33 pF				
Note: Ro idu Hi of sta gu its cc ap ne	ecommended entical to the r gher capacita the oscillato art-up time. The idance only. a own charac onsult the reso opropriate val- ents.	values of C1 ranges tested nce increases r, but also in hese values a Since each re teristics, the onator manufa lues of exte	and C2 are in this table. Is the stability perceases the re for design esonator has user should cturer for the rnal compo-				

Note:	When using resonators with frequencies
	above 3.5 MHz, the use of HS mode rather
	than XT mode, is recommended. HS mode
	may be used at any VDD for which the
	controller is rated.

TABLE 6-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz	68 - 100 pF	68 - 100 pF
	200 kHz	15 - 33 pF	15 - 33 pF
XT	100 kHz	100 - 150 pF	100 - 150 pF
	2 MHz	15 - 33 pF	15 - 33 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS	4 MHz	15 - 33 pF	15 - 33 pF
	20 MHz	15 - 33 pF	15 - 33 pF
Note:	Higher capa of the oscill start-up time guidance on mode, as we driving crysta cation. Sinc characteristic crystal ma values of ext For VDD > 4. mended.	citance increas lator, but also ator, but also but also values ly. Rs may be all as XT mode als with low drive e each crysta cs, the user sho nufacturer for ternal compone $5V, C1 = C2 \approx 3$	es the stability increases the are for design required in HS to avoid over- ve level specifi- l has its own buld consult the r appropriate ents. 30 pF is recom-

6.2.3 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) values, capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low CEXT values. The user needs to take into account variation, due to tolerance of the external R and C components. Figure 6-3 shows how an R/C combination is connected to the PIC16F84A.



TABLE 7-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles		14-Bit	Opcode	Status	Notos	
		Description		MSb			LSb	Affected	Notes
	BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		-
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
		BIT-ORIENTED FILE REGIST		RATION	IS				
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
		LITERAL AND CONTROL	OPERAT	IONS					
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Note: Additional information on the mid-range instruction set is available in the PIC[®] Mid-Range MCU Family Reference Manual (DS33023).

XORLW	Exclusive OR Literal with W	XORWF	Exclusive OR W with f		
Syntax:	[<i>label</i>] XORLW k	Syntax:	[<i>label</i>] XORWF f,d		
Operands:	$0 \leq k \leq 255$	Operands:	$0 \le f \le 127$		
Operation:	(W) .XOR. $k \rightarrow (W)$		$a \in [0, 1]$		
Status Affected:	Z	Operation:	(W) .XOR. (f) \rightarrow (destination)		
Description: The contents of are XOR'ed with eral 'k'. The resu the W register.	The contents of the W register	Status Affected:	Z		
	are XOR'ed with the eight-bit lit- eral 'k'. The result is placed in the W register.	Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.		

8.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

8.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

8.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

8.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

8.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command line interface
- · Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

8.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit[™] 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit[™] 2 enables in-circuit debugging on most PIC[®] microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

8.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

8.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

9.1 DC Characteristics

PIC16LF84A-04 (Commercial, Industrial)									
PIC16F84A-04 (Commercial, Industrial, Extended) PIC16F84A-20 (Commercial, Industrial, Extended)				Standard Operating Conditions (unless otherwise stated)Operating temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial) $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)					
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions		
	Vdd	Supply Voltage							
D001		16LF84A	2.0	—	5.5	V	XT, RC, and LP osc configuration		
D001		16F84A	4.0	—	5.5	V	XT, RC and LP osc configuration		
D001A			4.5	—	5.5	V	HS osc configuration		
D002	Vdr	RAM Data Retention Voltage (Note 1)	1.5	—	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	_	Vss		V	See section on Power-on Reset for details		
D004	Svdd	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms			
	Idd	Supply Current (Note 2)							
D010		16LF84A	—	1	4	mA	RC and XT osc configuration (Note 4) Fosc = 2.0 MHz, VDD = 5.5V		
D010		16F84A	—	1.8	4.5	mA	RC and XT osc configuration (Note 4) Fosc = 4.0 MHz, VDD = 5.5V		
D010A D013			_	3 10	10 20	mA mA	RC and XT osc configuration (Note 4) Fosc = 4.0 MHz, VDD = 5.5V (During FLASH programming) HS osc configuration (PIC16F84A-20)		
D014			—	15	45	μA	LP osc configuration Fosc = 32 kHz, VDD = 2.0V, WDT disabled		

Legend: Rows with standard voltage device data only are shaded for improved readability.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NR Not rated for operation.

- **Note 1:** This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD,
 - T0CKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - **3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - **4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula IR = VDD/2REXT (mA) with REXT in kOhm.
 - 5: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD measurement.

9.1 DC Characteristics (Continued)

PIC16LF84A-04 (Commercial, Industrial)							
PIC16F84A-04 (Commercial, Industrial, Extended) PIC16F84A-20 (Commercial, Industrial, Extended)			$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
	Ipd	Power-down Current (Note 3)				
D020		16LF84A					
D020		16F84A-20 16F84A-04					
D021A		16LF84A	_	0.4	1.0	μΑ	VDD = 2.0V, WDT disabled, industrial
D021A		16F84A-20 16F84A-04	_	1.5 1.0	3.5 3.0	μΑ μΑ	VDD = 4.5V, WDT disabled, industrial VDD = 4.0V, WDT disabled, industrial
D021B		16F84A-20 16F84A-04	_	1.5 1.0	5.5 5.0	μΑ μΑ	VDD = 4.5V, WDT disabled, extended VDD = 4.0V, WDT disabled, extended
		Module Differential Current (Note 5)					
D022	Δ IWDT	Watchdog Timer	—	.20	16	μA	VDD = 2.0V, Industrial, Commercial
				3.5	20	μΑ	VDD = $4.0V$, Commercial VDD = $4.0V$ Industrial Extended
				4.8	25	μA	$V_{DD} = 4.5V$. Commercial
				4.8	30	μA	VDD = 4.5V, Industrial, Extended

Legend: Rows with standard voltage device data only are shaded for improved readability.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NR Not rated for operation.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD,
 - TOCKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
- 4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula IR = VDD/2REXT (mA) with REXT in kOhm.
- The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD measurement.

FIGURE 9-9: TIMER0 CLOCK TIMINGS



TABLE 9-5: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions
40	Tt0H	T0CKI High Pulse	No Prescaler	0.5Tcy + 20	—		ns	
		Width	With Prescaler	50 30			ns ns	$2.0V \le VDD \le 3.0V$ $3.0V \le VDD \le 6.0V$
41	Tt0L	T0CKI Low Pulse	No Prescaler	0.5Tcy + 20	—	_	ns	
		Width	With Prescaler	50 20	_		ns ns	$\begin{array}{l} 2.0V \leq V \text{DD} \leq 3.0V \\ 3.0V \leq V \text{DD} \leq 6.0V \end{array}$
42	Tt0P	T0CKI Period		<u>Tcy + 40</u> N	—	_	ns	N = prescale value (2, 4,, 256)

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 10-5: TYPICAL IDD vs. Fosc OVER VDD (LP MODE, 25°C)







FIGURE 10-15: TYPICAL, MINIMUM AND MAXIMUM Vol vs. Iol (VDD = 5V, -40°C TO +125°C)





20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS			
Dimer	nsion Limits	MIN	NOM	MAX		
Number of Pins	Ν	20				
Pitch	Pitch e		0.65 BSC			
Overall Height	А	-	-	2.00		
Molded Package Thickness	A2	1.65	1.75	1.85		
Standoff	A1	0.05	-	-		
Overall Width	E	7.40	7.80	8.20		
Molded Package Width	E1	5.00	5.30	5.60		
Overall Length	D	6.90	7.20	7.50		
Foot Length	L	0.55	0.75	0.95		
Footprint	L1		1.25 REF			
Lead Thickness	С	0.09	-	0.25		
Foot Angle	φ	0°	4°	8°		
Lead Width	b	0.22	-	0.38		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B



For the most current package drawings, please see the Microchip Packaging Specification located at

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch E			0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X20)				0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

Note:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

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