



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf84at-04i-ss

PIC16F84A

Table of Contents

1.0	Device Overview	3
2.0	Memory Organization	5
3.0	Data EEPROM Memory	13
4.0	I/O Ports	15
5.0	Timer0 Module	19
6.0	Special Features of the CPU	21
7.0	Instruction Set Summary	35
8.0	Development Support.....	43
9.0	Electrical Characteristics	47
10.0	DC/AC Characteristic Graphs	59
11.0	Packaging Information.....	69
Appendix A: Revision History		77
Appendix B: Conversion Considerations.....		78
Appendix C: Migration from Baseline to Mid-range Devices80		
INDEX		81
The Microchip Web Site		85
Customer Change Notification Service		85
Customer Support		85
Reader Response		86
PIC16F84A Product Identification System		87

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@microchip.com or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com to receive the most current information on all of our products.

PIC16F84A

2.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 2-2 shows the data memory map organization.

Instructions MOVWF and MOVF can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 2.5). Indirect addressing uses the present value of the RP0 bit for access into the banked areas of data memory.

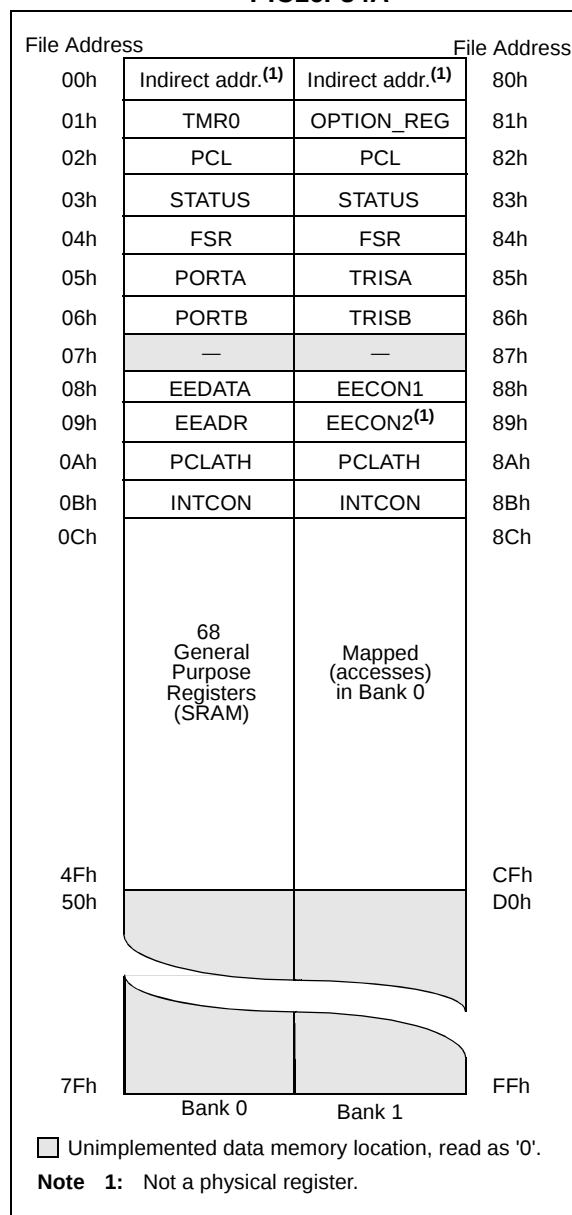
Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers, implemented as static RAM.

2.2.1 GENERAL PURPOSE REGISTER FILE

Each General Purpose Register (GPR) is 8-bits wide and is accessed either directly or indirectly through the FSR (Section 2.5).

The GPR addresses in Bank 1 are mapped to addresses in Bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

FIGURE 2-2: REGISTER FILE MAP - PIC16F84A



PIC16F84A

3.1 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available, in the very next cycle, in the EEDATA register; therefore, it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 3-1: DATA EEPROM READ

```
BCF    STATUS, RP0    ; Bank 0
MOVLW  CONFIG_ADDR    ;
MOVWF  EEADR           ; Address to read
BSF    STATUS, RP0    ; Bank 1
BSF    EECON1, RD      ; EE Read
BCF    STATUS, RP0    ; Bank 0
MOVF   EEDATA, W       ; W = EEDATA
```

3.2 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte.

EXAMPLE 3-2: DATA EEPROM WRITE

```
BSF    STATUS, RP0    ; Bank 1
BCF    INTCON, GIE     ; Disable INTs.
BSF    EECON1, WREN     ; Enable Write
MOVLW  55h             ;
;
; Required Sequence
MOVWF  EECON2           ; Write 55h
MOVLW  AAh             ;
MOVWF  EECON2           ; Write AAh
BSF    EECON1, WR       ; Set WR bit
;                          ; begin write
BSF    INTCON, GIE     ; Enable INTs.
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

3.3 Write Verify

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (Example 3-3) to the desired value to be written. This should be used in applications where an EEPROM bit will be stressed near the specification limit.

Generally, the EEPROM write failure will be a bit which was written as a '0', but reads back as a '1' (due to leakage off the bit).

EXAMPLE 3-3: WRITE VERIFY

```
BCF    STATUS, RP0    ; Bank 0
:                          ; Any code
:                          ; can go here
MOVF   EEDATA, W       ; Must be in Bank 0
BSF    STATUS, RP0    ; Bank 1
READ
BSF    EECON1, RD      ; YES, Read the
;                          ; value written
BCF    STATUS, RP0    ; Bank 0
;
; Is the value written
; (in W reg) and
; read (in EEDATA)
; the same?
;
SUBWF  EEDATA, W       ;
BTFS   STATUS, Z       ; Is difference 0?
GOTO   WRITE_ERR      ; NO, Write error
```

TABLE 3-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other RESETS
08h	EEDATA	EEPROM Data Register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM Address Register								xxxx xxxx	uuuu uuuu
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM Control Register 2								---- ----	---- ----

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends upon condition.

Shaded cells are not used by data EEPROM.

5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt-on-overflow from FFh to 00h

Figure 5-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PIC® Mid-Range Reference Manual (DS33023).

5.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment, either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PIC® Mid-Range Reference Manual, (DS33023).

5.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 5-2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 5-1: TIMER0 BLOCK DIAGRAM

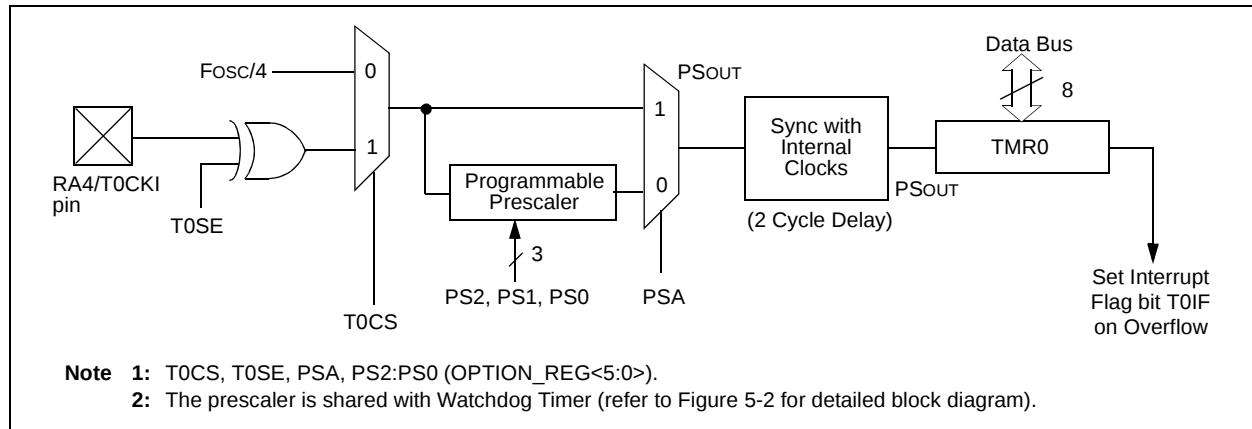


TABLE 6-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

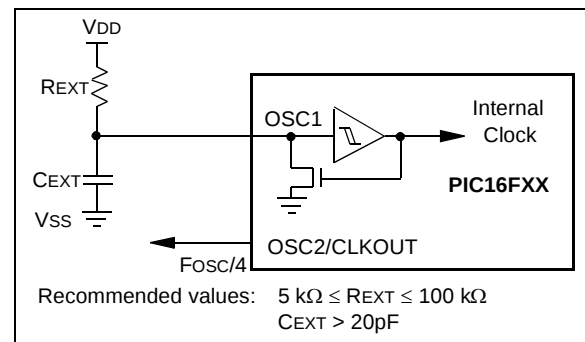
Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz	68 - 100 pF	68 - 100 pF
	200 kHz	15 - 33 pF	15 - 33 pF
XT	100 kHz	100 - 150 pF	100 - 150 pF
	2 MHz	15 - 33 pF	15 - 33 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS	4 MHz	15 - 33 pF	15 - 33 pF
	20 MHz	15 - 33 pF	15 - 33 pF

Note: Higher capacitance increases the stability of the oscillator, but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode, as well as XT mode, to avoid over-driving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components. For $V_{DD} > 4.5V$, $C1 = C2 \approx 30 \text{ pF}$ is recommended.

6.2.3 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) values, capacitor (C_{EXT}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low C_{EXT} values. The user needs to take into account variation, due to tolerance of the external R and C components. Figure 6-3 shows how an R/C combination is connected to the PIC16F84A.

FIGURE 6-3: RC OSCILLATOR MODE



6.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when V_{DD} rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin directly (or through a resistor) to V_{DD} . This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for V_{DD} must be met for this to operate properly. See Electrical Specifications for details.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting."

The POR circuit does not produce an internal RESET when V_{DD} declines.

6.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 ms nominal time-out ($TPWRT$) from POR (Figures 6-6 through 6-9). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level (possible exception shown in Figure 6-9).

A configuration bit, $\overline{\text{PWRTSE}}$, can enable/disable the PWRT. See Register 6-1 for the operation of the $\overline{\text{PWRTSE}}$ bit for a particular device.

The power-up time delay $TPWRT$ will vary from chip to chip due to V_{DD} , temperature, and process variation. See DC parameters for details.

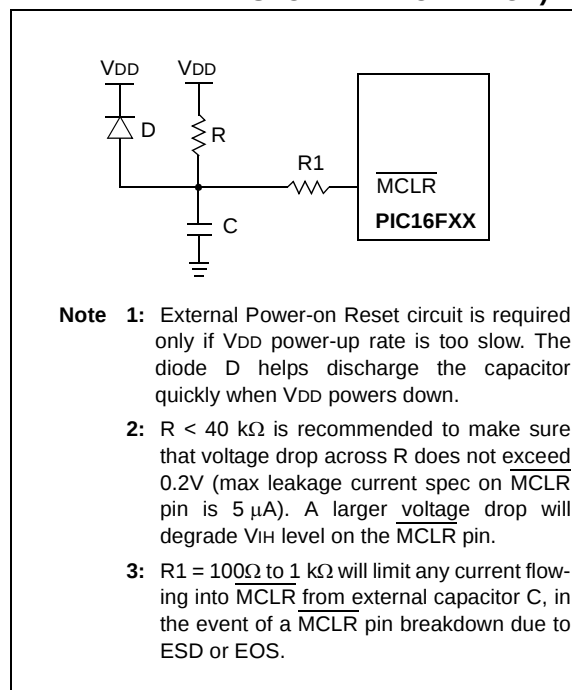
6.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends (Figure 6-6, Figure 6-7, Figure 6-8 and Figure 6-9). This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out (T_{OST}) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

When V_{DD} rises very slowly, it is possible that the $TPWRT$ time-out and T_{OST} time-out will expire before V_{DD} has reached its final value. In this case (Figure 6-9), an external Power-on Reset circuit may be necessary (Figure 6-5).

FIGURE 6-5: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V_{DD} POWER-UP)



6.8 Interrupts

The PIC16F84A has 4 sources of interrupt:

- External interrupt RB0/INT pin
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB7:RB4)
- Data EEPROM write complete interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also contains the individual and global interrupt enable bits.

The global interrupt enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. Bit GIE is cleared on RESET.

The “return from interrupt” instruction, RETFIE, exits interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. For external interrupt events, such as the RB0/INT pin or PORTB change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for both one and two cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

6.8.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION_REG<6>) is set, or falling if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing control bit INTE (INTCON<4>). Flag bit INTF must be cleared in software via the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP (Section 6.11) only if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether the processor branches to the interrupt vector following wake-up.

6.8.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in TMR0 will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>) (Section 5.0).

6.8.3 PORTB INTERRUPT

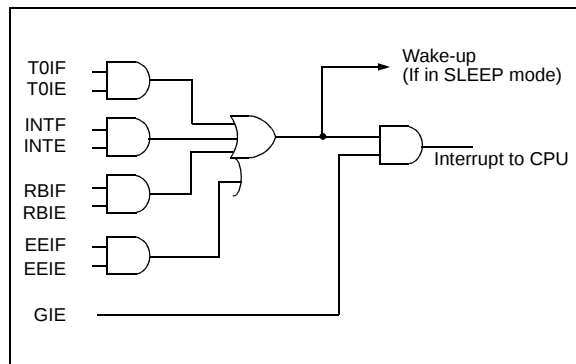
An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<3>) (Section 4.2).

Note: For a change on the I/O pin to be recognized, the pulse width must be at least T_{CY} wide.

6.8.4 DATA EEPROM INTERRUPT

At the completion of a data EEPROM write cycle, flag bit EEIF (EECON1<4>) will be set. The interrupt can be enabled/disabled by setting/clearing enable bit EEIE (INTCON<6>) (Section 3.0).

FIGURE 6-10: INTERRUPT LOGIC



PIC16F84A

6.9 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users wish to save key register values during an interrupt (e.g., W register and STATUS register). This is implemented in software.

The code in Example 6-1 stores and restores the STATUS and W register's values. The user defined registers, W_TEMP and STATUS_TEMP are the temporary storage locations for the W and STATUS registers values.

Example 6-1 does the following:

- a) Stores the W register.
- b) Stores the STATUS register in STATUS_TEMP.
- c) Executes the Interrupt Service Routine code.
- d) Restores the STATUS (and bank select bit) register.
- e) Restores the W register.

EXAMPLE 6-1: SAVING STATUS AND W REGISTERS IN RAM

PUSH	MOVWF	W_TEMP		; Copy W to TEMP register,
	SWAPF	STATUS,	W	; Swap status to be saved into W
	MOVWF	STATUS_TEMP		; Save status to STATUS_TEMP register
ISR	:	:		
	:	:		; Interrupt Service Routine
	:	:		; should configure Bank as required
	:	:		
POP	SWAPF	STATUS_TEMP,W		; Swap nibbles in STATUS_TEMP register
				; and place result into W
	MOVWF	STATUS		; Move W into STATUS register
				; (sets bank to original state)
	SWAPF	W_TEMP,	F	; Swap nibbles in W_TEMP and place result in W_TEMP
	SWAPF	W_TEMP,	W	; Swap nibbles in W_TEMP and place result into W

6.10 Watchdog Timer (WDT)

The Watchdog Timer is a free running On-Chip RC Oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT wake-up causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming configuration bit WDTE as a '0' (Section 6.1).

6.10.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION_REG register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a WDT time-out.

6.10.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (V_{DD} = Min., Temperature = Max., Max. WDT Prescaler), it may take several seconds before a WDT time-out occurs.

FIGURE 6-11: WATCHDOG TIMER BLOCK DIAGRAM

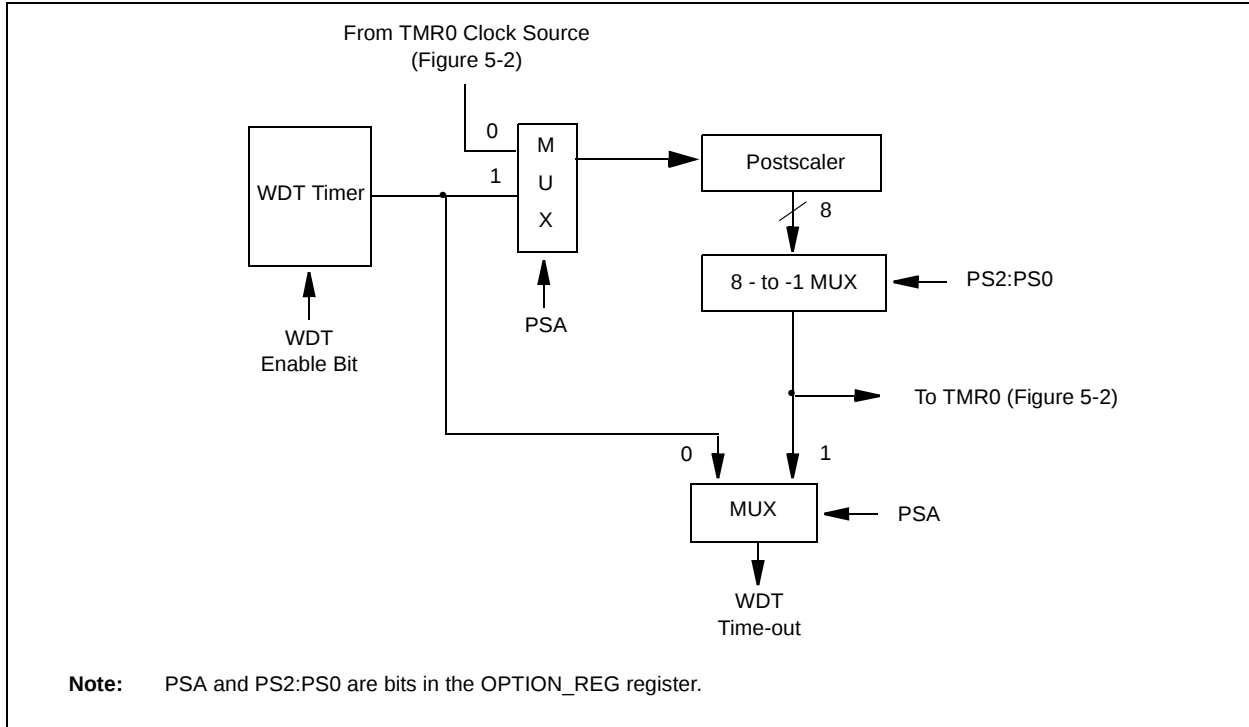


TABLE 6-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other RESETS
2007h	Config. bits	(2)	(2)	(2)	(2)	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0	(2)	
81h	OPTION_REG	RBPV	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown. Shaded cells are not used by the WDT.

Note 1: See Register 6-1 for operation of the PWRTE bit.

Note 2: See Register 6-1 and Section 6.12 for operation of the code and data protection bits.

PIC16F84A

BTFSC Bit Test, Skip if Clear

Syntax: `[label] BTFSC f,b`

Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$

Operation: skip if $(f < b) = 0$

Status Affected: None

Description: If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded, and a `NOP` is executed instead, making this a 2Tcy instruction.

CLRWDTClear Watchdog Timer

Syntax: `[label] CLRWDT`

Operands: None

Operation: 00h $\rightarrow$ WDT
0 $\rightarrow$ WDT prescaler,
1 $\rightarrow$ $\overline{TO}$
1 $\rightarrow$ $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

CALL Call Subroutine

Syntax: `[label] CALL k`

Operands: $0 \leq k \leq 2047$

Operation: (PC)+1 $\rightarrow$ TOS,
k $\rightarrow$ PC<10:0>,
(PCLATH<4:3>) $\rightarrow$ PC<12:11>

Status Affected: None

Description: Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

COMF Complement f

Syntax: `[label] COMF f,d`

Operands: $0 \leq f \leq 127$
d $\in [0,1]$

Operation: $\bar{f} \rightarrow$ (destination)

Status Affected: Z

Description: The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

CLRF Clear f

Syntax: `[label] CLRF f`

Operands: $0 \leq f \leq 127$

Operation: 00h $\rightarrow$ (f)
1 $\rightarrow$ Z

Status Affected: Z

Description: The contents of register 'f' are cleared and the Z bit is set.

DECF Decrement f

Syntax: `[label] DECF f,d`

Operands: $0 \leq f \leq 127$
d $\in [0,1]$

Operation: (f) - 1 $\rightarrow$ (destination)

Status Affected: Z

Description: Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

CLRWClear W

Syntax: `[label] CLRW`

Operands: None

Operation: 00h $\rightarrow$ (W)
1 $\rightarrow$ Z

Status Affected: Z

Description: W register is cleared. Zero bit (Z) is set.

PIC16F84A

XORLW	Exclusive OR Literal with W
Syntax:	<i>[label]</i> XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .XOR. k $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	<i>[label]</i> XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

PIC16F84A

FIGURE 9-1: PIC16F84A-20 VOLTAGE-FREQUENCY GRAPH

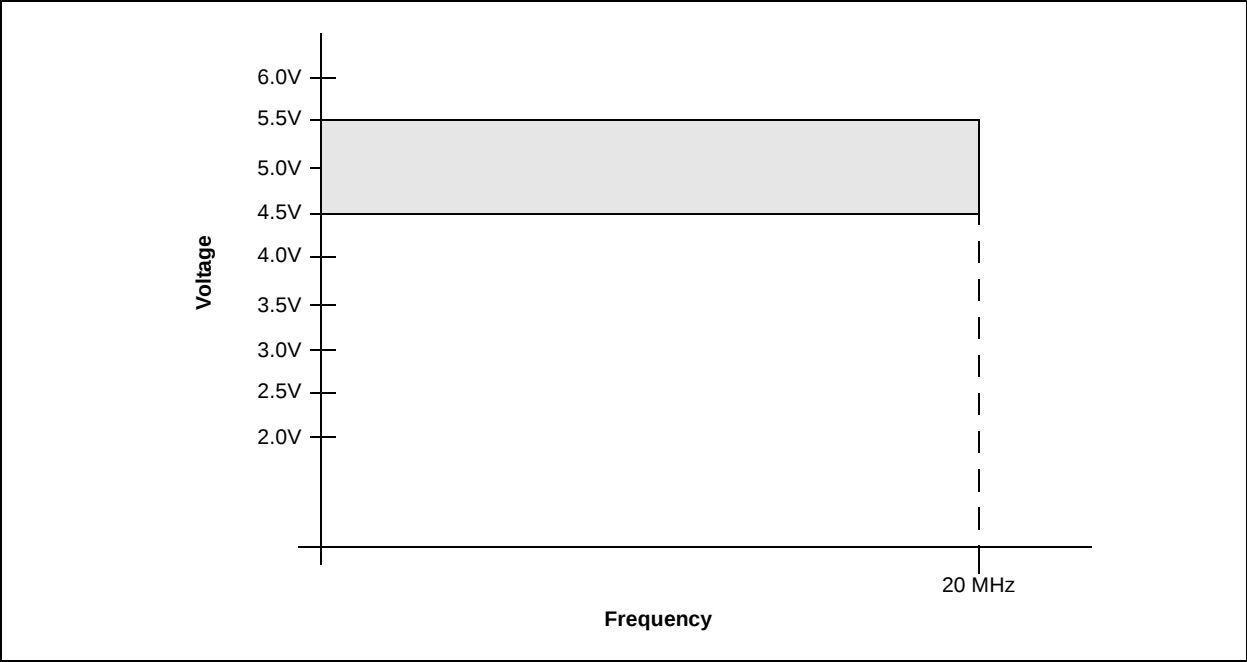


FIGURE 9-2: PIC16LF84A-04 VOLTAGE-FREQUENCY GRAPH

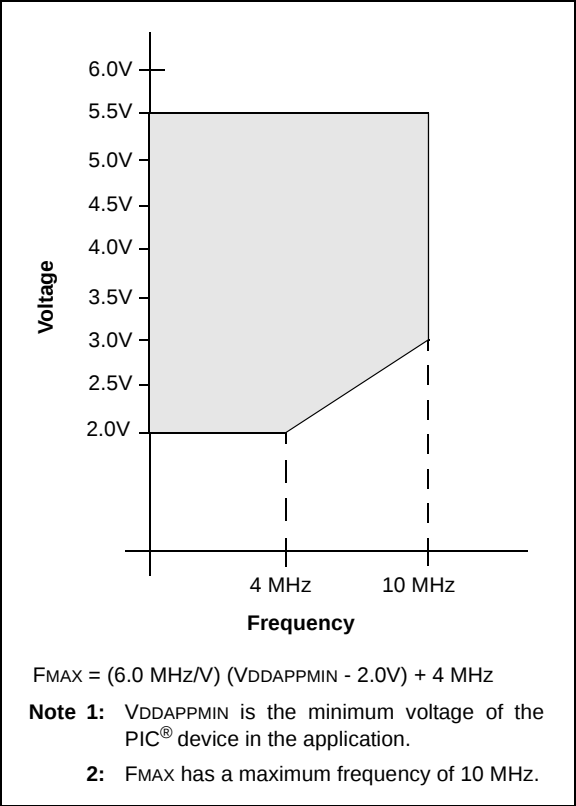
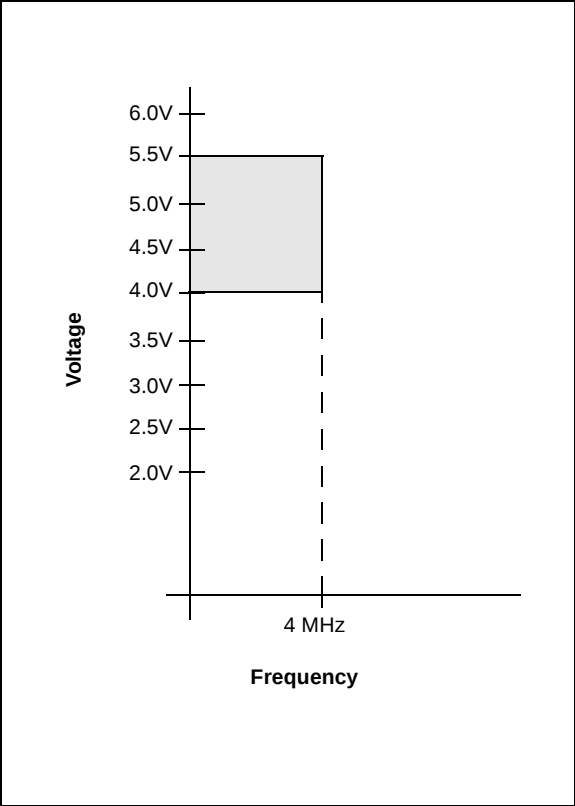


FIGURE 9-3: PIC16F84A-04 VOLTAGE-FREQUENCY GRAPH



PIC16F84A

9.1 DC Characteristics (Continued)

PIC16LF84A-04 (Commercial, Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
PIC16F84A-04 (Commercial, Industrial, Extended) PIC16F84A-20 (Commercial, Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D020	IPD	Power-down Current (Note 3)					
		16LF84A					
D020		16F84A-20 16F84A-04					
D021A		16LF84A	—	0.4	1.0	μA	V _{DD} = 2.0V, WDT disabled, industrial
D021A		16F84A-20	—	1.5	3.5	μA	V _{DD} = 4.5V, WDT disabled, industrial
		16F84A-04	—	1.0	3.0	μA	V _{DD} = 4.0V, WDT disabled, industrial
D021B		16F84A-20	—	1.5	5.5	μA	V _{DD} = 4.5V, WDT disabled, extended
		16F84A-04	—	1.0	5.0	μA	V _{DD} = 4.0V, WDT disabled, extended
D022	ΔI _{WDT}	Module Differential Current (Note 5) Watchdog Timer	—	.20	16	μA	V _{DD} = 2.0V, Industrial, Commercial
			—	3.5	20	μA	V _{DD} = 4.0V, Commercial
			—	3.5	28	μA	V _{DD} = 4.0V, Industrial, Extended
			—	4.8	25	μA	V _{DD} = 4.5V, Commercial
			—	4.8	30	μA	V _{DD} = 4.5V, Industrial, Extended

Legend: Rows with standard voltage device data only are shaded for improved readability.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NR Not rated for operation.

Note 1: This is the limit to which V_{DD} can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all I_{DD} measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD},

T0CKI = V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

4: For RC osc configuration, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I_{DD} measurement.

PIC16F84A

FIGURE 9-7: CLKOUT AND I/O TIMING

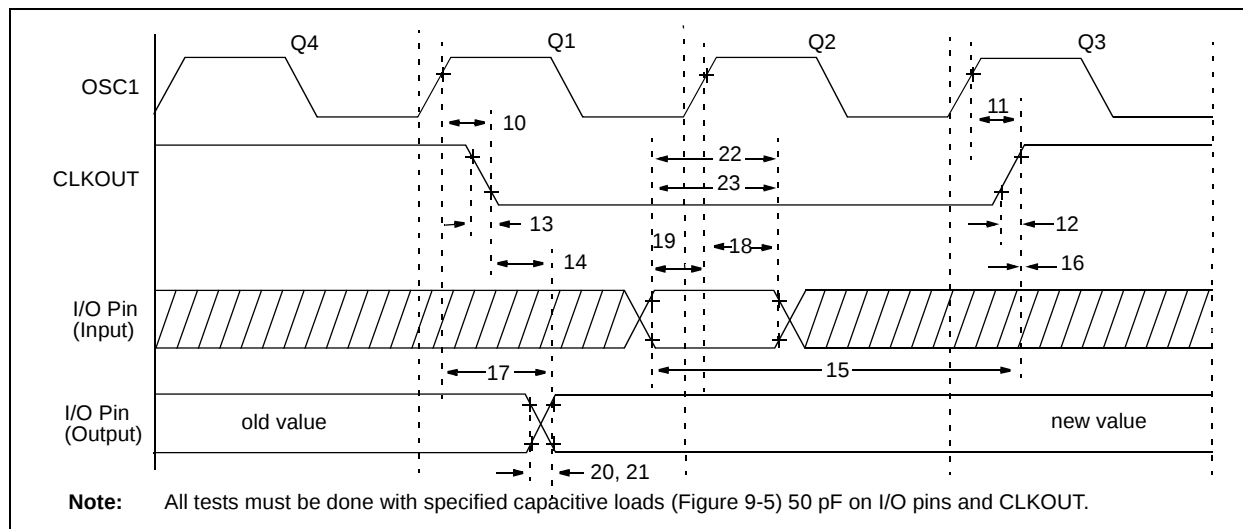


TABLE 9-3: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	—	15	30	ns	(Note 1)
10A		Extended (LF)	—	15	120	ns	(Note 1)
11	TosH2ckH	OSC1↑ to CLKOUT↑	—	15	30	ns	(Note 1)
11A		Extended (LF)	—	15	120	ns	(Note 1)
12	TckR	CLKOUT rise time	—	15	30	ns	(Note 1)
12A		Extended (LF)	—	15	100	ns	(Note 1)
13	TckF	CLKOUT fall time	—	15	30	ns	(Note 1)
13A		Extended (LF)	—	15	100	ns	(Note 1)
14	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5Tcy + 20	ns	(Note 1)
15	TioV2ckH	Port in valid before CLKOUT ↑	Standard Extended (LF)	0.30Tcy + 30 0.30Tcy + 80	— —	ns ns	(Note 1) (Note 1)
16	TckH2ioI	Port in hold after CLKOUT ↑	0	—	—	ns	(Note 1)
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	Standard Extended (LF)	— —	125 250	ns ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	Standard Extended (LF)	10 10	— —	ns ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	Standard Extended (LF)	-75 -175	— —	ns ns	
20	TioR	Port output rise time	Standard Extended (LF)	— 10	35 70	ns ns	
21	TioF	Port output fall time	Standard Extended (LF)	— 10	35 70	ns ns	
22	TINP	INT pin high or low time	Standard Extended (LF)	20 55	— —	ns ns	
23	TRBP	RB7:RB4 change INT high or low time	Standard Extended (LF)	Tosc§ Tosc§	— —	ns ns	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ By design.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.

PIC16F84A

FIGURE 10-9: AVERAGE Fosc vs. VDD FOR R (RC MODE, C = 300 pF, 25°C)

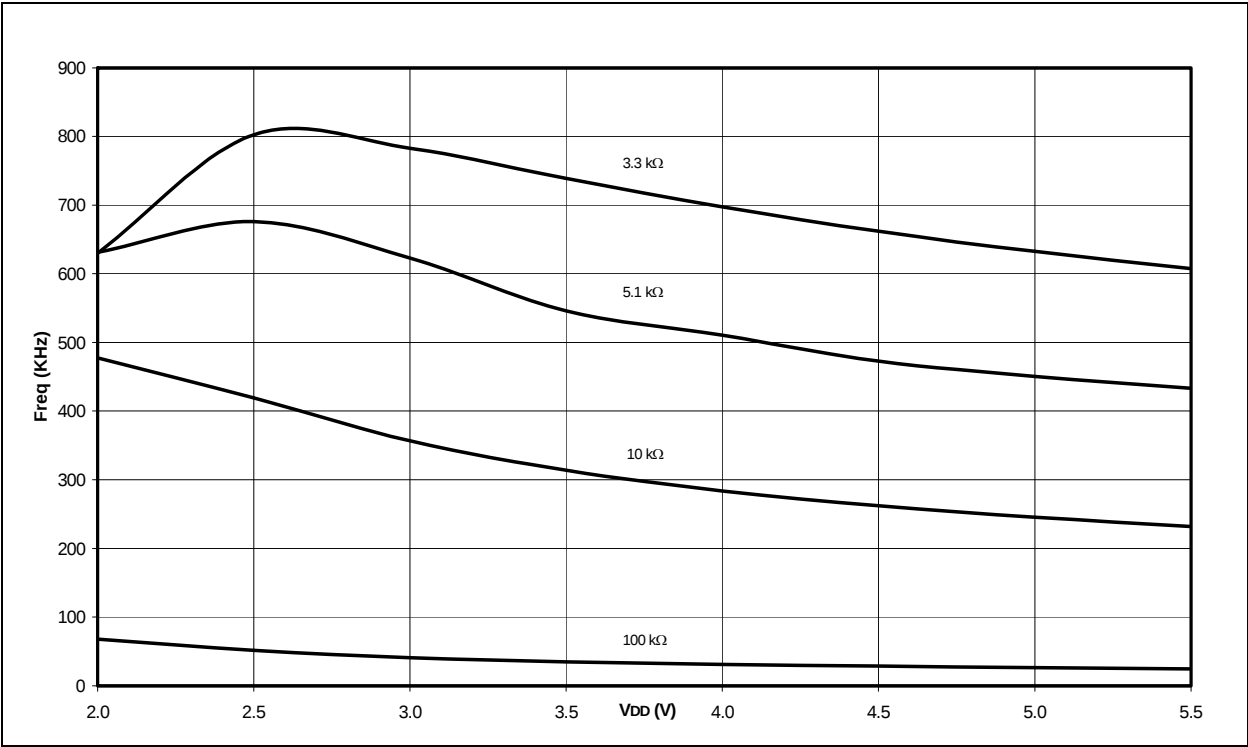
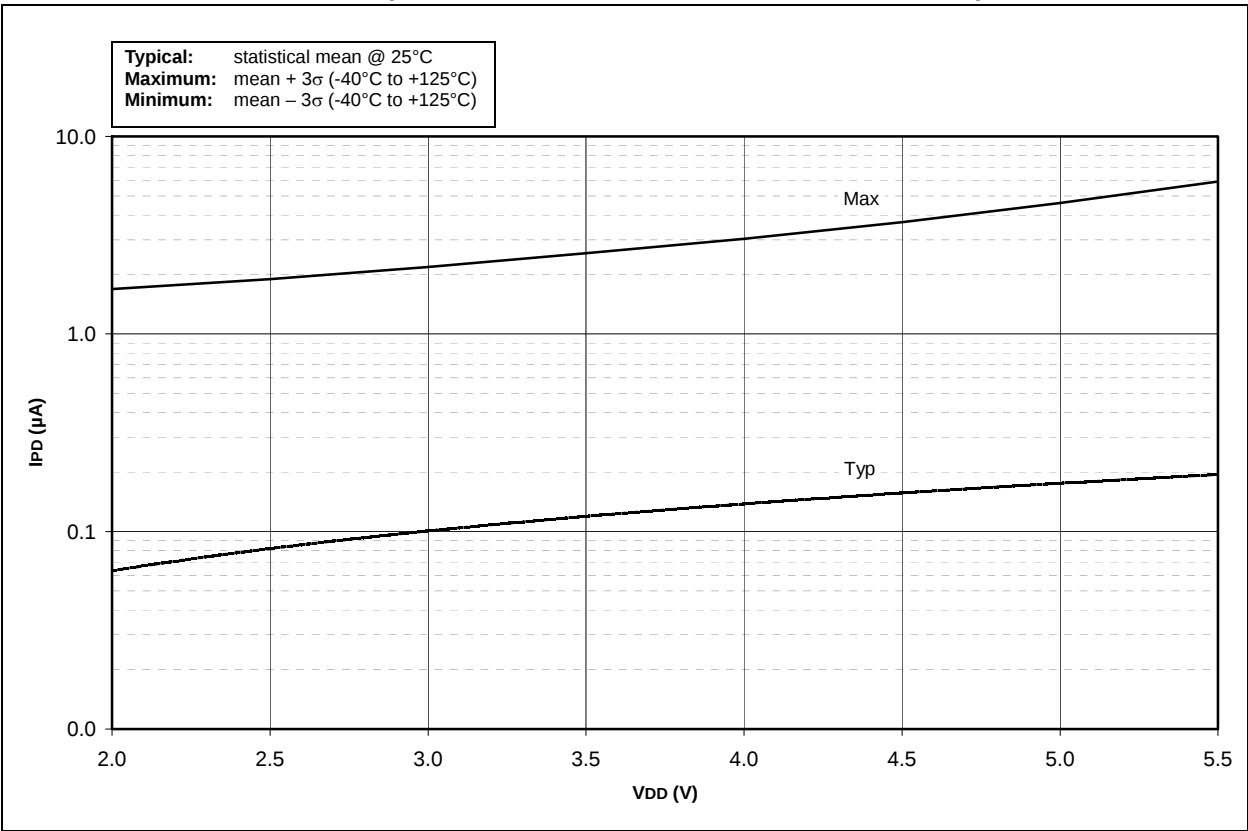


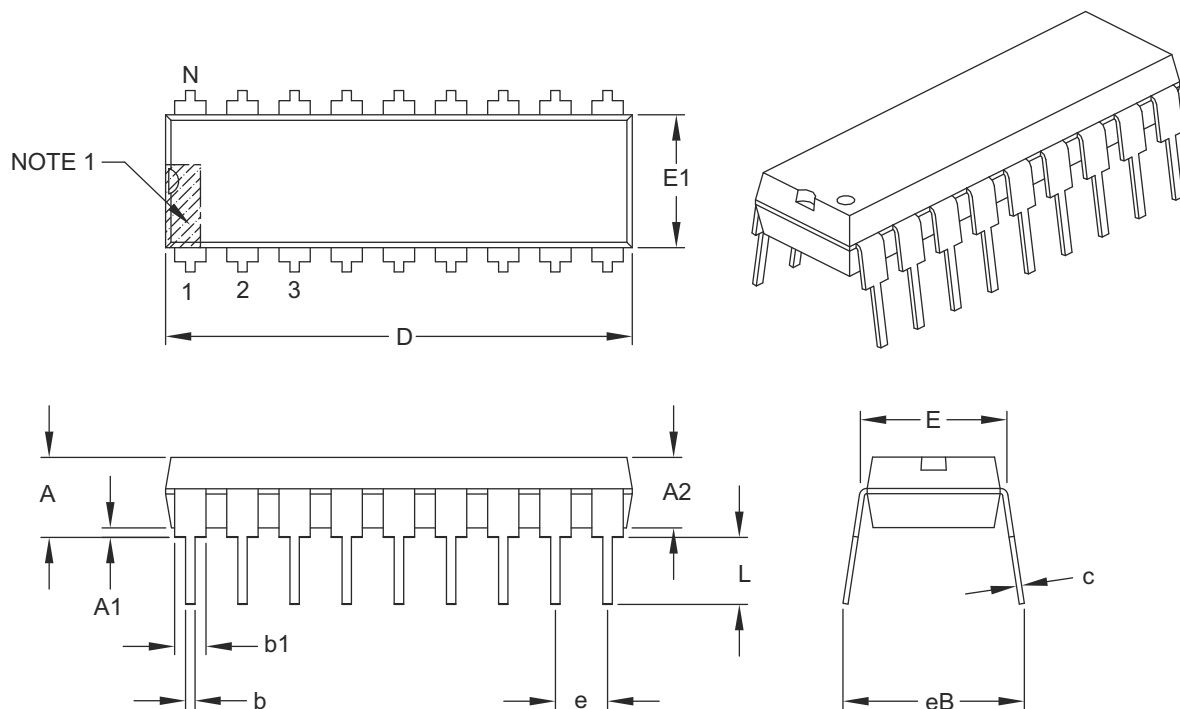
FIGURE 10-10: IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)



PIC16F84A

18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	INCHES		
		Dimension Limits	MIN	NOM	MAX
Number of Pins	N		18		
Pitch	e		.100 BSC		
Top to Seating Plane	A		–	–	.210
Molded Package Thickness	A2		.115	.130	.195
Base to Seating Plane	A1		.015	–	–
Shoulder to Shoulder Width	E		.300	.310	.325
Molded Package Width	E1		.240	.250	.280
Overall Length	D		.880	.900	.920
Tip to Seating Plane	L		.115	.130	.150
Lead Thickness	c		.008	.010	.014
Upper Lead Width	b1		.045	.060	.070
Lower Lead Width	b		.014	.018	.022
Overall Row Spacing §	eB		–	–	.430

Notes:

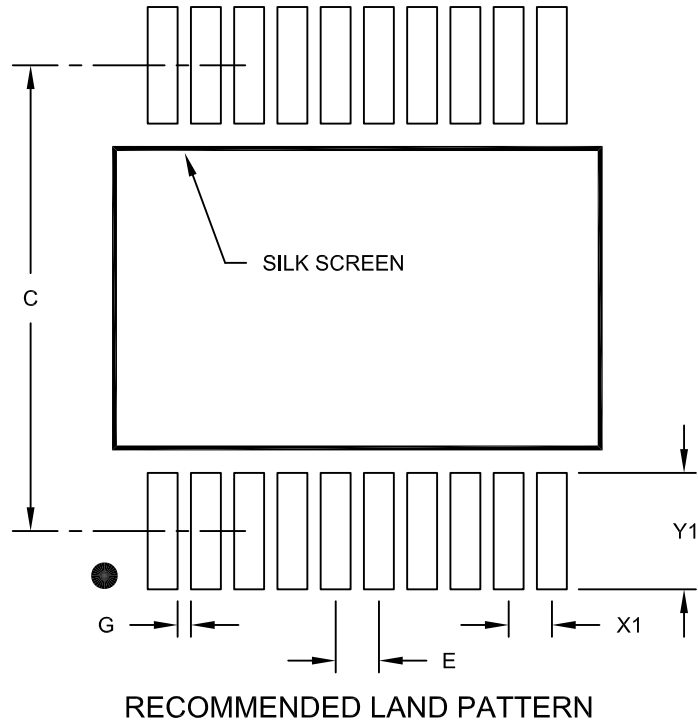
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

INDEX

A

Absolute Maximum Ratings	47
AC (Timing) Characteristics	53
Architecture, Block Diagram	3
Assembler	
MPASM Assembler	44

B

Banking, Data Memory	6
Block Diagrams	
Crystal/Ceramic Resonator Operation	22
External Clock Input Operation	22
External Power-on Reset Circuit	26
Interrupt Logic	29
On-chip Reset	24
PIC16F84A	3
PORTA	
RA3:RA0 Pins	15
RA4 Pins	15
PORTB	
RB3:RB0 Pins	17
RB7:RB4 Pins	17
RC Oscillator Mode	23
Timer0	19
Timer0/WDT Prescaler	20
Watchdog Timer (WDT)	31

C

C (Carry) bit	8
C Compilers	
MPLAB C18	44
CLKIN Pin	4
CLKOUT Pin	4
Code Examples	
Clearing RAM Using Indirect Addressing	11
Data EEPROM Write Verify	14
Indirect Addressing	11
Initializing PORTA	15
Initializing PORTB	17
Reading Data EEPROM	14
Saving STATUS and W Registers in RAM	30
Writing to Data EEPROM	14
Code Protection	21, 33
Configuration Bits	21
Configuration Word	21
Conversion Considerations	78
Customer Change Notification Service	85
Customer Notification Service	85
Customer Support	85

D

Data EEPROM Memory	13
Associated Registers	14
EEADR Register	7, 13, 25
EECON1 Register	7, 13, 25
EECON2 Register	7, 13, 25
EEDATA Register	7, 13, 25
Write Complete Enable (EEIE Bit)	29
Write Complete Flag (EEIF Bit)	29
Data EEPROM Write Complete	29
Data Memory	6
Bank Select (RP0 Bit)	6
Banking	6
DC bit	8

DC Characteristics	49, 51
Development Support	43
Device Overview	3

E

EECON1 Register	
EEIF Bit	29
Electrical Characteristics	47
Load Conditions	54
Parameter Measurement Information	54
PIC16F84A-04 Voltage-Frequency Graph	48
PIC16F84A-20 Voltage-Frequency Graph	48
PIC16LF84A-04 Voltage-Frequency Graph	48
Temperature and Voltage Specifications - AC	54
Endurance	1
Errata	2
External Clock Input (RA4/T0CKI). See Timer0	
External Interrupt Input (RB0/INT). See Interrupt Sources	
External Power-on Reset Circuit	26

F

Firmware Instructions	35
-----------------------------	----

I

I/O Ports	15
ID Locations	21, 33
In-Circuit Serial Programming (ICSP)	21, 33
INDF Register	7
Indirect Addressing	11
FSR Register	6, 7, 11, 25
INDF Register	7, 11, 25
Instruction Format	35
Instruction Set	35
ADDLW	37
ADDWF	37
ANDLW	37
ANDWF	37
BCF	37
BSF	37
BTFSC	38
BTFSS	37
CALL	38
CLRf	38
CLRWF	38
CLRWDt	38
COMF	38
DECF	38
DECFSZ	39
GOTO	39
INCF	39
INCFSZ	39
IORLW	39
IORWF	39
MOVF	40
MOVLW	40
MOVWF	40
NOP	40
RETFIE	40
RETLW	40
RETURN	40
RLF	41
RRF	41
SLEEP	41
SUBLW	41

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://microchip.com/support>

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

TO: Technical Publications Manager Total Pages Sent _____

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (____) _____ - _____ FAX: (____) _____ - _____

Application (optional):

Would you like a reply? ____Y ____N

Device:

Literature Number: DS35007C

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?
