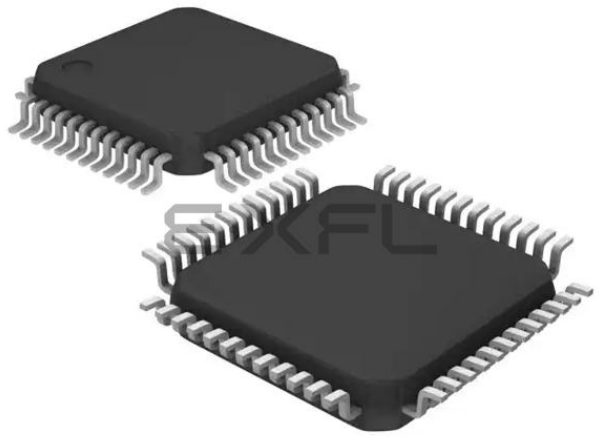

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc230lc2ae

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2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC230 Features – Automotive Line

- ARM® Cortex™-M0 core
  - Runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K/128K bytes Flash for program code
  - 8 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for 128 KB system, fixed 4 KB Data Flash for the 32 KB and 64 KB system
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 8K/16K bytes embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ±3 % at -40 ℃ ~ +105 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 72 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- Watchdog Timer
  - Multiple clock sources

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

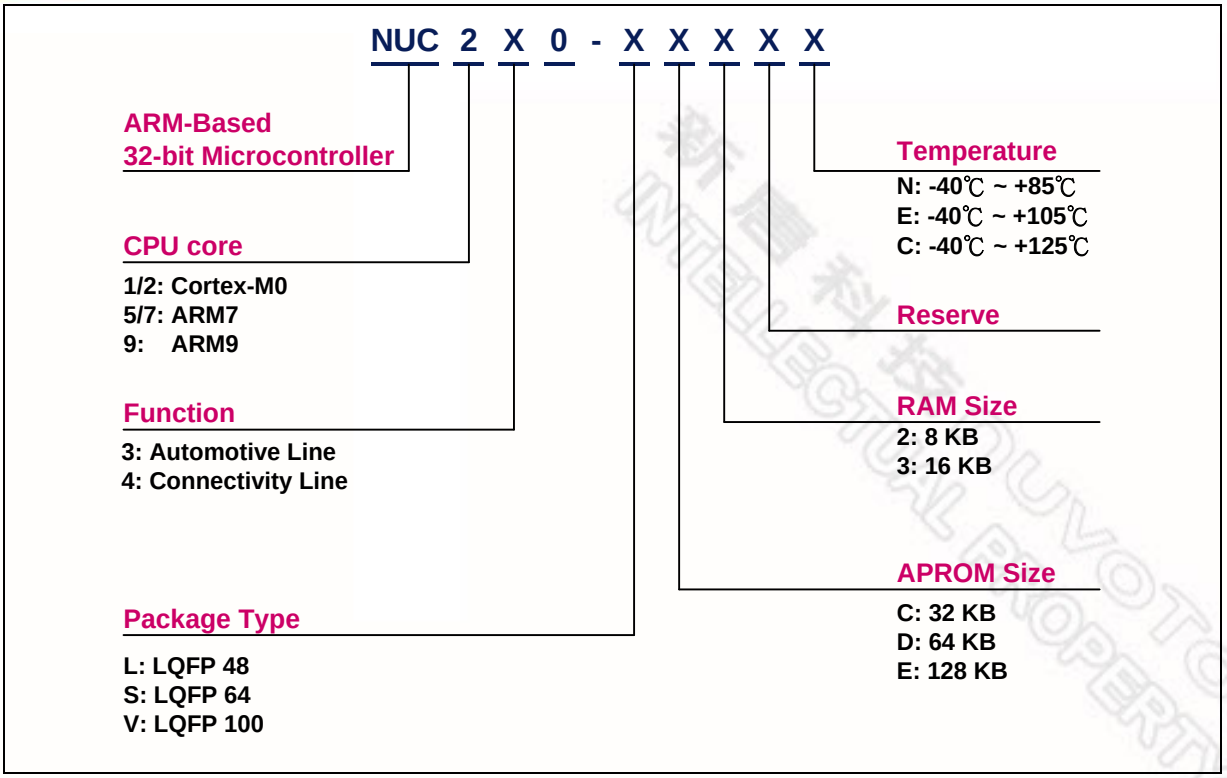


Figure 4-1 NuMicro™ NUC230/240 Series Selection Code

4.2.1.3 NuMicro™ NUC230LxxAE LQFP 48 pin

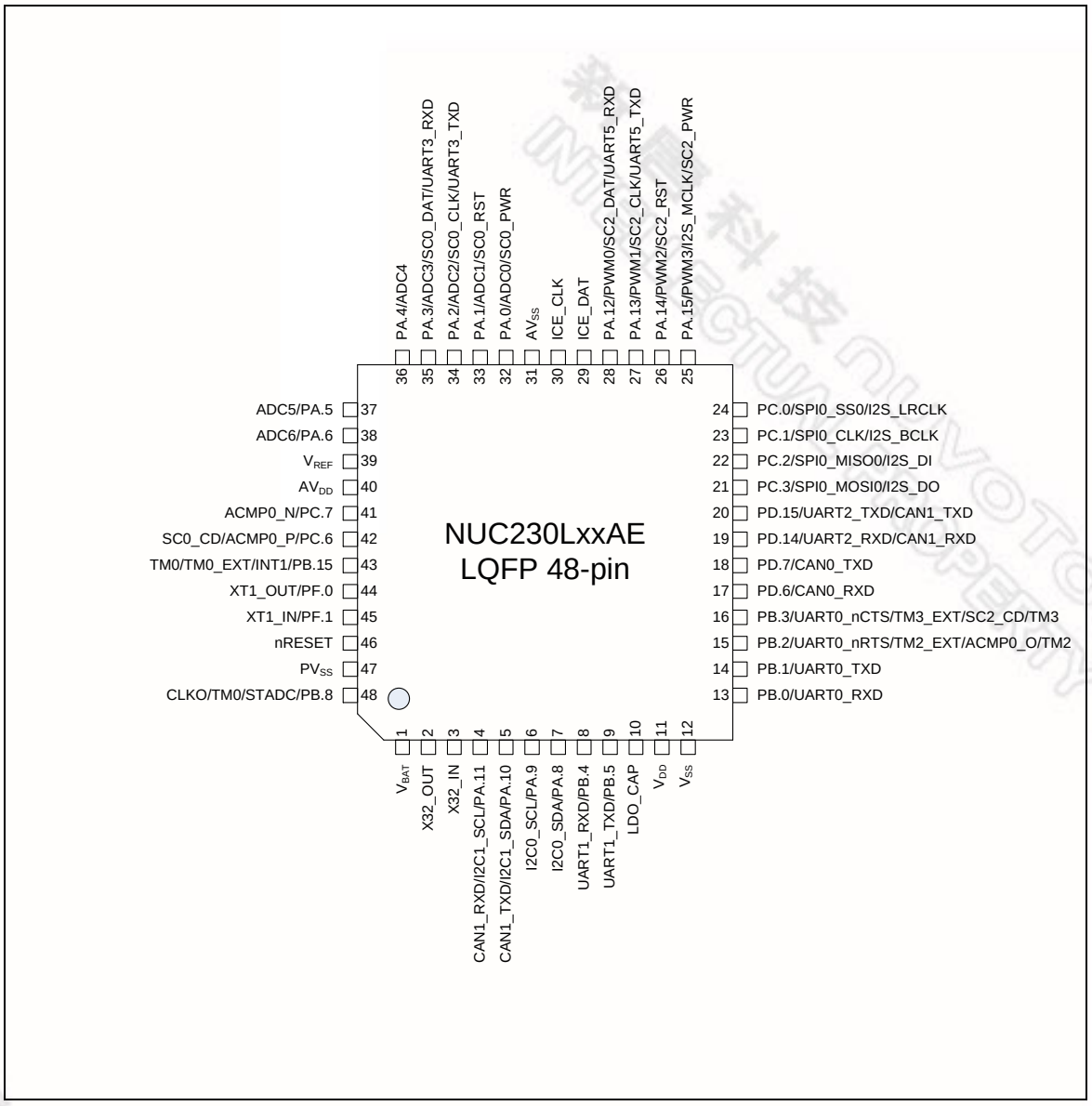


Figure 4-4 NuMicro™ NUC230LxxAE LQFP 48-pin Diagram

4.2.2.3 NuMicro™ NUC240LxxAE LQFP 48 pin

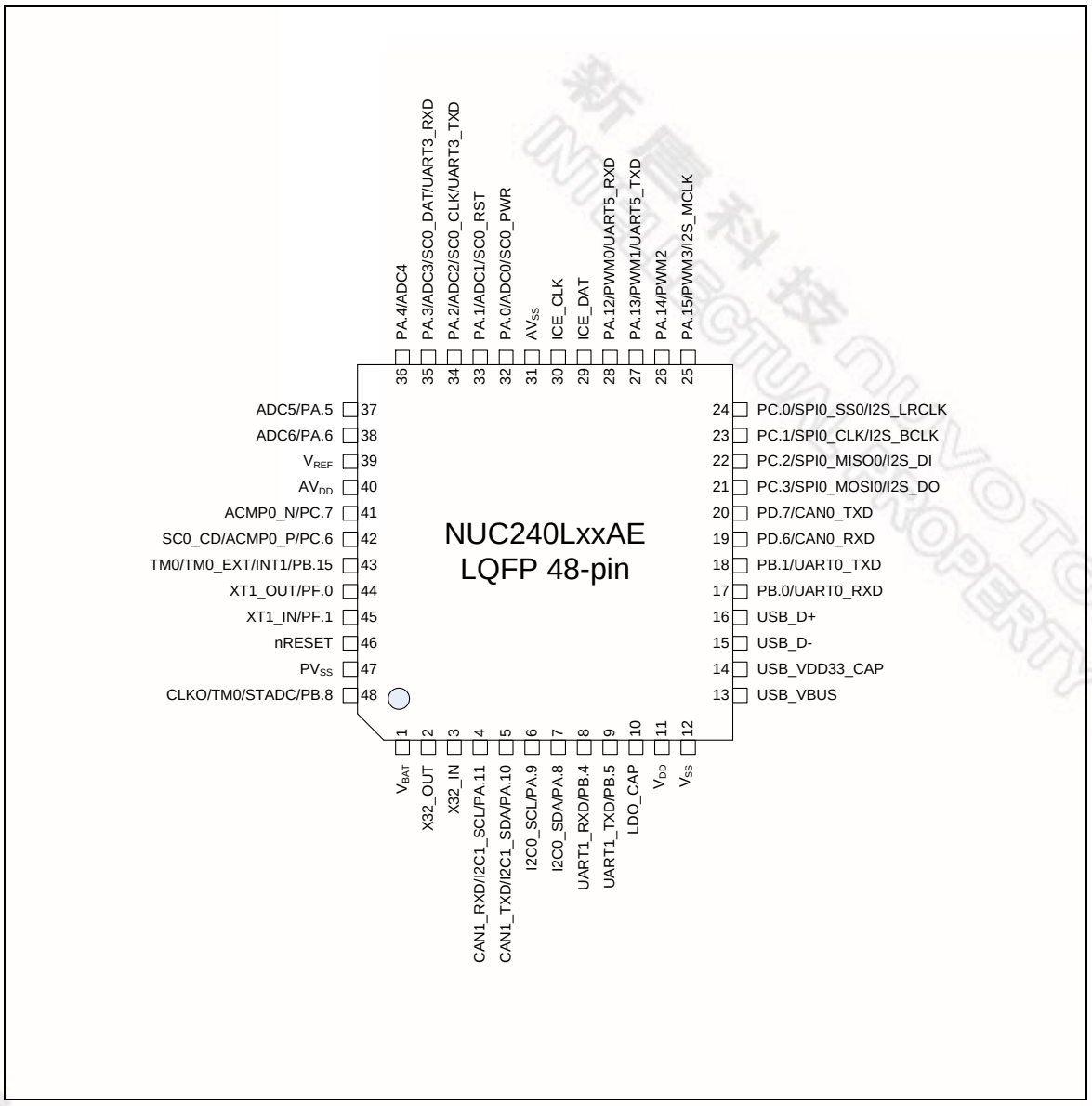


Figure 4-7 NuMicro™ NUC240LxxAE LQFP 48-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			TM2_EXT	I	Timer2 external capture input pin.
			TM2	O	Timer2 toggle output pin.
			ACMP0_O	O	Comparator0 output pin.
35	24		PB.3	I/O	General purpose digital I/O pin.
			UART0_nCTS	I	Clear to Send input pin for UART0.
			nWRH	O	EBI high byte write enable output pin
			TM3_EXT	I	Timer3 external capture input pin.
			TM3	O	Timer3 toggle output pin.
			SC2_CD	I	SmartCard2 card detect pin.
36	25	19	PD.6	I/O	General purpose digital I/O pin.
			CAN0_RXD	I	Data receiver input pin for CAN0.
37	26	20	PD.7	I/O	General purpose digital I/O pin.
			CAN0_TXD	O	Data transmitter output pin for CAN0.
38	27		PD.14	I/O	General purpose digital I/O pin.
			UART2_RXD	I	Data receiver input pin for UART2.
			CAN1_RXD	I	Data receiver input pin for CAN1.
39	28		PD.15	I/O	General purpose digital I/O pin.
			UART2_TXD	O	Data transmitter output pin for UART2.
			CAN1_TXD	O	Data transmitter output pin for CAN1.
40			PC.5	I/O	General purpose digital I/O pin.
			SPI0_MOSI1	I/O	2nd SPI0 MOSI (Master Out, Slave In) pin.
41			PC.4	I/O	General purpose digital I/O pin.
			SPI0_MISO1	I/O	2nd SPI0 MISO (Master In, Slave Out) pin.
42	29	21	PC.3	I/O	General purpose digital I/O pin.
			SPI0_MOSI0	I/O	1st SPI0 MOSI (Master Out, Slave In) pin.
			I2S_DO	O	I^2S data output.
43	30	22	PC.2	I/O	General purpose digital I/O pin.
			SPI0_MISO0	I/O	1st SPI0 MISO (Master In, Slave Out) pin.
			I2S_DI	I	I^2S data input.
44	31	23	PC.1	I/O	General purpose digital I/O pin.
			SPI0_CLK	I/O	SPI0 serial clock pin.
			I2S_BCLK	I/O	I^2S bit clock pin.

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4018_0000 – 0x4018_3FFF	CAN0_BA	CAN0 Bus Control Registers
0x4018_4000 – 0x4018_7FFF	CAN1_BA	CAN1 Bus Control Registers
0x4019_0000 – 0x4019_3FFF	SC0_BA	SC0 Control Registers
0x4019_4000 – 0x4019_7FFF	SC1_BA	SC1 Control Registers
0x4019_8000 – 0x4019_BFFF	SC2_BA	SC2 Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I^2S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6-1 Address Space Assignments for On-Chip Controllers

6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

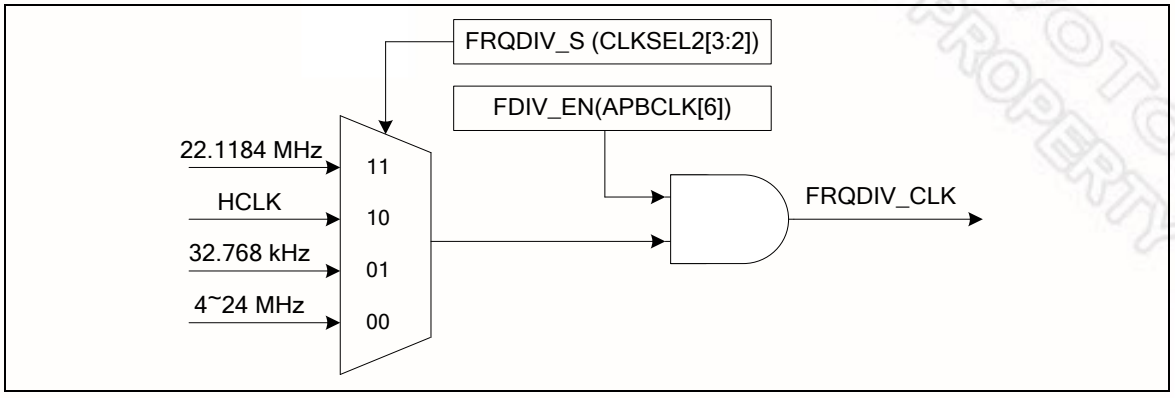


Figure 6-8 Clock Source of Frequency Divider

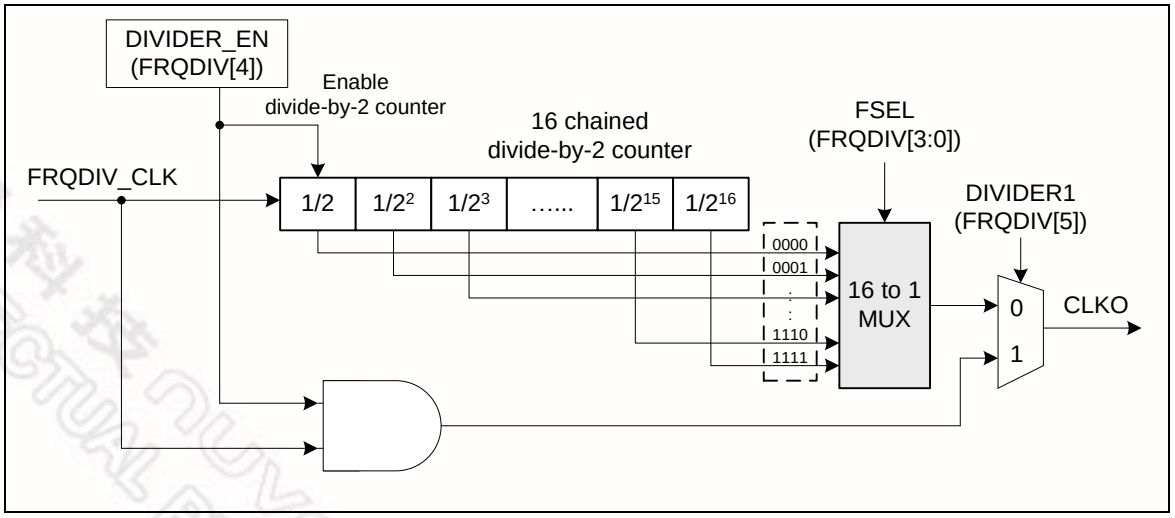


Figure 6-9 Frequency Divider Block Diagram

6.9 PWM Generator and Capture Timer (PWM)

6.9.1 Overview

The NuMicro™ NUC230/240 series has 2 sets of PWM group supporting a total of 4 sets of PWM generators that can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide eight independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DZEN01 (PCR[4]) is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively. Refer to **錯誤! 找不到參照來源。** and **錯誤! 找不到參照來源。** for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0 (CCR0[1]) (Rising latch Interrupt enable) and CFL_IE0 (CCR0[2]) (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CRL_IE1 (CCR0[17]) and CFL_IE1 (CCR0[18]). And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For

6.14 Smart Card Host Interface (SC)

6.14.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal. It also support UART mode for full duplex asynchronous communications.

6.14.2 Features

- Supports up to three ISO7816-3 ports (SC0, SC1 and SC2)
  - ISO7816-3 T=0, T=1 compliant
  - EMV2000 compliant
  - Separates receive/ transmit 4 byte entry FIFO for data payloads.
  - Programmable transmission clock frequency.
  - Programmable receiver buffer trigger level.
  - Programmable guard time selection (11 ETU ~ 267 ETU).
  - A 24-bit and two 8-bit times for Answer to Request (ATR) and waiting times processing.
  - Supports auto inverse convention function.
  - Supports transmitter and receiver error retry and error number limiting function.
  - Supports hardware activation sequence, hardware warm reset sequence and hardware deactivation sequence process.
  - Supports hardware auto deactivation sequence when detecting the card removal.
- Supports up to three UART ports (UART3, UART4, UART5)
  - Full duplex, asynchronous communications.
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character.
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads.
  - Supports programmable baud rate generator for each channel.
  - Supports programmable receiver buffer trigger level.
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SCx_EGTR [EGT] register.
  - Programmable even, odd or no parity bit generation and detection.
  - Programmable stop bit, 1 or 2 stop bit generation.

6.17.2 Features

- Up to four sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32 bits
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Two slave select lines in Master mode
- Supports the Byte Reorder function
- Supports Byte or Word Suspend mode
- Variable output bus clock frequency in Master mode
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface

6.18 I²S Controller (I²S)

6.18.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 8-word depth FIFO for reading path and writing path respectively and is capable of handling 8-, 16-, 24- and 32-bit word sizes. PDMA controller handles the data movement between FIFO and memory.

6.18.2 Features

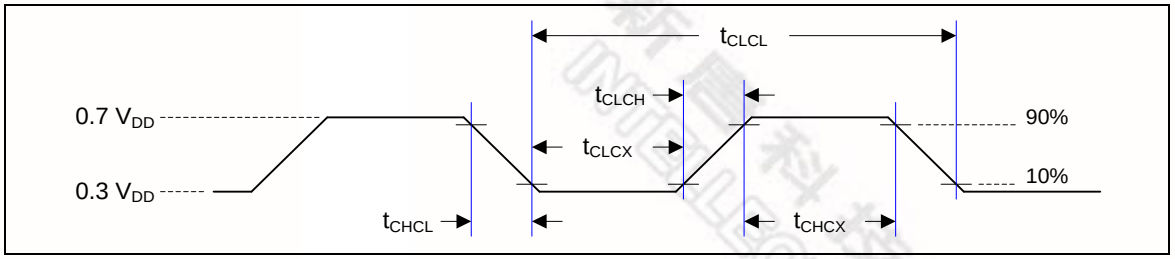
- Supports Master mode and Slave mode
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports monaural and stereo audio data
- Supports I²S and MSB justified data format
- Provides two 8-word FIFO data buffers, one for transmitting and the other for receiving
- Supports PDMA transfer

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Normal Run Mode at 32.768 kHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD17}		141		µA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital module
						5.5V	32.768	X	X	V
	I_{DD18}		129		µA	5.5V	32.768	X	X	X
	I_{DD19}		138		µA	3.3V	32.768	X	X	V
	I_{DD20}		125		µA	3.3V	32.768	X	X	X
Operating Current Normal Run Mode at 10 kHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD21}		125		µA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{DD22}		120		µA	5.5V	X	10	X	X
	I_{DD23}		125		µA	3.3V	X	10	X	V
	I_{DD24}		120		µA	3.3V	X	10	X	X
Operating Current Idle Mode at 72 MHz V_{LDO} =1.8 V	I_{IDLE1}		42		mA	V_{DD}	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{IDLE2}		11		mA	5.5V	12 MHz	X	V	X
	I_{IDLE3}		41		mA	3.3V	12 MHz	X	V	V
	I_{IDLE4}		9		mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 50 MHz V_{LDO} =1.8 V	I_{IDLE5}		28		mA	5.5V	12 MHz	X	V	V
	I_{IDLE6}		10		mA	5.5V	12 MHz	X	V	X
	I_{IDLE7}		27		mA	3.3V	12 MHz	X	V	V
	I_{IDLE8}		9		mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 12 MHz V_{LDO} =1.8 V	I_{IDLE9}		7.5		mA	5.5V	12 MHz	X	X	V
	I_{IDLE10}		2.4		mA	5.5V	12 MHz	X	X	X
	I_{IDLE11}		6.5		mA	3.3V	12 MHz	X	X	V
	I_{IDLE12}		1.5		mA	3.3V	12 MHz	X	X	X
Operating Current Idle Mode at 4 MHz V_{LDO} =1.8 V	I_{IDLE13}		3.3		mA	5.5V	4 MHz	X	X	V
	I_{IDLE14}		1.7		mA	5.5V	4 MHz	X	X	X
	I_{IDLE15}		2.4		mA	3.3V	4 MHz	X	X	V
	I_{IDLE16}		0.8		mA	3.3V	4 MHz	X	X	X
Operating Current Idle Mode at 32.768 kHz V_{LDO} =1.8 V	I_{IDLE17}		133		µA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital module
						5.5V	32.768	X	X	V
	I_{IDLE18}		120		µA	5.5V	32.768	X	X	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{IDLE19}		133		µA	3.3V	32.768	X	X	V
	I_{IDLE20}		120		µA	3.3V	32.768	X	X	X
Operating Current Idle Mode at 10 kHz	I_{IDLE21}		122		µA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{IDLE22}		118		µA	5.5V	X	10	X	X
	I_{IDLE23}		122		µA	3.3V	X	10	X	V
	I_{IDLE24}		118		µA	3.3V	X	10	X	X
Standby Current Power-down Mode (Deep Sleep Mode) V_{LDO} =1.6 V	I_{PWD1}		15		µA	V_{DD}	HXT/HIRC PLL	LXT (kHz)	RTC	RAM retension
						5.5V	X	X	X	V
	I_{PWD2}		15		µA	5.5V	X	X	X	V
	I_{PWD3}		17		µA	3.3V	X	32.768	V	V
	I_{PWD4}		17		µA	3.3V	X	32.768	V	V
RTC Operating Current	I_{VBAT}		1.6		µA	V_{BAT}= 3.0V, RTC enabled				
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-50	-60	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}				
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	µA	V_{DD} = 3.3V, V_{IN} = 0.45V				
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-2	-	+2	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}				
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	µA	V_{DD} = 5.5V, V_{IN}<2.0V				
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V				
		-0.3	-	0.6		V_{DD} = 2.5V				
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V				
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V				
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IL2}	-0.3	-	0.3V_{DD}	V					
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IH2}	0.7V_{DD}	-	V_{DD} +0.2	V					

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

8.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	105	℃
Operating Current	12 MHz at V_{DD} = 5V	-	2	-	mA
Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

8.4.8 USB PHY Specification

8.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High (driven)		2.0			V
V_{IL}	Input Low				0.8	V
V_{DI}	Differential Input Sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential Common-mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
V_{OL}	Output Low (driven)		0		0.3	V
V_{OH}	Output High (driven)		2.8		3.6	V
V_{CRS}	Output Signal Cross Voltage		1.3		2.0	V
R_{PU}	Pull-up Resistor		1.425		1.575	kΩ
V_{TRM}	Termination Voltage for Upstream Port Pull-up (RPU)		3.0		3.6	V
Z_{DRV}	Driver Output Resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver Capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

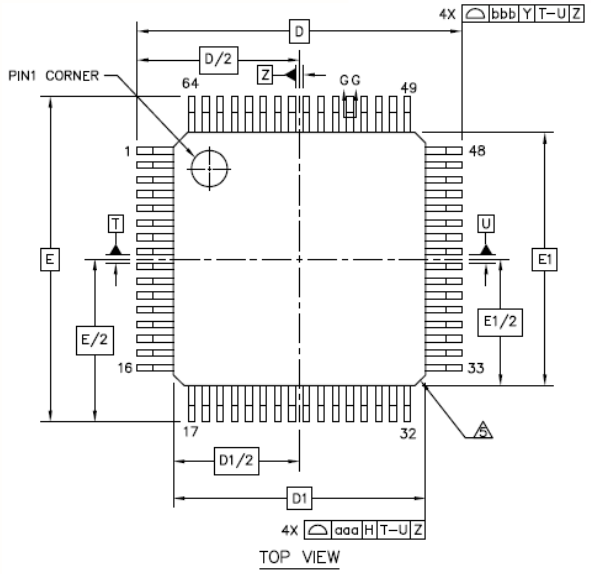
8.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and Fall Time Matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

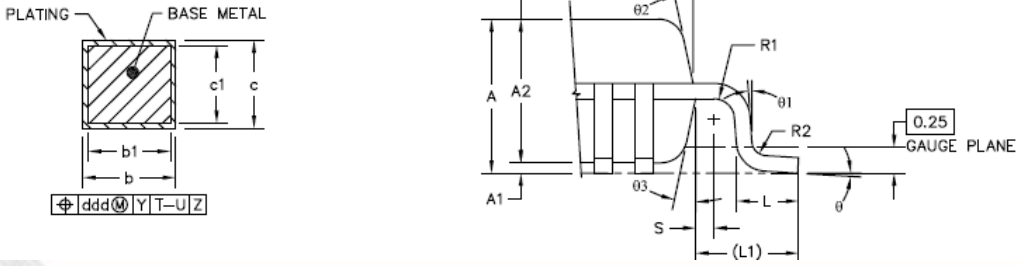
8.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VBUS}	VBUS Current (Steady State)	Standby		50		μA

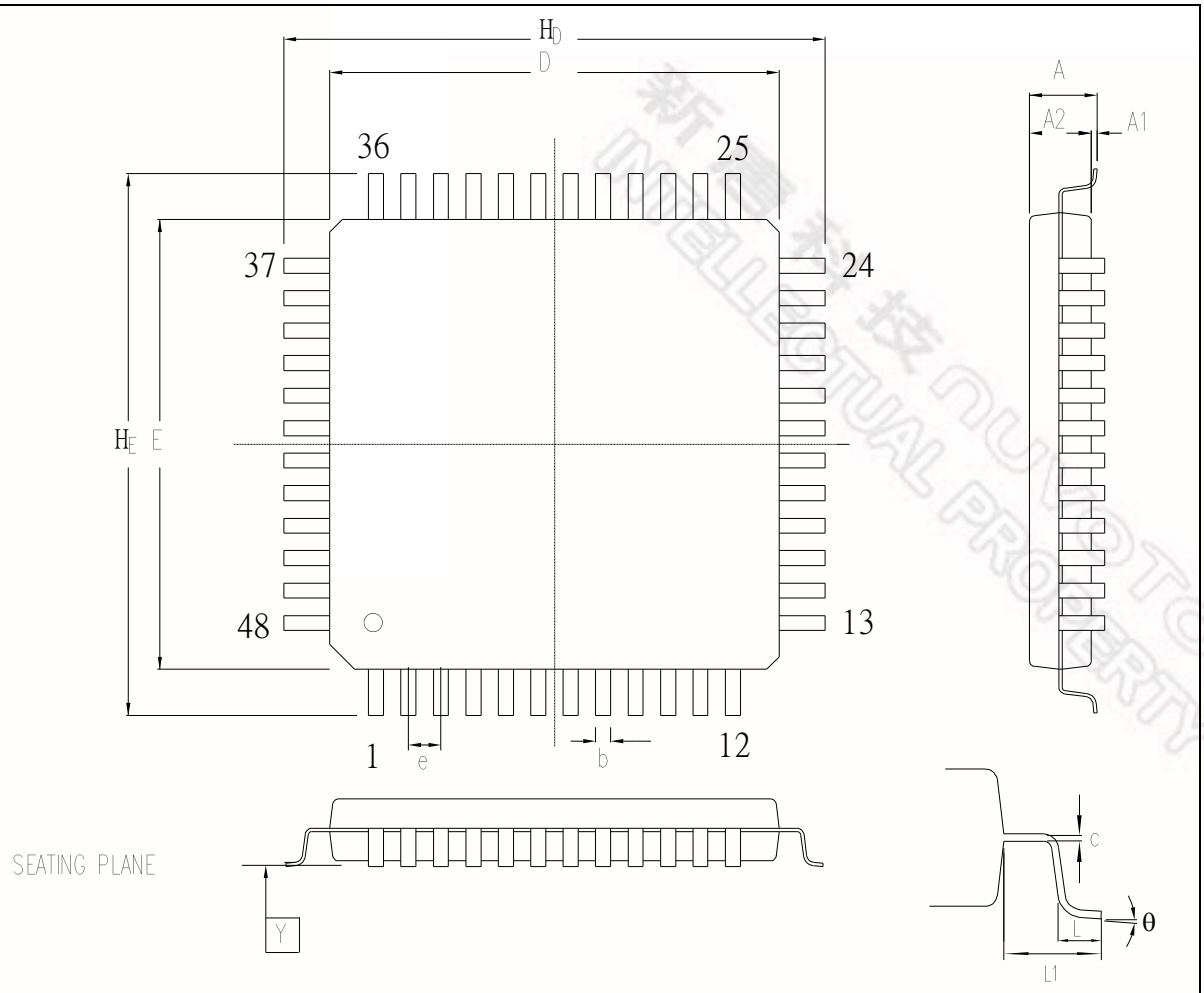
9.2 64-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



9.3 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7