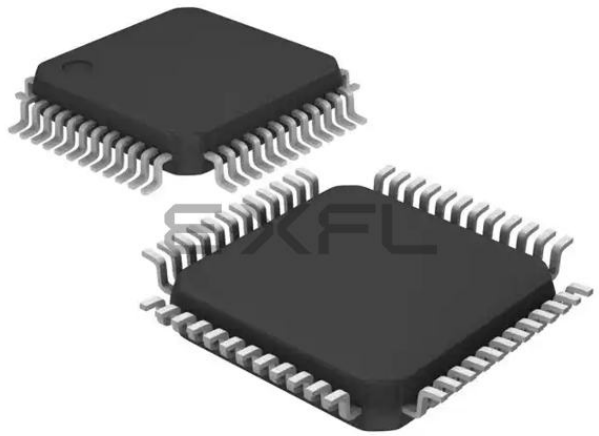

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 7x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc230ld2ae |

# 4 PARTS INFORMATION LIST AND PIN CONFIGURATION

## 4.1 NuMicro™ NUC230/240xxxAE Selection Guide

### 4.1.1 NuMicro™ NUC230 Automotive Line Selection Guide

| Part Number | APROM (KB) | RAM (KB) | Data Flash (KB) | ISP ROM (KB) | I/O | Timer (32-bit) | Connectivity | | | | | | I²S | SC | Comp. | PWM | ADC (12-bit) | RTC | EBI | ISP/ICP/IAP | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | UART | SPI | I²C | USB | LIN | CAN | | | | | | | | | |
| NUC230LC2AE | 32 | 8 | 4 | 8 | 35 | 4 | 5 | 1 | 2 | - | 3 | 2 | 1 | 2 | 1 | 4 | 7 | v | - | v | LQFP48 |
| NUC230LD2AE | 64 | 8 | 4 | 8 | 35 | 4 | 5 | 1 | 2 | - | 3 | 2 | 1 | 2 | 1 | 4 | 7 | v | - | v | LQFP48 |
| NUC230LE3AE | 128 | 16 | Config. | 8 | 35 | 4 | 5 | 1 | 2 | - | 3 | 2 | 1 | 2 | 1 | 4 | 7 | v | - | v | LQFP48 |
| NUC230SC2AE | 32 | 8 | 4 | 8 | 49 | 4 | 5 | 2 | 2 | - | 3 | 2 | 1 | 2 | 2 | 6 | 7 | v | v | v | LQFP64 |
| NUC230SD2AE | 64 | 8 | 4 | 8 | 49 | 4 | 5 | 2 | 2 | - | 3 | 2 | 1 | 2 | 2 | 6 | 7 | v | v | v | LQFP64 |
| NUC230SE3AE | 128 | 16 | Config. | 8 | 49 | 4 | 5 | 2 | 2 | - | 3 | 2 | 1 | 2 | 2 | 6 | 7 | v | v | v | LQFP64 |
| NUC230VE3AE | 128 | 16 | Config. | 8 | 83 | 4 | 6 | 4 | 2 | - | 3 | 2 | 1 | 3 | 2 | 8 | 8 | v | v | v | LQFP100 |

### 4.1.2 NuMicro™ NUC240 Connectivity Line Selection Guide

| Part Number | APROM (KB) | RAM (KB) | Data Flash (KB) | ISP ROM (KB) | I/O | Timer (32-bit) | Connectivity | | | | | | I²S | SC | Comp. | PWM | ADC (12-bit) | RTC | EBI | ISP/ICP/IAP | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | UART | SPI | I²C | USB | LIN | CAN | | | | | | | | | |
| NUC240LC2AE | 32 | 8 | 4 | 8 | 31 | 4 | 4 | 1 | 2 | 1 | 2 | 2 | 1 | 1 | 1 | 4 | 7 | v | - | v | LQFP48 |
| NUC240LD2AE | 64 | 8 | 4 | 8 | 31 | 4 | 4 | 1 | 2 | 1 | 2 | 2 | 1 | 1 | 1 | 4 | 7 | v | - | v | LQFP48 |
| NUC240LE3AE | 128 | 16 | Config. | 8 | 31 | 4 | 4 | 1 | 2 | 1 | 2 | 2 | 1 | 1 | 1 | 4 | 7 | v | - | v | LQFP48 |
| NUC240SC2AE | 32 | 8 | 4 | 8 | 45 | 4 | 5 | 2 | 2 | 1 | 3 | 2 | 1 | 2 | 2 | 4 | 7 | v | v | v | LQFP64 |
| NUC240SD2AE | 64 | 8 | 4 | 8 | 45 | 4 | 5 | 2 | 2 | 1 | 3 | 2 | 1 | 2 | 2 | 4 | 7 | v | v | v | LQFP64 |
| NUC240SE3AE | 128 | 16 | Config. | 8 | 45 | 4 | 5 | 2 | 2 | 1 | 3 | 2 | 1 | 2 | 2 | 4 | 7 | v | v | v | LQFP64 |
| NUC240VE3AE | 128 | 16 | Config. | 8 | 79 | 4 | 6 | 4 | 2 | 1 | 3 | 2 | 1 | 3 | 2 | 8 | 8 | v | v | v | LQFP100 |

#### 4.2.2.3 NuMicro™ NUC240LxxAE LQFP 48 pin

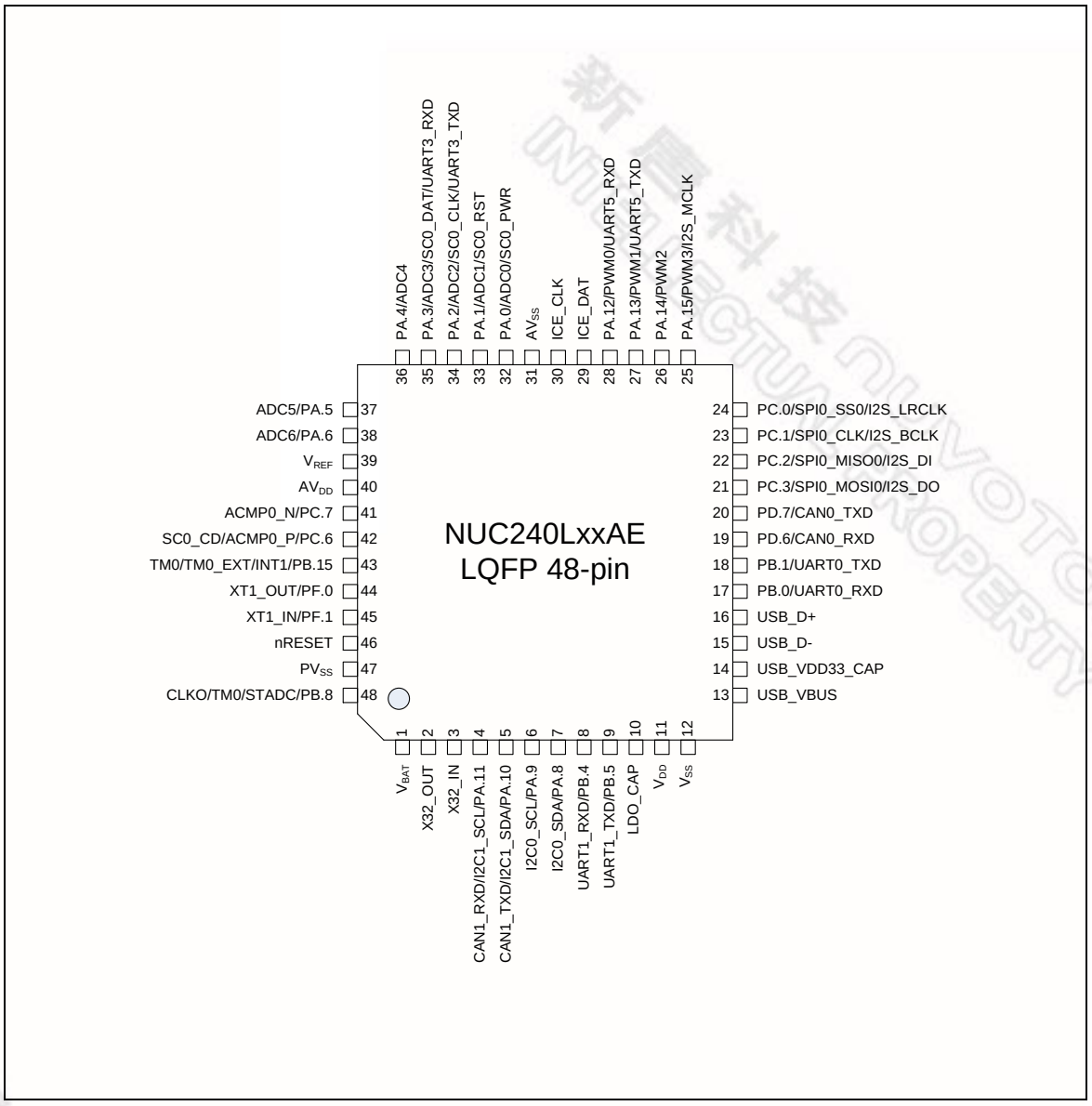



Figure 4-7 NuMicro™ NUC240LxxAE LQFP 48-pin Diagram

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 100-pin | LQFP 64-pin | LQFP 48-pin | | | |
| | | | SPI3_MISO0 | I/O | 1st SPI3 MISO (Master In, Slave Out) pin. |
| 16 | | | PD.11 | I/O | General purpose digital I/O pin. |
| | | | SPI3_MOSI0 | I/O | 1st SPI3 MOSI (Master Out, Slave In) pin. |
| 17 | | | PD.12 | I/O | General purpose digital I/O pin. |
| | | | SPI3_MISO1 | I/O | 2nd SPI3 MISO (Master In, Slave Out) pin. |
| 18 | | | PD.13 | I/O | General purpose digital I/O pin. |
| | | | SPI3_MOSI1 | I/O | 2nd SPI3 MOSI (Master Out, Slave In) pin. |
| 19 | 10 | 8 | PB.4 | I/O | General purpose digital I/O pin. |
| | | | UART1_RXD | I | Data receiver input pin for UART1. |
| 20 | 11 | 9 | PB.5 | I/O | General purpose digital I/O pin. |
| | | | UART1_TXD | O | Data transmitter output pin for UART1. |
| 21 | 12 | | PB.6 | I/O | General purpose digital I/O pin. |
| | | | ALE | O | EBI address latch enable output pin |
| | | | UART1_nRTS | O | Request to Send output pin for UART1. |
| 22 | 13 | | PB.7 | I/O | General purpose digital I/O pin. |
| | | | nCS | O | EBI chip select enable output pin |
| | | | UART1_nCTS | I | Clear to Send input pin for UART1. |
| 23 | 14 | 10 | LDO_CAP | P | LDO output pin. |
| 24 | 15 | 11 | $V_{DD}$ | P | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 25 | 16 | 12 | $V_{SS}$ | P | Ground pin for digital circuit. |
| 26 | | | PE.12 | I/O | General purpose digital I/O pin. |
| 27 | | | PE.11 | I/O | General purpose digital I/O pin. |
| 28 | | | PE.10 | I/O | General purpose digital I/O pin. |
| 29 | | | PE.9 | I/O | General purpose digital I/O pin. |
| 30 | | | PE.8 | I/O | General purpose digital I/O pin. |
| 31 | | | PE.7 | I/O | General purpose digital I/O pin. |
| 32 | 17 | 13 | PB.0 | I/O | General purpose digital I/O pin. |
| | | | UART0_RXD | I | Data receiver input pin for UART0. |
| 33 | 18 | 14 | PB.1 | I/O | General purpose digital I/O pin. |
| | | | UART0_TXD | O | Data transmitter output pin for UART0. |
| 34 | 19 | 15 | PB.2 | I/O | General purpose digital I/O pin. |
| | | | UART0_nRTS | O | Request to Send output pin for UART0. |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 100-pin | LQFP 64-pin | LQFP 48-pin | | | |
| | | | TM2_EXT | I | Timer2 external capture input pin. |
| | | | ACMP0_O | O | Comparator0 output pin. |
| | | | nWRL | O | EBI low byte write enable output pin |
| 35 | 20 | 16 | PB.3 | I/O | General purpose digital I/O pin. |
| | | | UART0_nCTS | I | Clear to Send input pin for UART0. |
| | | | TM3_EXT | I | Timer3 external capture input pin. |
| | | | SC2_CD | I | SmartCard2 card detect pin. |
| | | | nWRH | O | EBI high byte write enable output pin |
| 36 | 21 | 17 | PD.6 | I/O | General purpose digital I/O pin. |
| | | | CAN0_RXD | I | Data receiver input pin for CAN0. |
| 37 | 22 | 18 | PD.7 | I/O | General purpose digital I/O pin. |
| | | | CAN0_TXD | O | Data transmitter output pin for CAN0. |
| 38 | 23 | 19 | PD.14 | I/O | General purpose digital I/O pin. |
| | | | UART2_RXD | I | Data receiver input pin for UART2. |
| | | | CAN1_RXD | I | Data receiver input pin for CAN1. |
| 39 | 24 | 20 | PD.15 | I/O | General purpose digital I/O pin. |
| | | | UART2_TXD | O | Data transmitter output pin for UART2. |
| | | | CAN1_TXD | O | Data transmitter output pin for CAN1. |
| 40 | | | PC.5 | I/O | General purpose digital I/O pin. |
| | | | SPI0_MOSI1 | I/O | 2nd SPI0 MOSI (Master Out, Slave In) pin. |
| 41 | | | PC.4 | I/O | General purpose digital I/O pin. |
| | | | SPI0_MISO1 | I/O | 2nd SPI0 MISO (Master In, Slave Out) pin. |
| 42 | 25 | 21 | PC.3 | I/O | General purpose digital I/O pin. |
| | | | SPI0_MOSI0 | I/O | 1st SPI0 MOSI (Master Out, Slave In) pin. |
| | | | I2S_DO | O | I2S data output. |
| 43 | 26 | 22 | PC.2 | I/O | General purpose digital I/O pin. |
| | | | SPI0_MISO0 | I/O | 1st SPI0 MISO (Master In, Slave Out) pin. |
| | | | I2S_DI | I | I2S data input. |
| 44 | 27 | 23 | PC.1 | I/O | General purpose digital I/O pin. |
| | | | SPI0_CLK | I/O | SPI0 serial clock pin. |
| | | | I2S_BCLK | I/O | I2S bit clock pin. |
| 45 | 28 | 24 | PC.0 | I/O | General purpose digital I/O pin. |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 100-pin | LQFP 64-pin | LQFP 48-pin | | | |
| | | | SC0_RST | **O** | SmartCard0 reset pin. |
| | | | AD12 | **I/O** | EBI Address/Data bus bit12 |
| 73 | 46 | 34 | PA.2 | **I/O** | General purpose digital I/O pin. |
| | | | ADC2 | **AI** | ADC2 analog input. |
| | | | SC0_CLK | **O** | SmartCard0 clock pin. |
| | | | UART3_TXD | **O** | Data transmitter output pin for UART3. |
| | | | AD11 | **I/O** | EBI Address/Data bus bit11 |
| 74 | 47 | 35 | PA.3 | **I/O** | General purpose digital I/O pin. |
| | | | ADC3 | **AI** | ADC3 analog input. |
| | | | SC0_DAT | **O** | SmartCard0 data pin. |
| | | | UART3_RXD | **I** | Data receiver input pin for UART3. |
| | | | AD10 | **I/O** | EBI Address/Data bus bit10 |
| 75 | 48 | 36 | PA.4 | **I/O** | General purpose digital I/O pin. |
| | | | ADC4 | **AI** | ADC4 analog input. |
| | | | AD9 | **I/O** | EBI Address/Data bus bit9 |
| | | | SC1_PWR | **O** | SmartCard1 power pin. |
| 76 | 49 | 37 | PA.5 | **I/O** | General purpose digital I/O pin. |
| | | | ADC5 | **AI** | ADC5 analog input. |
| | | | AD8 | **I/O** | EBI Address/Data bus bit8 |
| | | | SC1_RST | **O** | SmartCard1 reset pin. |
| 77 | 50 | 38 | PA.6 | **I/O** | General purpose digital I/O pin. |
| | | | ADC6 | **AI** | ADC6 analog input. |
| | | | AD7 | **I/O** | EBI Address/Data bus bit7 |
| | | | SC1_CLK | **I/O** | SmartCard1 clock pin. |
| | | | UART4_TXD | **O** | Data transmitter output pin for UART4. |
| 78 | | | PA.7 | **I/O** | General purpose digital I/O pin. |
| | | | ADC7 | **AI** | ADC7 analog input. |
| | | | AD6 | **I/O** | EBI Address/Data bus bit6 |
| | | | SC1_DAT | **O** | SmartCard1 data pin. |
| | | | UART4_RXD | **I** | Data receiver input pin for UART4. |
| | | | SPI2_SS1 | **I/O** | 2nd SPI2 slave select pin. |
| 79 | 51 | 39 | $V_{REF}$ | **AP** | Voltage reference input for ADC. |
| 80 | 52 | 40 | $AV_{DD}$ | **AP** | Power supply for internal analog circuit. |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 100-pin | LQFP 64-pin | LQFP 48-pin | | | |
| 16 | | | PD.11 | **I/O** | General purpose digital I/O pin. |
| | | | SPI3_MOSI0 | **I/O** | 1st SPI3 MOSI (Master Out, Slave In) pin. |
| 17 | | | PD.12 | **I/O** | General purpose digital I/O pin. |
| | | | SPI3_MISO1 | **I/O** | 2nd SPI3 MISO (Master In, Slave Out) pin. |
| 18 | | | PD.13 | **I/O** | General purpose digital I/O pin. |
| | | | SPI3_MOSI1 | **I/O** | 2nd SPI3 MOSI (Master Out, Slave In) pin. |
| 19 | 10 | 8 | PB.4 | **I/O** | General purpose digital I/O pin. |
| | | | UART1_RXD | **I** | Data receiver input pin for UART1. |
| 20 | 11 | 9 | PB.5 | **I/O** | General purpose digital I/O pin. |
| | | | UART1_TXD | **O** | Data transmitter output pin for UART1. |
| 21 | 12 | | PB.6 | **I/O** | General purpose digital I/O pin. |
| | | | ALE | **O** | EBI address latch enable output pin |
| | | | UART1_nRTS | **O** | Request to Send output pin for UART1. |
| 22 | 13 | | PB.7 | **I/O** | General purpose digital I/O pin. |
| | | | nCS | **O** | EBI chip select enable output pin |
| | | | UART1_nCTS | **I** | Clear to Send input pin for UART1. |
| 23 | 14 | 10 | LDO_CAP | **P** | LDO output pin. |
| 24 | 15 | 11 | $V_{DD}$ | **P** | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 25 | 16 | 12 | $V_{SS}$ | **P** | Ground pin for digital circuit. |
| 26 | | | PE.8 | **I/O** | General purpose digital I/O pin. |
| 27 | | | PE.7 | **I/O** | General purpose digital I/O pin. |
| 28 | 17 | 13 | USB_VBUS | **USB** | Power supply from USB host or HUB. |
| 29 | 18 | 14 | USB_$V_{DD}$33_CAP | **USB** | Internal power regulator output 3.3V decoupling pin. |
| 30 | 19 | 15 | USB_D- | **USB** | USB differential signal D-. |
| 31 | 20 | 16 | USB_D+ | **USB** | USB differential signal D+. |
| 32 | 21 | 17 | PB.0 | **I/O** | General purpose digital I/O pin. |
| | | | UART0_RXD | **I** | Data receiver input pin for UART0. |
| 33 | 22 | 18 | PB.1 | **I/O** | General purpose digital I/O pin. |
| | | | UART0_TXD | **O** | Data transmitter output pin for UART0. |
| 34 | 23 | | PB.2 | **I/O** | General purpose digital I/O pin. |
| | | | nWRL | **O** | EBI low byte write enable output pin |
| | | | UART0_nRTS | **O** | Request to Send output pin for UART0. |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 100-pin | LQFP 64-pin | LQFP 48-pin | | | |
| 60 | 35 | | PC.9 | I/O | General purpose digital I/O pin. |
| | | | SPI1_CLK | I/O | SPI1 serial clock pin. |
| 61 | 36 | | PC.8 | I/O | General purpose digital I/O pin. |
| | | | MCLK | O | EBI clock output |
| | | | SPI1_SS0 | I/O | 1st SPI1 slave select pin. |
| 62 | 37 | 25 | PA.15 | I/O | General purpose digital I/O pin. |
| | | | PWM3 | I/O | PWM3 output/Capture input. |
| | | | I2S_MCLK | O | I2S master clock output pin. |
| | | | SC2_PWR | O | SmartCard2 power pin. |
| 63 | 38 | 26 | PA.14 | I/O | General purpose digital I/O pin. |
| | | | PWM2 | I/O | PWM2 output/Capture input. |
| | | | AD15 | I/O | EBI Address/Data bus bit15 |
| | | | SC2_RST | O | SmartCard2 reset pin. |
| 64 | 39 | 27 | PA.13 | I/O | General purpose digital I/O pin. |
| | | | PWM1 | I/O | PWM1 output/Capture input. |
| | | | AD14 | I/O | EBI Address/Data bus bit14 |
| | | | SC2_CLK | O | SmartCard2 clock pin. |
| | | 27 | UART5_TXD | O | Data transmitter output pin for UART5. |
| 65 | 40 | 28 | PA.12 | I/O | General purpose digital I/O pin. |
| | | | PWM0 | I/O | PWM0 output/Capture input. |
| | | | AD13 | I/O | EBI Address/Data bus bit13 |
| | | | SC2_DAT | O | SmartCard2 data pin. |
| | | 28 | UART5_RXD | I | Data receiver input pin for UART5. |
| 66 | 41 | 29 | ICE_DAT | I/O | Serial wire debugger data pin. |
| 67 | 42 | 30 | ICE_CLK | I | Serial wire debugger clock pin. |
| 68 | | | $V_{DD}$ | P | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 69 | | | $V_{SS}$ | P | Ground pin for digital circuit. |
| 70 | 43 | 31 | $AV_{SS}$ | AP | Ground pin for analog circuit. |
| 71 | 44 | 32 | PA.0 | I/O | General purpose digital I/O pin. |
| | | | ADC0 | AI | ADC0 analog input. |
| | | | SC0_PWR | O | SmartCard0 power pin. |
| 72 | 45 | 33 | PA.1 | I/O | General purpose digital I/O pin. |

| | | |
|---|---|---|
| 0x4014_0000 – 0x4014_3FFF | PWMB_BA | PWM4/5/6/7 Control Registers |
| 0x4015_0000 – 0x4015_3FFF | UART1_BA | UART1 Control Registers |
| 0x4015_4000 – 0x4015_7FFF | UART2_BA | UART2 Control Registers |
| 0x4018_0000 – 0x4018_3FFF | CAN0_BA | CAN0 Bus Control Registers |
| 0x4018_4000 – 0x4018_7FFF | CAN1_BA | CAN1 Bus Control Registers |
| 0x4019_0000 – 0x4019_3FFF | SC0_BA | SC0 Control Registers |
| 0x4019_4000 – 0x4019_7FFF | SC1_BA | SC1 Control Registers |
| 0x4019_8000 – 0x4019_BFFF | SC2_BA | SC2 Control Registers |
| 0x401A_0000 – 0x401A_3FFF | I2S_BA | $I^2S$ Interface Control Registers |
| **System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)** | | |
| 0xE000_E010 – 0xE000_E0FF | SCS_BA | System Timer Control Registers |
| 0xE000_E100 – 0xE000_ECFF | SCS_BA | External Interrupt Controller Control Registers |
| 0xE000_ED00 – 0xE000_ED8F | SCS_BA | System Control Registers |

Table 6-1 Address Space Assignments for On-Chip Controllers

### 6.2.6 Nested Vectored Interrupt Controller (NVIC)

The Cortex™-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

## 6.6 General Purpose I/O (GPIO)

### 6.6.1 Overview

The NuMicro™ NUC230/240 series has up to 84 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 84 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B/C/D/E port has the maximum of 16 pins and GPIOF port has the maximum of 4 pins. Each of the 84 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for $V_{DD}$ is from 5.0 V to 2.5 V.

### 6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function.

## 6.7 PDMA Controller (PDMA)

### 6.7.1 Overview

The NuMicro™ NUC230/240 series DMA contains nine-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA that transfers data to and from memory or transfer data to and from APB devices. For PDMA channel (PDMA CH0~CH8), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. Software can stop the PDMA operation by disable PDMA PDMACEN (PDMA_CSRx[0]). The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

The DMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU PIO mode and DMA transfer mode.

## 8.2 DC Electrical Characteristics

($V_{DD}$-$V_{SS}$=5.5 V, $T_A$ = 25°C, $F_{OSC}$ = 50 MHz unless otherwise specified.)

| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| Operation Voltage | $V_{DD}$ | 2.5 | | 5.5 | V | $V_{DD}$ = 2.5V ~ 5.5V up to 72 MHz | | | | |
| Power Ground | $V_{SS}$<br>$AV_{SS}$ | -0.3 | | | V | | | | | |
| LDO Output Voltage | $V_{LDO}$ | 1.62 | 1.8 | 1.98 | V | $V_{DD}$ > 2.5V | | | | |
| Band-gap Voltage | $V_{BG}$ | 1.22 | 1.25 | 1.28 | V | $V_{DD}$ = 2.5 V ~ 5.5 V, $T_A$ = 25°C | | | | |
| Analog Operating Voltage | $AV_{DD}$ | | $V_{DD}$ | | V | When system used analog function, please refer to NUC230/240 Series Technical Reference Manual chapter 6.5 for corresponding analog operating voltage | | | | |
| RTC Operating Voltage | $V_{BAT}$ | 2.5 | | 5.5 | V | | | | | |
| Operating Current Normal Run Mode at 72 MHz while(1){} executed from flash $V_{LDO}$ =1.8 V | $I_{DD1}$ | | 50 | | mA | $V_{DD}$ | HXT | HIRC | PLL | All digital module |
| | | | | | | 5.5V | 12 MHz | X | V | V |
| | $I_{DD2}$ | | 20 | | mA | 5.5V | 12 MHz | X | V | X |
| | $I_{DD3}$ | | 48 | | mA | 3.3V | 12 MHz | X | V | V |
| | $I_{DD4}$ | | 18 | | mA | 3.3V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode at 50 MHz while(1){} executed from flash $V_{LDO}$ =1.8 V | $I_{DD5}$ | | 34 | | mA | 5.5V | 12 MHz | X | V | V |
| | $I_{DD6}$ | | 15 | | mA | 5.5V | 12 MHz | X | V | X |
| | $I_{DD7}$ | | 32 | | mA | 3.3V | 12 MHz | X | V | V |
| | $I_{DD8}$ | | 14 | | mA | 3.3V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode at 12 MHz while(1){} executed from flash $V_{LDO}$ =1.8 V | $I_{DD9}$ | | 8.5 | | mA | 5.5V | 12 MHz | X | X | V |
| | $I_{DD10}$ | | 3.6 | | mA | 5.5V | 12 MHz | X | X | X |
| | $I_{DD11}$ | | 7.5 | | mA | 3.3V | 12 MHz | X | X | V |
| | $I_{DD12}$ | | 2.6 | | mA | 3.3V | 12 MHz | X | X | X |
| Operating Current Normal Run Mode at 4 MHz while(1){} executed from flash $V_{LDO}$ =1.8 V | $I_{DD13}$ | | 3.6 | | mA | 5.5V | 4 MHz | X | X | V |
| | $I_{DD14}$ | | 2 | | mA | 5.5V | 4 MHz | X | X | X |
| | $I_{DD15}$ | | 2.8 | | mA | 3.3V | 4 MHz | X | X | V |
| | $I_{DD16}$ | | 1.2 | | mA | 3.3V | 4 MHz | X | X | X |

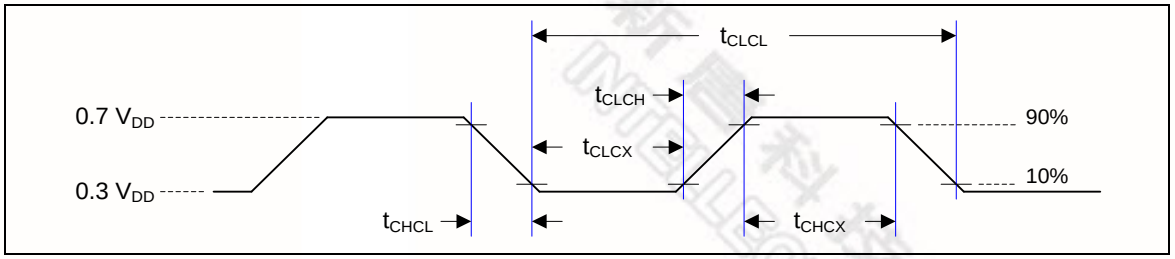
| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| Operating Current<br>Normal Run Mode<br>at 32.768 kHz<br>while(1){} executed from flash<br>$V_{LDO}$ =1.8 V | $I_{DD17}$ | | 141 | | µA | $V_{DD}$ | LXT (kHz) | HIRC | PLL | All digital module |
| | | | | | | 5.5V | 32.768 | X | X | V |
| | $I_{DD18}$ | | 129 | | µA | 5.5V | 32.768 | X | X | X |
| | $I_{DD19}$ | | 138 | | µA | 3.3V | 32.768 | X | X | V |
| | $I_{DD20}$ | | 125 | | µA | 3.3V | 32.768 | X | X | X |
| Operating Current<br>Normal Run Mode<br>at 10 kHz<br>while(1){} executed from flash<br>$V_{LDO}$ =1.8 V | $I_{DD21}$ | | 125 | | µA | $V_{DD}$ | HXT/LXT | LIRC (kHz) | PLL | All digital module |
| | | | | | | 5.5V | X | 10 | X | V |
| | $I_{DD22}$ | | 120 | | µA | 5.5V | X | 10 | X | X |
| | $I_{DD23}$ | | 125 | | µA | 3.3V | X | 10 | X | V |
| | $I_{DD24}$ | | 120 | | µA | 3.3V | X | 10 | X | X |
| Operating Current<br>Idle Mode<br>at 72 MHz<br>$V_{LDO}$ =1.8 V | $I_{IDLE1}$ | | 42 | | mA | $V_{DD}$ | HXT | HIRC | PLL | All digital module |
| | | | | | | 5.5V | 12 MHz | X | V | V |
| | $I_{IDLE2}$ | | 11 | | mA | 5.5V | 12 MHz | X | V | X |
| | $I_{IDLE3}$ | | 41 | | mA | 3.3V | 12 MHz | X | V | V |
| | $I_{IDLE4}$ | | 9 | | mA | 3.3V | 12 MHz | X | V | X |
| Operating Current<br>Idle Mode<br>at 50 MHz<br>$V_{LDO}$ =1.8 V | $I_{IDLE5}$ | | 28 | | mA | 5.5V | 12 MHz | X | V | V |
| | $I_{IDLE6}$ | | 10 | | mA | 5.5V | 12 MHz | X | V | X |
| | $I_{IDLE7}$ | | 27 | | mA | 3.3V | 12 MHz | X | V | V |
| | $I_{IDLE8}$ | | 9 | | mA | 3.3V | 12 MHz | X | V | X |
| Operating Current<br>Idle Mode<br>at 12 MHz<br>$V_{LDO}$ =1.8 V | $I_{IDLE9}$ | | 7.5 | | mA | 5.5V | 12 MHz | X | X | V |
| | $I_{IDLE10}$ | | 2.4 | | mA | 5.5V | 12 MHz | X | X | X |
| | $I_{IDLE11}$ | | 6.5 | | mA | 3.3V | 12 MHz | X | X | V |
| | $I_{IDLE12}$ | | 1.5 | | mA | 3.3V | 12 MHz | X | X | X |
| Operating Current<br>Idle Mode<br>at 4 MHz<br>$V_{LDO}$ =1.8 V | $I_{IDLE13}$ | | 3.3 | | mA | 5.5V | 4 MHz | X | X | V |
| | $I_{IDLE14}$ | | 1.7 | | mA | 5.5V | 4 MHz | X | X | X |
| | $I_{IDLE15}$ | | 2.4 | | mA | 3.3V | 4 MHz | X | X | V |
| | $I_{IDLE16}$ | | 0.8 | | mA | 3.3V | 4 MHz | X | X | X |
| Operating Current<br>Idle Mode<br>at 32.768 kHz<br>$V_{LDO}$ =1.8 V | $I_{IDLE17}$ | | 133 | | µA | $V_{DD}$ | LXT (kHz) | HIRC | PLL | All digital module |
| | | | | | | 5.5V | 32.768 | X | X | V |
| | $I_{IDLE18}$ | | 120 | | µA | 5.5V | 32.768 | X | X | X |

| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | | | | | |
| | $I_{IDLE19}$ | | 133 | | µA | 3.3V | 32.768 | X | X | V |
| | $I_{IDLE20}$ | | 120 | | µA | 3.3V | 32.768 | X | X | X |
| Operating Current Idle Mode at 10 kHz | $I_{IDLE21}$ | | 122 | | µA | $V_{DD}$ | HXT/LXT | LIRC (kHz) | PLL | All digital module |
| | | | | | | 5.5V | X | 10 | X | V |
| | $I_{IDLE22}$ | | 118 | | µA | 5.5V | X | 10 | X | X |
| | $I_{IDLE23}$ | | 122 | | µA | 3.3V | X | 10 | X | V |
| | $I_{IDLE24}$ | | 118 | | µA | 3.3V | X | 10 | X | X |
| Standby Current Power-down Mode (Deep Sleep Mode) $V_{LDO}$ =1.6 V | $I_{PWD1}$ | | 15 | | µA | $V_{DD}$ | HXT/HIRC PLL | LXT (kHz) | RTC | RAM retension |
| | | | | | | 5.5V | X | X | X | V |
| | $I_{PWD2}$ | | 15 | | µA | 5.5V | X | X | X | V |
| | $I_{PWD3}$ | | 17 | | µA | 3.3V | X | 32.768 | V | V |
| | $I_{PWD4}$ | | 17 | | µA | 3.3V | X | 32.768 | V | V |
| RTC Operating Current | $I_{VBAT}$ | | 1.6 | | µA | $V_{BAT}$= 3.0V, RTC enabled | | | | |
| Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode) | $I_{IN1}$ | | -50 | -60 | µA | $V_{DD}$ = 5.5V, $V_{IN}$ = 0V or $V_{IN}$=$V_{DD}$ | | | | |
| Input Current at /RESET[1] | $I_{IN2}$ | -55 | -45 | -30 | µA | $V_{DD}$ = 3.3V, $V_{IN}$ = 0.45V | | | | |
| Input Leakage Current PA, PB, PC, PD, PE, PF | $I_{LK}$ | -2 | - | +2 | µA | $V_{DD}$ = 5.5V, 0<$V_{IN}$<$V_{DD}$ | | | | |
| Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode) | $I_{TL}$ [3] | -650 | - | -200 | µA | $V_{DD}$ = 5.5V, $V_{IN}$<2.0V | | | | |
| Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input) | $V_{IL1}$ | -0.3 | - | 0.8 | V | $V_{DD}$ = 4.5V | | | | |
| | | -0.3 | - | 0.6 | | $V_{DD}$ = 2.5V | | | | |
| Input High Voltage PA, PB, PC, PD, PE, PF (TTL input) | $V_{IH1}$ | 2.0 | - | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V | | | | |
| | | 1.5 | - | $V_{DD}$ +0.2 | | $V_{DD}$ =3.0V | | | | |
| Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input) | $V_{IL2}$ | -0.3 | - | 0.3$V_{DD}$ | V | | | | | |
| Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input) | $V_{IH2}$ | 0.7$V_{DD}$ | - | $V_{DD}$ +0.2 | V | | | | | |

| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Hysteresis voltage of PA, PB, PC, PD,PE, PF (Schmitt input) | $V_{HY}$ | | $0.2V_{DD}$ | | V | |
| Input Low Voltage XT1_IN[*2] | $V_{IL3}$ | 0 | - | 0.8 | V | $V_{DD}$ = 4.5V |
| | | 0 | - | 0.4 | | $V_{DD}$ = 3.0V |
| Input High Voltage XT1_IN[*2] | $V_{IH3}$ | 3.5 | - | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V |
| | | 2.4 | - | $V_{DD}$ +0.2 | | $V_{DD}$ = 3.0V |
| Input Low Voltage X32I[*2] | $V_{IL4}$ | 0 | - | 0.4 | v | |
| Input High Voltage X32I[*2] | $V_{IH4}$ | 1.2 | | 1.8 | V | |
| Negative going threshold (Schmitt input), /RESET | $V_{ILS}$ | -0.5 | - | $0.2V_{DD}$ -0.2 | V | |
| Positive going threshold (Schmitt input), /RESET | $V_{IHS}$ | $0.7V_{DD}$ | - | $V_{DD}$ +0.5 | V | |
| Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode) | $I_{SR11}$ | -300 | -370 | -450 | µA | $V_{DD}$ = 4.5V, $V_S$ = 2.4V |
| | $I_{SR12}$ | -50 | -70 | -90 | µA | $V_{DD}$ = 2.7V, $V_S$ = 2.2V |
| | $I_{SR12}$ | -40 | -60 | -80 | µA | $V_{DD}$ = 2.5V, $V_S$ = 2.0V |
| Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode) | $I_{SR21}$ | -24 | -28 | -32 | mA | $V_{DD}$ = 4.5V, $V_S$ = 2.4V |
| | $I_{SR22}$ | -4 | -6 | -8 | mA | $V_{DD}$ = 2.7V, $V_S$ = 2.2V |
| | $I_{SR22}$ | -3 | -5 | -7 | mA | $V_{DD}$ = 2.5V, $V_S$ = 2.0V |
| Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode) | $I_{SK1}$ | 10 | 16 | 20 | mA | $V_{DD}$ = 4.5V, $V_S$ = 0.45V |
| | $I_{SK1}$ | 7 | 10 | 13 | mA | $V_{DD}$ = 2.7V, $V_S$ = 0.45V |
| | $I_{SK1}$ | 6 | 9 | 12 | mA | $V_{DD}$ = 2.5V, $V_S$ = 0.45V |
| Brown-out Voltage with BOD_VL [1:0] = 00b | $V_{BO2.2}$ | 2.1 | 2.2 | 2.3 | V | |
| Brown-out Voltage with BOD_VL [1:0] = 01b | $V_{BO2.7}$ | 2.6 | 2.7 | 2.8 | V | |
| Brown-out voltage with BOD_VL [1:0] = 10b | $V_{BO3.7}$ | 3.5 | 3.7 | 3.9 | V | |
| Brown-out Voltage with BOD_VL [1:0] = 11b | $V_{BO4.4}$ | 4.2 | 4.4 | 4.6 | V | |

## 8.3 AC Electrical Characteristics

### 8.3.1 External 4~24 MHz High Speed Oscillator




**Note:** Duty cycle is 50%.

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $t_{CHCX}$ | Clock High Time | | 10 | - | - | nS |
| $t_{CLCX}$ | Clock Low Time | | 10 | - | - | nS |
| $t_{CLCH}$ | Clock Rise Time | | 2 | - | 15 | nS |
| $t_{CHCL}$ | Clock Fall Time | | 2 | - | 15 | nS |

### 8.3.2 External 4~24 MHz High Speed Crystal

| PARAMETER | CONDITION | MIN. | TYP.. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage $V_{DD}$ | - | 2.5 | - | 5.5 | V |
| Temperature | - | -40 | - | 105 | ℃ |
| Operating Current | 12 MHz at $V_{DD}$ = 5V | - | 2 | - | mA |
| Clock Frequency | External crystal | 4 | | 24 | MHz |

#### *8.3.2.1 Typical Crystal Application Circuits*

| CRYSTAL | C1 | C2 | R |
|---|---|---|---|
| 4 MHz ~ 24 MHz | 10~20pF | 10~20pF | without |

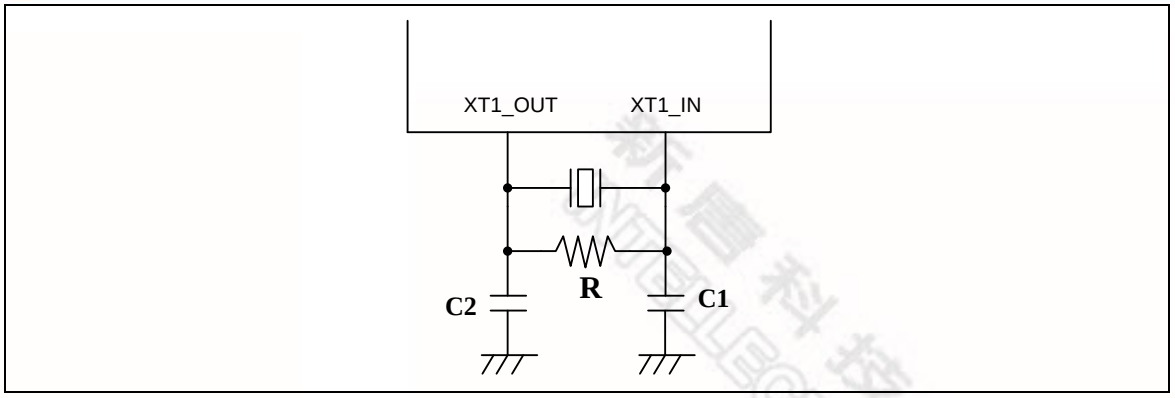



Figure 8-1 Typical Crystal Application Circuit

### 8.3.3 External 32.768 kHz Low Speed Crystal Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage $V_{DD}$ | - | 2.5 | - | 5.5 | V |
| Operation Temperature | - | -40 | - | 105 | ℃ |
| Operation Current | 32.768KHz at $V_{DD}$=5V | | 1.6 | | μA |
| Clock Frequency | External crystal | - | 32.768 | - | kHz |

### 8.3.4 Internal 22.1184 MHz High Speed Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage $V_{DD}$ | - | 2.5 | - | 5.5 | V |
| Center Frequency | - | - | 22.1184 | - | MHz |
| Calibrated Internal Oscillator Frequency | +25℃; $V_{DD}$ =5 V | -1 | - | +1 | % |
| | -40℃~+105℃; $V_{DD}$=2.5 V~5.5 V | -3 | - | +3 | % |
| Operation Current | $V_{DD}$ =5 V | - | 800 | - | uA |

### 8.3.5 Internal 10 kHz Low Speed Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation Voltage $V_{DD}$ | - | 2.5 | - | 5.5 | V |
| Center Frequency | - | - | 10 | - | kHz |
| Calibrated Internal Oscillator Frequency | +25℃; $V_{DD}$ =5 V | -20 | - | +20 | % |
| | -40℃~+105℃; $V_{DD}$=2.5 V~5.5 V | -50 | - | +50 | % |

## 8.4 Analog Characteristics

### 8.4.1 12-bit SARADC Specification

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| - | Resolution | - | - | 12 | Bit |
| DNL | Differential nonlinearity error | - | -1~2 | -1~4 | LSB |
| INL | Integral nonlinearity error | - | ±2 | ±4 | LSB |
| EO | Offset error | - | 2 | 4 | LSB |
| EG | Gain error (Transfer gain) | - | -2 | -4 | - |
| - | Monotonic | Guaranteed | | | |
| $F_{ADC}$ | ADC clock frequency ($AV_{DD}$ = 5V/3V) | - | - | 16/8 | MHz |
| $F_S$ | Sample rate | - | - | 1 | MSPS |
| $V_{DDA}$ | Supply voltage | 3 | - | 5.5 | V |
| $I_{DDA}$ | Supply current (Avg.) | | 2.9 | | mA |
| $V_{REF}$ | Reference voltage | 3 | | $V_{DDA}$ | V |
| $V_{IN}$ | Input voltage | 0 | - | $V_{REF}$ | V |

### 8.4.2 LDO and Power Management Specification

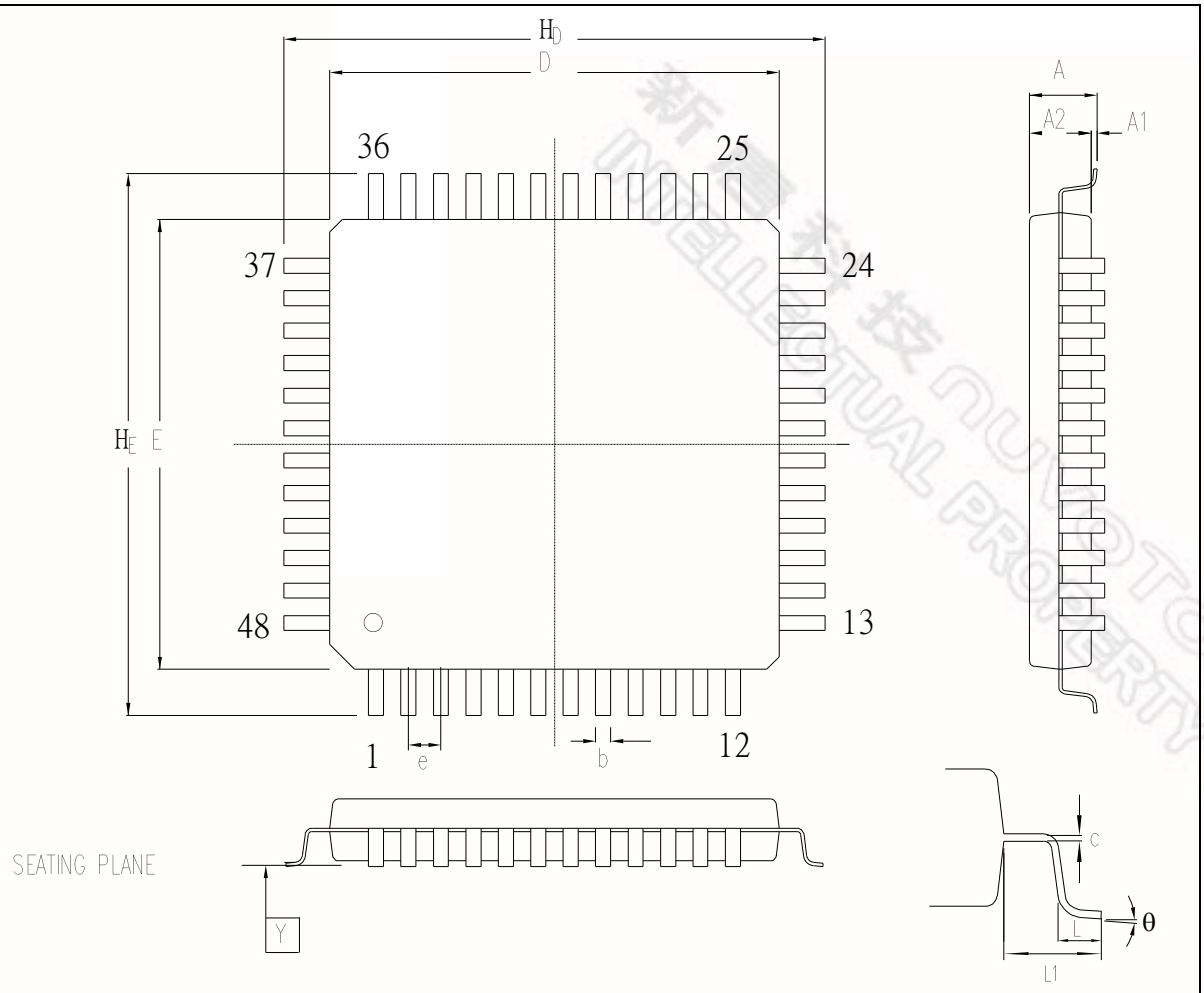
| PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|
| Input Voltage $V_{DD}$ | 2.5 | | 5.5 | V | $V_{DD}$ input voltage |
| Output Voltage | 1.62 | 1.8 | 1.98 | V | $V_{DD}$ > 2.5 V |
| Operating Temperature | -40 | 25 | 105 | ℃ | |
| Cbp | - | 1 | - | μF | $R_{ESR}$ = 1 Ω |

**Note:**

1. It is recommended that a 10 uF or higher capacitor and a 100 nF bypass capacitor are connected between $V_{DD}$ and the closest $V_{SS}$ pin of the device.

2. To ensure power stability, an 1 μF or higher capacitor must be connected between LDO_CAP pin and the closest $V_{SS}$ pin of the device.

## 9.3 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)




Controlling dimension : Millimeters

| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | — | — | — | — |
| $A_1$ | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| $A_2$ | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.006 | 0.008 | 0.010 | 0.15 | 0.20 | 0.25 |
| c | 0.004 | 0.006 | 0.008 | 0.10 | 0.15 | 0.20 |
| D | 0.272 | 0.276 | 0.280 | 6.90 | 7.00 | 7.10 |
| E | 0.272 | 0.276 | 0.280 | 6.90 | 7.00 | 7.10 |
| e | 0.014 | 0.020 | 0.026 | 0.35 | 0.50 | 0.65 |
| $H_D$ | 0.350 | 0.354 | 0.358 | 8.90 | 9.00 | 9.10 |
| $H_E$ | 0.350 | 0.354 | 0.358 | 8.90 | 9.00 | 9.10 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| $L_1$ | — | 0.039 | — | — | 1.00 | — |
| Y | — | — | 0.004 | — | — | 0.10 |
| θ | 0 | — | 7 | 0 | — | 7 |

## 10 REVISION HISTORY

| REVISION | DATE | DESCRIPTION |
|---|---|---|
| 1.00 | May 12, 2014 | Preliminary version |
| 1.01 | Dec. 30,2014 | 1, Added EBI function<br>2, Rearranged the chepter sequence. |

## Important Notice

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