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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	49
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc230sd2ae

- 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
- Wake-up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog time-out
- Supports 4 selectable Watchdog Timer reset delay period(1026, 130, 18 or 3 WDT_CLK)

- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports battery power pin (VBAT)
  - Supports wake-up function
- PWM/Capture
  - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Supports One-shot or Auto-reload mode
  - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to six UART controllers (three UART controllers are shared with SC)
  - UART ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports CTS wake-up function (UART0 and UART1 support)
  - Supports PDMA mode
- Smart Card Host (SC)
  - Supports up to three ISO-7816-3 ports
    - Compliant to ISO-7816-3 T=0, T=1
    - Separate receive / transmit 4 bytes entry FIFO for data payloads
    - Programmable transmission clock frequency
    - Programmable receiver buffer trigger level
    - Programmable guard time selection (11 ETU ~ 266 ETU)
    - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
    - Supports auto inverse convention function
    - Supports transmitter and receiver error retry and error limit function
    - Supports hardware activation sequence process
    - Supports hardware warm reset sequence process
    - Supports hardware deactivation sequence process
    - Supports hardware auto deactivation sequence when detecting the card is removal
  - Supports up to three UART ports
    - Full duplex, asynchronous communications
    - Supports receiving / transmitting 4-bytes FIFO
    - Supports programmable baud rate generator for each channel
    - Programmable even, odd or no parity bit generation and detection
    - Programmable stop bit, 1 or 2 stop bit generation

- SPI
  - Up to four sets of SPI controllers
  - The maximum SPI clock rate of Master can up to 36 MHz (chip working at 5V)
  - The maximum SPI clock rate of Slave can up to 18 MHz (chip working at 5V)
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports PDMA mode
  - Supports three wire, no slave select signal, bi-direction interface
- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- I^2S
  - Interface with external audio CODEC
  - Operate as either Master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - Software override bus
- CAN 2.0
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Support wake-up function
- ADC
  - 12-bit SAR ADC with 1 MSPS (chip working at 5V)
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan

- Supports SPI Master/Slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
- Supports Byte Suspend mode in 32-bit transmission
- Supports PDMA mode
- Supports three wire, no slave select signal, bi-direction interface

- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- I^2S
  - Interface with external audio CODEC
  - Operate as either Master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - Software override bus
- CAN 2.0
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Supports Power-down wake-up function
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB Transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Includes 512 Bytes internal SRAM as USB buffer

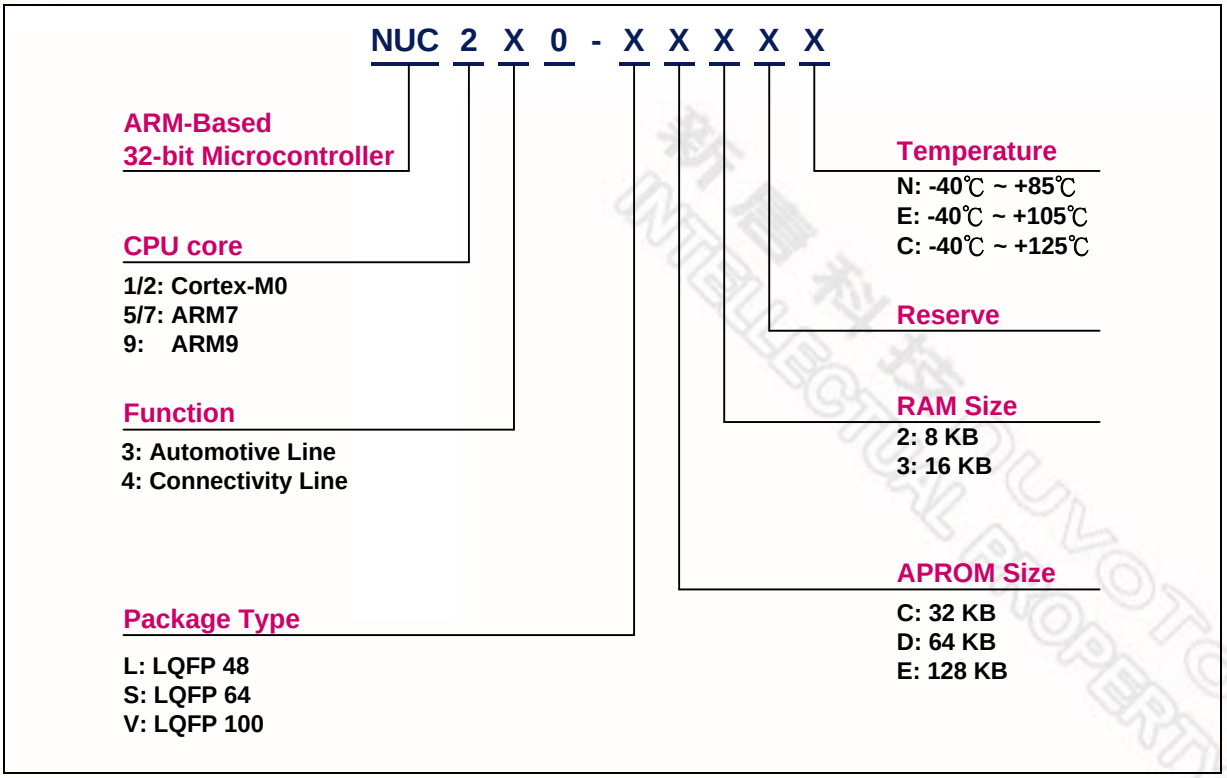

Figure 4-1 NuMicro™ NUC230/240 Series Selection Code

4.2 Pin Configuration

4.2.1 NuMicro™ NUC230 Pin Diagram

4.2.1.1 NuMicro™ NUC230VxxAE LQFP 100 pin

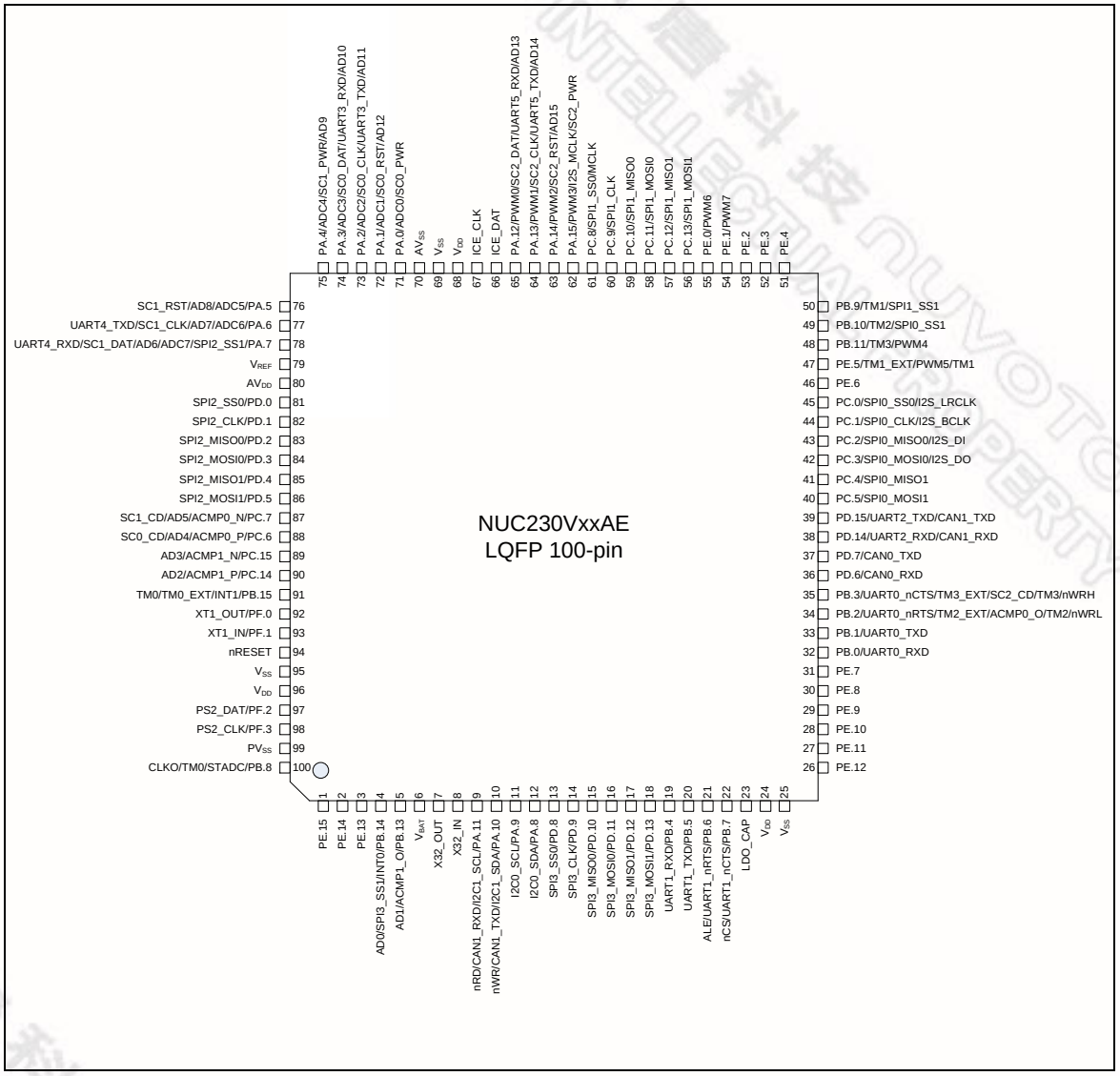

Figure 4-2 NuMicro™ NUC230VxxAE LQFP 100-pin Diagram

4.2.2 NuMicro™ NUC240 Pin Diagram

4.2.2.1 NuMicro™ NUC240VxxAE LQFP 100 pin

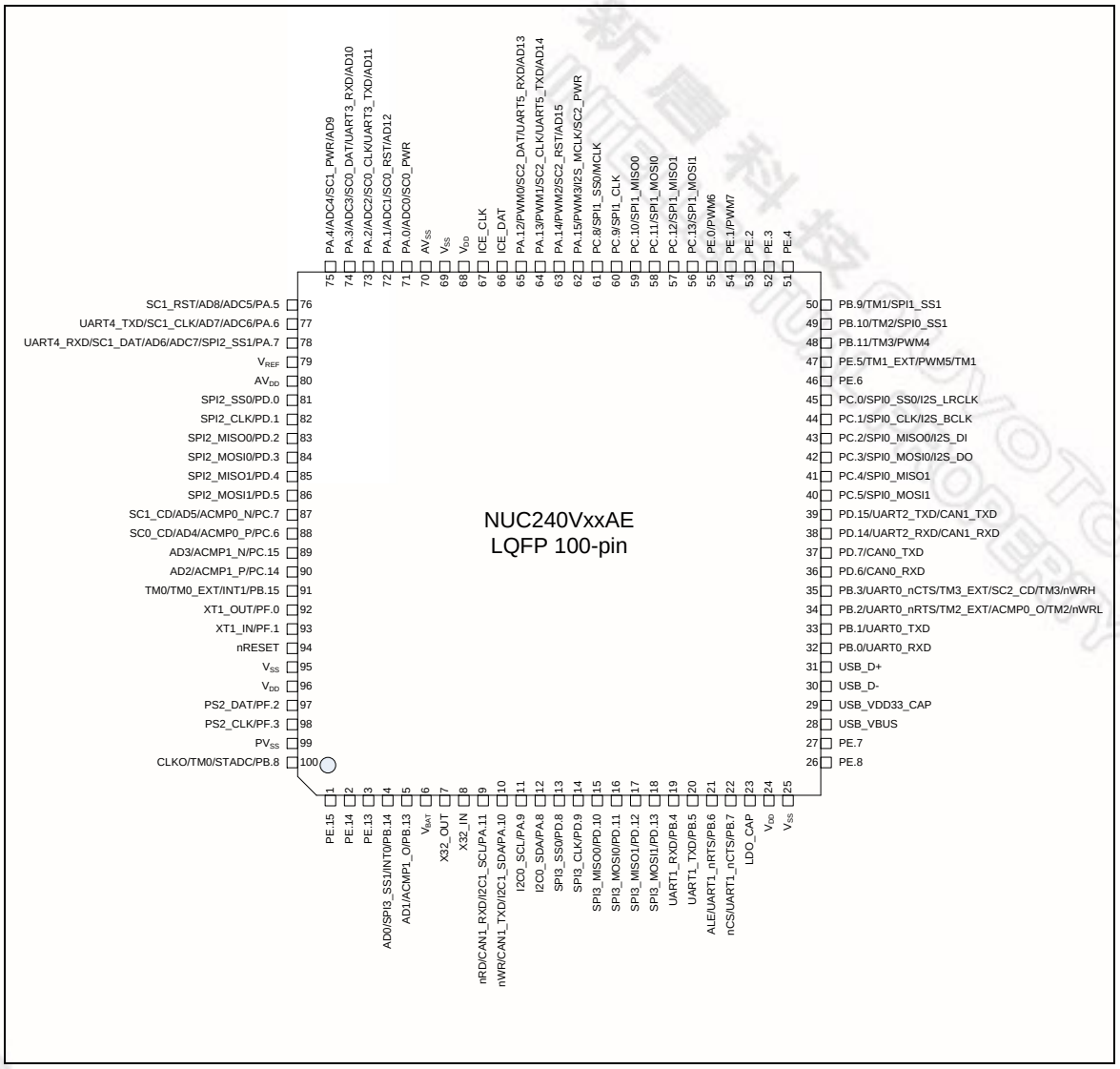

Figure 4-5 NuMicro™ NUC240VxxAE LQFP 100-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SPI1_CLK	**I/O**	SPI1 serial clock pin.
61	36		PC.8	**I/O**	General purpose digital I/O pin.
			MCLK	**O**	EBI clock output
			SPI1_SS0	**I/O**	1st SPI1 slave select pin.
62	37	25	PA.15	**I/O**	General purpose digital I/O pin.
			PWM3	**I/O**	PWM output/Capture input.
			I2S_MCLK	**O**	I^2S master clock output pin.
			SC2_PWR	**O**	SmartCard2 power pin.
63	38	26	PA.14	**I/O**	General purpose digital I/O pin.
			PWM2	**I/O**	PWM2 output/Capture input.
			SC2_RST	**O**	SmartCard2 reset pin.
			AD15	**I/O**	EBI Address/Data bus bit15
64	39	27	PA.13	**I/O**	General purpose digital I/O pin.
			PWM1	**I/O**	PWM1 output/Capture input.
			SC2_CLK	**O**	SmartCard2 clock pin.
			UART5_TXD	**O**	Data transmitter output pin for UART5.
			AD14	**I/O**	EBI Address/Data bus bit14
65	40	28	PA.12	**I/O**	General purpose digital I/O pin.
			PWM0	**I/O**	PWM0 output/Capture input.
			SC2_DAT	**O**	SmartCard2 data pin.
			UART5_RXD	**I**	Data receiver input pin for UART5.
			AD13	**I/O**	EBI Address/Data bus bit13
66	41	29	ICE_DAT	**I/O**	Serial wire debugger data pin.
67	42	30	ICE_CLK	**I**	Serial wire debugger clock pin.
68			V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V_{SS}	**P**	Ground pin for digital circuit.
70	43	31	AV_{SS}	**AP**	Ground pin for analog circuit.
71	44	32	PA.0	**I/O**	General purpose digital I/O pin.
			ADC0	**AI**	ADC0 analog input.
			SC0_PWR	**O**	SmartCard0 power pin.
72	45	33	PA.1	**I/O**	General purpose digital I/O pin.
			ADC1	**AI**	ADC1 analog input.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SC0_RST	**O**	SmartCard0 reset pin.
			AD12	**I/O**	EBI Address/Data bus bit12
73	46	34	PA.2	**I/O**	General purpose digital I/O pin.
			ADC2	**AI**	ADC2 analog input.
			SC0_CLK	**O**	SmartCard0 clock pin.
			UART3_TXD	**O**	Data transmitter output pin for UART3.
			AD11	**I/O**	EBI Address/Data bus bit11
74	47	35	PA.3	**I/O**	General purpose digital I/O pin.
			ADC3	**AI**	ADC3 analog input.
			SC0_DAT	**O**	SmartCard0 data pin.
			UART3_RXD	**I**	Data receiver input pin for UART3.
			AD10	**I/O**	EBI Address/Data bus bit10
75	48	36	PA.4	**I/O**	General purpose digital I/O pin.
			ADC4	**AI**	ADC4 analog input.
			AD9	**I/O**	EBI Address/Data bus bit9
			SC1_PWR	**O**	SmartCard1 power pin.
76	49	37	PA.5	**I/O**	General purpose digital I/O pin.
			ADC5	**AI**	ADC5 analog input.
			AD8	**I/O**	EBI Address/Data bus bit8
			SC1_RST	**O**	SmartCard1 reset pin.
77	50	38	PA.6	**I/O**	General purpose digital I/O pin.
			ADC6	**AI**	ADC6 analog input.
			AD7	**I/O**	EBI Address/Data bus bit7
			SC1_CLK	**I/O**	SmartCard1 clock pin.
			UART4_TXD	**O**	Data transmitter output pin for UART4.
78			PA.7	**I/O**	General purpose digital I/O pin.
			ADC7	**AI**	ADC7 analog input.
			AD6	**I/O**	EBI Address/Data bus bit6
			SC1_DAT	**O**	SmartCard1 data pin.
			UART4_RXD	**I**	Data receiver input pin for UART4.
			SPI2_SS1	**I/O**	2nd SPI2 slave select pin.
79	51	39	V_{REF}	**AP**	Voltage reference input for ADC.
80	52	40	AV_{DD}	**AP**	Power supply for internal analog circuit.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			ADC1	AI	ADC1 analog input.
			SC0_RST	O	SmartCard0 reset pin.
			AD12	I/O	EBI Address/Data bus bit12
73	46	34	PA.2	I/O	General purpose digital I/O pin.
			ADC2	AI	ADC2 analog input.
			SC0_CLK	O	SmartCard0 clock pin.
			UART3_TXD	O	Data transmitter output pin for UART3.
			AD11	I/O	EBI Address/Data bus bit11
74	47	35	PA.3	I/O	General purpose digital I/O pin.
			ADC3	AI	ADC3 analog input.
			SC0_DAT	O	SmartCard0 data pin.
			UART3_RXD	I	Data receiver input pin for UART3.
			AD10	I/O	EBI Address/Data bus bit10
75	48	36	PA.4	I/O	General purpose digital I/O pin.
			ADC4	AI	ADC4 analog input.
			AD9	I/O	EBI Address/Data bus bit9
			SC1_PWR	O	SmartCard1 power pin.
76	49	37	PA.5	I/O	General purpose digital I/O pin.
			ADC5	AI	ADC5 analog input.
			AD8	I/O	EBI Address/Data bus bit8
			SC1_RST	O	SmartCard1 reset pin.
77	50	38	PA.6	I/O	General purpose digital I/O pin.
			ADC6	AI	ADC6 analog input.
			AD7	I/O	EBI Address/Data bus bit7
			SC1_CLK	I/O	SmartCard1 clock pin.
			UART4_TXD	O	Data transmitter output pin for UART4.
78			PA.7	I/O	General purpose digital I/O pin.
			ADC7	AI	ADC7 analog input.
			AD6	I/O	EBI Address/Data bus bit6
			SC1_DAT	O	SmartCard1 data pin.
			UART4_RXD	I	Data receiver input pin for UART4.
			SPI2_SS1	I/O	2nd SPI2 slave select pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
92	58	44	PF.0	**I/O**	General purpose digital I/O pin.
			XT1_OUT	**O**	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	**I/O**	General purpose digital I/O pin.
			XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
94	60	46	nRESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V_{SS}	**P**	Ground pin for digital circuit.
96	62		V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	**I/O**	General purpose digital I/O pin.
			PS2_DAT	**I/O**	PS/2 data pin.
98			PF.3	**I/O**	General purpose digital I/O pin.
			PS2_CLK	**I/O**	PS/2 clock pin.
99	63	47	PV_{SS}	**P**	PLL ground.
100	64	48	PB.8	**I/O**	General purpose digital I/O pin.
			STADC	**I**	ADC external trigger input.
			TM0	**I/O**	Timer0 event counter input / toggle output.
			CLKO	**O**	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**SPI2_INT**	SPI2	SPI2 interrupt
33	17	**SPI3_INT**	SPI3	SPI3 interrupt
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**-**	-	Reserved
37	21	**-**	-	Reserved
38	22	**SC012_INT**	SC0/1/2	SC0, SC1 and SC2 interrupt
39	23	**USB_INT**	USBD	USB 2.0 FS Device interrupt
40	24	**PS2_INT**	PS/2	PS/2 interrupt
41	25	**ACMP_INT**	ACMP	Analog Comparator interrupt
42	26	**PDMA_INT**	PDMA	PDMA interrupt
43	27	**I2S_INT**	I^2S	I^2S interrupt
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state
45	29	**ADC_INT**	ADC	ADC interrupt
46	30	**IRC_INT**	IRC	IRC TRIM interrupt
47	31	**RTC_INT**	RTC	Real Time Clock interrupt

Table 6-3 System Interrupt Map

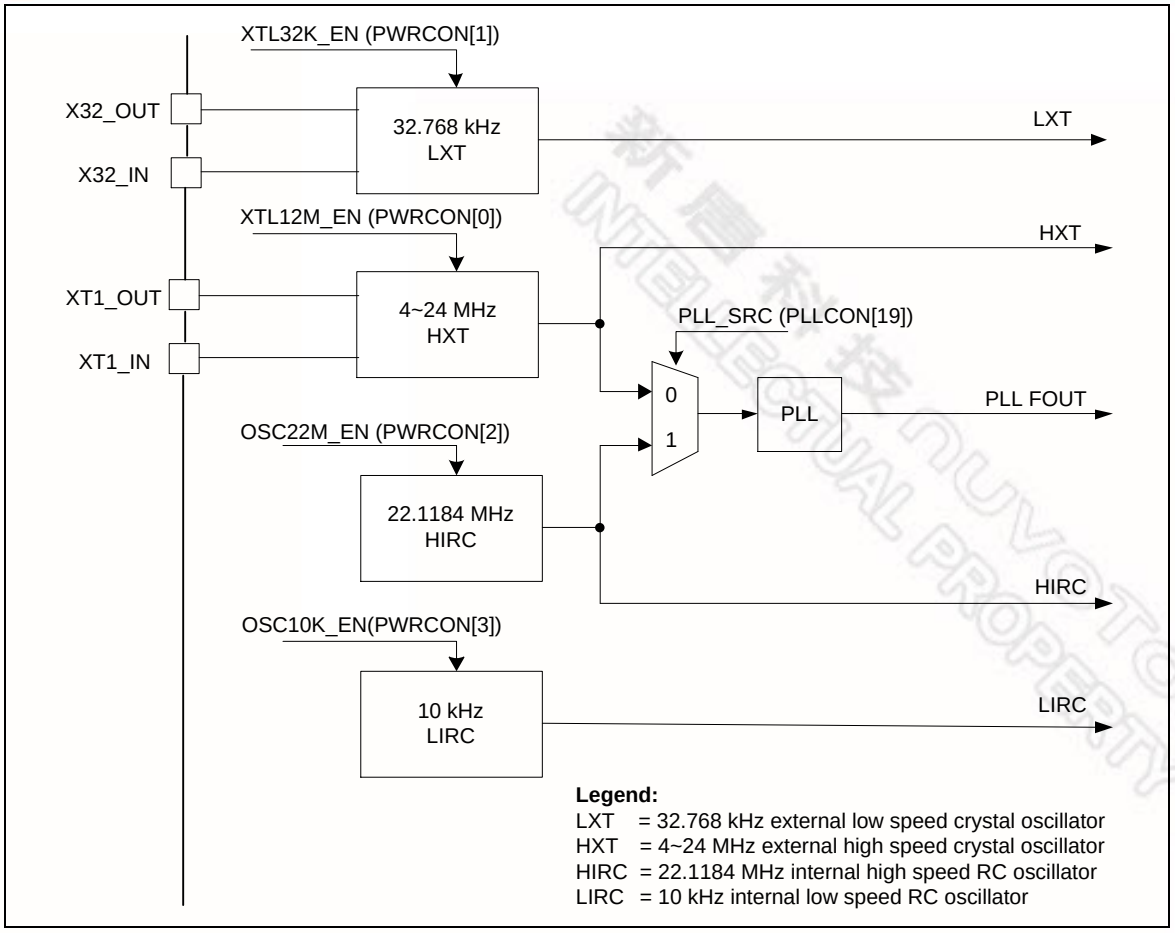

Figure 6-4 Clock Generator Block Diagram

6.3.2 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-6.

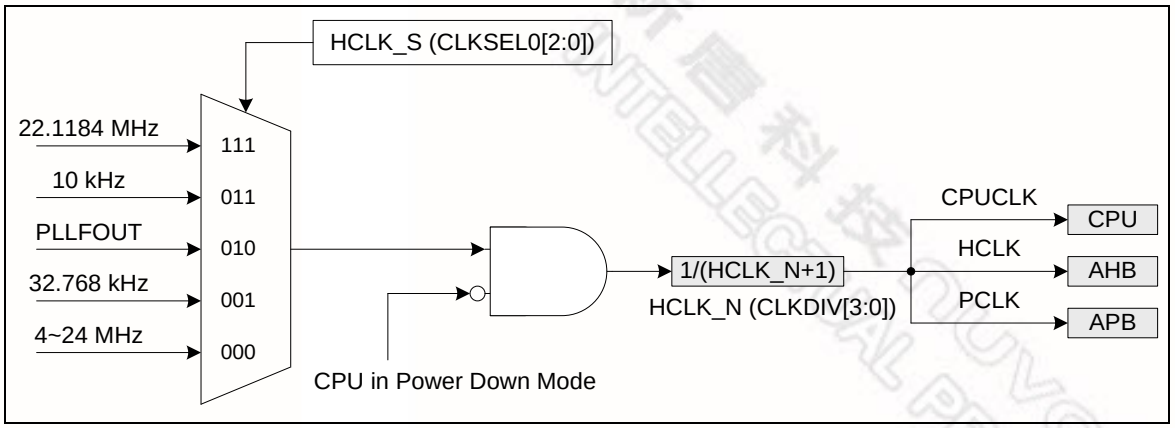

Figure 6-6 System Clock Block Diagram

The clock source of SysTick in Cortex™-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6-7.

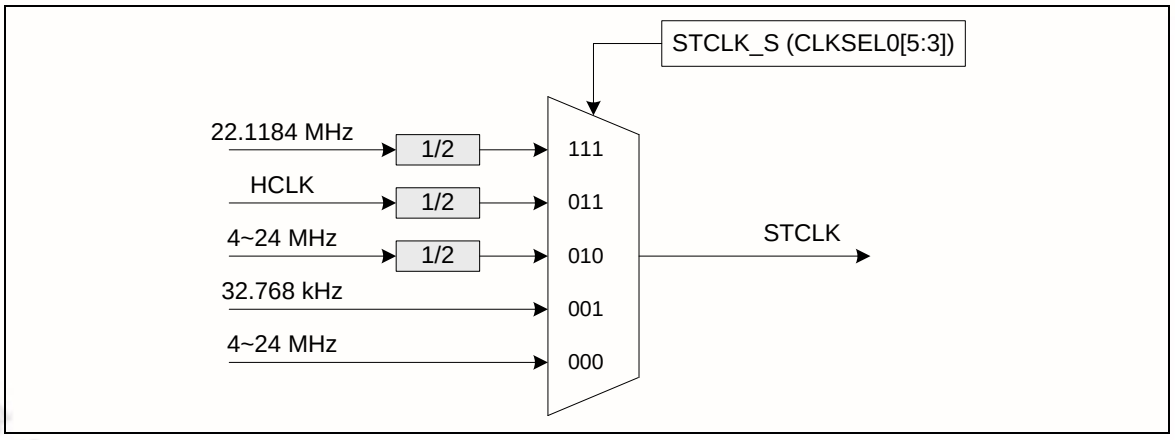

Figure 6-7 SysTick Clock Control Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro™ NUC230/240 series has 128/64/32K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro™ NUC230/240 series also provides additional Data Flash for user to store some application dependent data. For 128K bytes APROM device, the Data Flash is shared with original 128K program memory and its start address is configurable in CONFIG1. For 64K/32K bytes APROM device, the Data Flash is fixed at 4KB.

6.4.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access and runs up to 72MHz with one wait cycle for continuous address read.
- All embedded flash memory supports 512 bytes page erase
- 128/64/32 KB application program memory (APROM)
- 8KB In-System-Programming (ISP) loader program memory (LDROM)
- 4KB Data Flash for 64/32 KB APROM device
- Configurable Data Flash size for 128KB APROM device
- Configurable or fixed 4 KB Data Flash with 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.9 PWM Generator and Capture Timer (PWM)

6.9.1 Overview

The NuMicro™ NUC230/240 series has 2 sets of PWM group supporting a total of 4 sets of PWM generators that can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide eight independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DZEN01 (PCR[4]) is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively. Refer to **錯誤! 找不到參照來源。** and **錯誤! 找不到參照來源。** for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0 (CCR0[1]) (Rising latch Interrupt enable) and CFL_IE0 (CCR0[2]) (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CRL_IE1 (CCR0[17]) and CFL_IE1 (CCR0[18]). And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For

6.16 I²C Serial Interface Controller (I²C)

6.16.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.16.2 Features

The I²C bus uses two wires (I2Cn_SDA and I2Cn_SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C serial interface controller
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function

6.17 Serial Peripheral Interface (SPI)

6.17.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro™ NUC230/240 series contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a master or a slave device.

The SPI controller supports the variable bus clock function for special applications and 2-bit Transfer mode to connect 2 off-chip slave devices at the same time. This controller also supports the PDMA function to access the data buffer and also supports Dual I/O Transfer mode.

6.20 Controller Area Network (CAN)

6.20.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface (Refer 錯誤! 找不到參照來源。). The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.20.2 Features

- Supports CAN protocol version 2.0 part A and B.
- Bit rates up to 1 MBit/s.
- 32 Message Objects.
- Each Message Object has its own identifier mask.
- Programmable FIFO mode (concatenation of Message Objects).
- Maskable interrupt.
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications.
- Programmable loop-back mode for self-test operation.
- 16-bit module interfaces to the AMBA APB bus.
- Supports wake-up function

6.21 Analog-to-Digital Converter (ADC)

6.21.1 Overview

The NuMicro™ NUC230/240 series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM Center-aligned trigger and external STADC pin.

6.21.2 Features

- Analog input voltage range: 0~VREF
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels

8.4.8.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V_{DD33}	LDO Output Voltage		3.0	3.3	3.6	V
C_{bp}	External Bypass Capacitor			1.0	-	uF

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		10000			cycles[1]
T_{RET}	Data Retention	At 25℃	100			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			40		μs
I_{DD1}	Read Current		-	0.15	0.5	mA/MHz
I_{DD2}	Program/Erase Current				7	mA

1. Number of program/erase cycles.
2. V_{DD} is source from chip LDO output voltage.

This table is guaranteed by design, not test in production.