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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	49
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc230se3ae



1 GENERAL DESCRIPTION

The NuMicro™ NUC230/240 series 32-bit microcontrollers are embedded with the ARM® Cortex™-M0 core with a cost equivalent to traditional 8-bit MCU for industrial control and applications requiring rich communication interfaces. The NuMicro™ NUC230/240 series includes NUC230 and NUC240 product lines.

The NuMicro™ NUC230 CAN Line is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I²C, I²S, PWM Timer, GPIO, LIN, CAN, PS/2, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

The NuMicro™ NUC240 Connectivity Line with USB 2.0 full-speed and CAN functions is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I²C, I²S, PWM Timer, GPIO, LIN, CAN, PS/2, USB 2.0 FS Device, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I ² C	USB	LIN	CAN	PS/2	I ² S	SC
NUC230	●	●	●		●	●	●	●	●
NUC240	●	●	●	●	●	●	●	●	●

Table 1-1 NuMicro™ NUC230/240 Series Connectivity Support Table



- Each channel with individual result register
- Scan on enabled channels
- Threshold voltage detection
- Conversion started by software programming, external input or PWM Center-aligned trigger
- Supports PDMA mode
- Analog Comparator
 - Up to two analog comparators
 - External input or internal Band-gap voltage selectable at negative node
 - Interrupt when compare result change
 - Supports Power-down wake-up
- EBI (External bus interface)
 - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
 - Supports 8-/16-bit data width
 - Supports byte write in 16-bit data width mode
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- One built-in temperature sensor with 1°C resolution
- Brown-out Detector
 - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
 - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
 - Threshold voltage level: 2.0 V
- Operating Temperature: -40°C ~ 105°C
- Packages:
 - All Green package (RoHS)
 - LQFP 100-pin / 64-pin / 48-pin

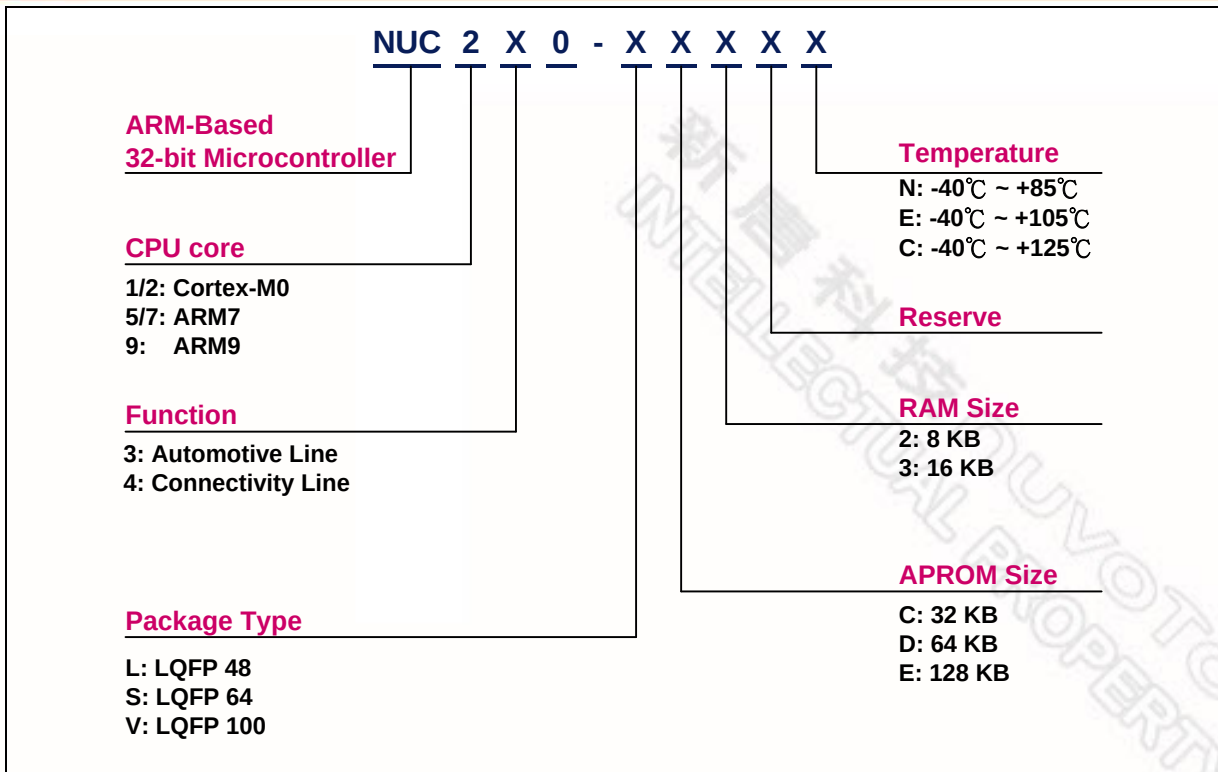


Figure 4-1 NuMicro™ NUC230/240 Series Selection Code



4.2 Pin Configuration

4.2.1 NuMicro™ NUC230 Pin Diagram

4.2.1.1 NuMicro™ NUC230VxxAE LQFP 100 pin

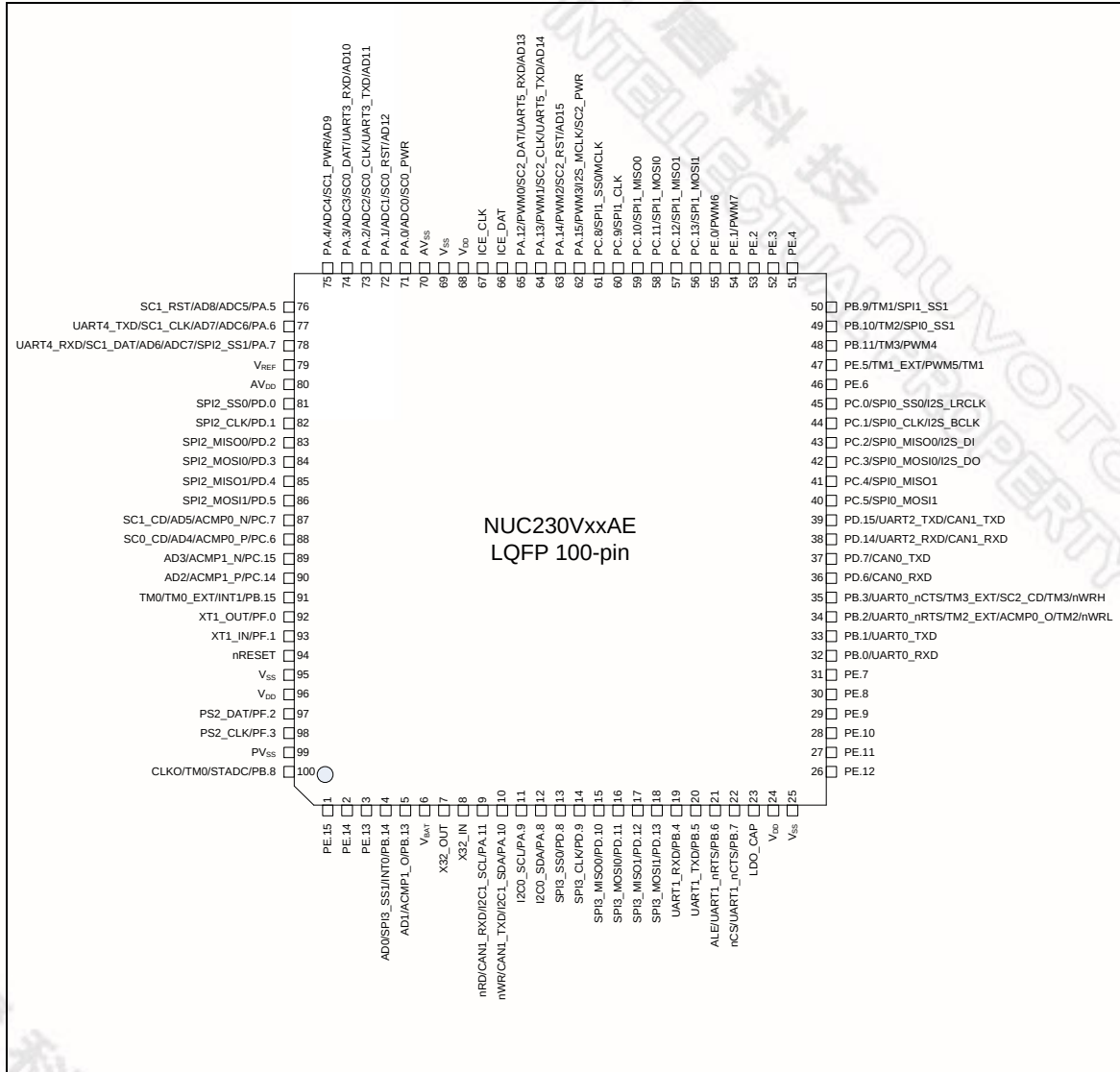


Figure 4-2 NuMicro™ NUC230VxxAE LQFP 100-pin Diagram

4.2.2.2 NuMicro™ NUC240SxxAE LQFP 64 pin

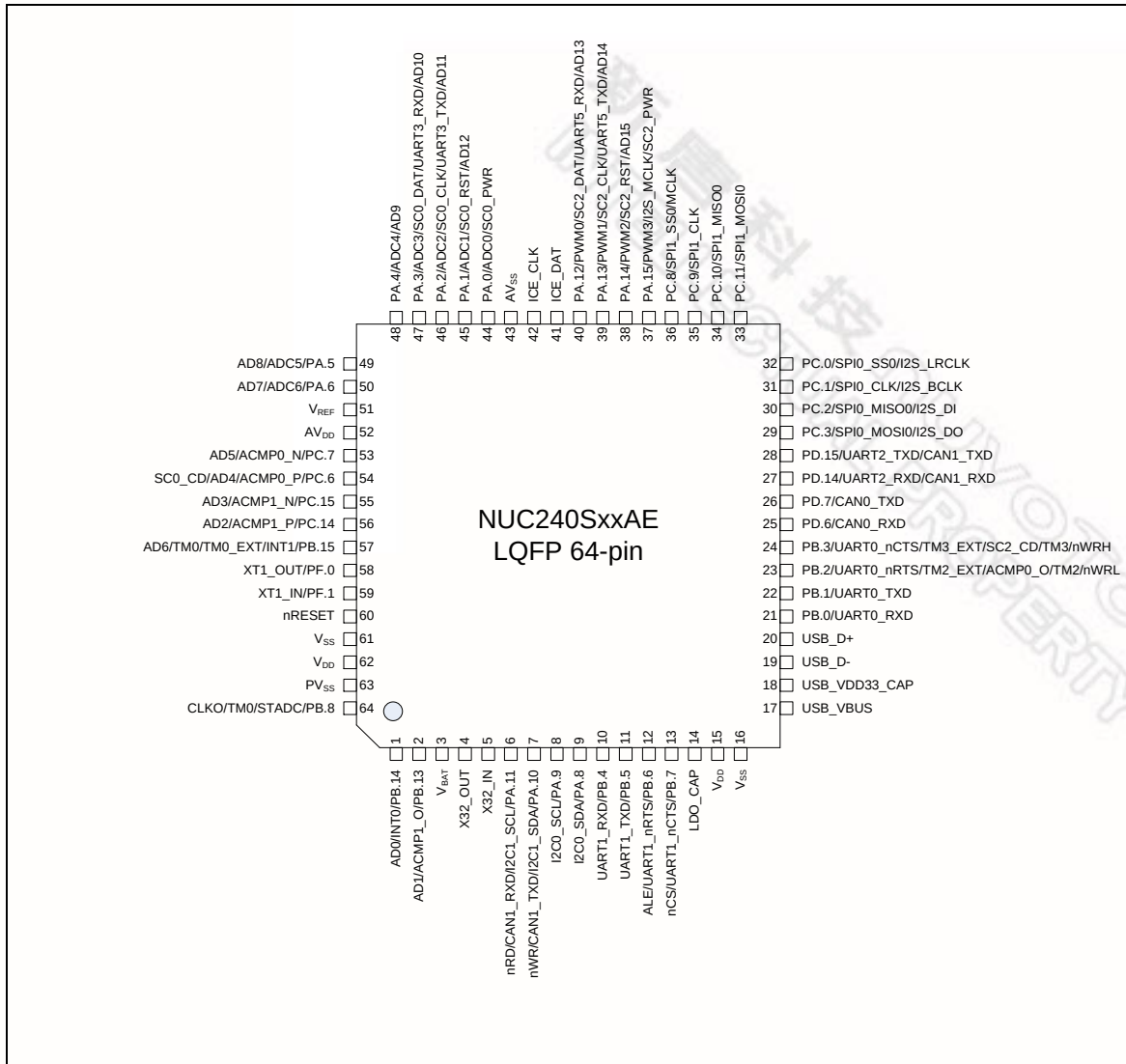


Figure 4-6 NuMicro™ NUC240SxxAE LQFP 64-pin Diagram



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SPI0_SS0	I/O	1 st SPI0 slave select pin.
			I2S_LRCLK	I/O	I ² S left right channel clock.
46			PE.6	I/O	General purpose digital I/O pin.
47	29		PE.5	I/O	General purpose digital I/O pin.
			PWM5	I/O	PWM5 output/Capture input.
			TM1_EXT	I	Timer1 external capture input pin.
			TM1	O	Timer1 toggle output pin.
48	30		PB.11	I/O	General purpose digital I/O pin.
			TM3	I/O	Timer3 event counter input / toggle output.
			PWM4	I/O	PWM4 output/Capture input.
49	31		PB.10	I/O	General purpose digital I/O pin.
			TM2	I/O	Timer2 event counter input / toggle output.
			SPI0_SS1	I/O	2 nd SPI0 slave select pin.
50	32		PB.9	I/O	General purpose digital I/O pin.
			TM1	I/O	Timer1 event counter input / toggle output.
			SPI1_SS1	I/O	2 nd SPI1 slave select pin.
51			PE.4	I/O	General purpose digital I/O pin.
52			PE.3	I/O	General purpose digital I/O pin.
53			PE.2	I/O	General purpose digital I/O pin.
54			PE.1	I/O	General purpose digital I/O pin.
			PWM7	I/O	PWM7 output/Capture input.
55			PE.0	I/O	General purpose digital I/O pin.
			PWM6	I/O	PWM6 output/Capture input.
56			PC.13	I/O	General purpose digital I/O pin.
			SPI1_MOSI1	I/O	2 nd SPI1 MOSI (Master Out, Slave In) pin.
57			PC.12	I/O	General purpose digital I/O pin.
			SPI1_MISO1	I/O	2 nd SPI1 MISO (Master In, Slave Out) pin.
58	33		PC.11	I/O	General purpose digital I/O pin.
			SPI1_MOSI0	I/O	1 st SPI1 MOSI (Master Out, Slave In) pin.
59	34		PC.10	I/O	General purpose digital I/O pin.
			SPI1_MISO0	I/O	1 st SPI1 MISO (Master In, Slave Out) pin.
60	35		PC.9	I/O	General purpose digital I/O pin.



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SPI1_CLK	I/O	SPI1 serial clock pin.
61	36		PC.8	I/O	General purpose digital I/O pin.
			MCLK	O	EBI clock output
			SPI1_SS0	I/O	1 st SPI1 slave select pin.
62	37	25	PA.15	I/O	General purpose digital I/O pin.
			PWM3	I/O	PWM output/Capture input.
			I2S_MCLK	O	I ² S master clock output pin.
			SC2_PWR	O	SmartCard2 power pin.
63	38	26	PA.14	I/O	General purpose digital I/O pin.
			PWM2	I/O	PWM2 output/Capture input.
			SC2_RST	O	SmartCard2 reset pin.
			AD15	I/O	EBI Address/Data bus bit15
64	39	27	PA.13	I/O	General purpose digital I/O pin.
			PWM1	I/O	PWM1 output/Capture input.
			SC2_CLK	O	SmartCard2 clock pin.
			UART5_TXD	O	Data transmitter output pin for UART5.
			AD14	I/O	EBI Address/Data bus bit14
65	40	28	PA.12	I/O	General purpose digital I/O pin.
			PWM0	I/O	PWM0 output/Capture input.
			SC2_DAT	O	SmartCard2 data pin.
			UART5_RXD	I	Data receiver input pin for UART5.
			AD13	I/O	EBI Address/Data bus bit13
66	41	29	ICE_DAT	I/O	Serial wire debugger data pin.
67	42	30	ICE_CLK	I	Serial wire debugger clock pin.
68			V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V _{SS}	P	Ground pin for digital circuit.
70	43	31	AV _{SS}	AP	Ground pin for analog circuit.
71	44	32	PA.0	I/O	General purpose digital I/O pin.
			ADC0	AI	ADC0 analog input.
			SC0_PWR	O	SmartCard0 power pin.
72	45	33	PA.1	I/O	General purpose digital I/O pin.
			ADC1	AI	ADC1 analog input.



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
79	51	39	V _{REF}	AP	Voltage reference input for ADC.
80	52	40	AV _{DD}	AP	Power supply for internal analog circuit.
81			PD.0	I/O	General purpose digital I/O pin.
			SPI2_SS0	I/O	1 st SPI2 slave select pin.
82			PD.1	I/O	General purpose digital I/O pin.
			SPI2_CLK	I/O	SPI2 serial clock pin.
83			PD.2	I/O	General purpose digital I/O pin.
			SPI2_MISO0	I/O	1 st SPI2 MISO (Master In, Slave Out) pin.
84			PD.3	I/O	General purpose digital I/O pin.
			SPI2_MOSI0	I/O	1 st SPI2 MOSI (Master Out, Slave In) pin.
85			PD.4	I/O	General purpose digital I/O pin.
			SPI2_MISO1	I/O	2 nd SPI2 MISO (Master In, Slave Out) pin.
86			PD.5	I/O	General purpose digital I/O pin.
			SPI2_MOSI1	I/O	2 nd SPI2 MOSI (Master Out, Slave In) pin.
87	53	41	PC.7	I/O	General purpose digital I/O pin.
			ACMP0_N	AI	Comparator0 negative input pin.
			AD5	I/O	EBI Address/Data bus bit5
			SC1_CD	I	SmartCard1 card detect pin.
88	54	42	PC.6	I/O	General purpose digital I/O pin.
			ACMP0_P	AI	Comparator0 positive input pin.
			SC0_CD	I	SmartCard0 card detect pin.
			AD4	I/O	EBI Address/Data bus bit4
89	55		PC.15	I/O	General purpose digital I/O pin.
			AD3	I/O	EBI Address/Data bus bit3
			ACMP1_N	AI	Comparator1 negative input pin.
90	56		PC.14	I/O	General purpose digital I/O pin.
			AD2	I/O	EBI Address/Data bus bit2
			ACMP1_P	AI	Comparator1 positive input pin.
91	57	43	PB.15	I/O	General purpose digital I/O pin.
			INT1	I	External interrupt1 input pin.
			TM0_EXT	I	Timer 0 external capture input pin.
			TM0	O	Timer0 toggle output pin.
			AD6	I/O	EBI Address/Data bus bit6



6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Power-on Reset
- Low level on the nRESET pin
- Watchdog Time-out Reset
- Low Voltage Reset
- Brown-out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-on Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-on Reset is external crystal circuit and BS(ISPCON[1]) bit. System Reset does not reset external crystal circuit and BS(ISPCON[1]) bit, but Power-on Reset does.



0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4018_0000 – 0x4018_3FFF	CAN0_BA	CAN0 Bus Control Registers
0x4018_4000 – 0x4018_7FFF	CAN1_BA	CAN1 Bus Control Registers
0x4019_0000 – 0x4019_3FFF	SC0_BA	SC0 Control Registers
0x4019_4000 – 0x4019_7FFF	SC1_BA	SC1 Control Registers
0x4019_8000 – 0x4019_BFFF	SC2_BA	SC2 Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I ² S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6-1 Address Space Assignments for On-Chip Controllers



6.2.5 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.



6.3.3 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
 - 10 kHz internal low speed RC oscillator clock
 - 32.768 kHz external low speed crystal oscillator clock
- RTC/WDT/Timer/PWM Peripherals Clock (when 32.768 kHz external low speed crystal oscillator or 10 kHz internal low speed RC oscillator is adopted as clock source)



6.5 External Bus Interface (EBI)

6.5.1 Overview

The NuMicro™ NUC100 series LQFP-64 and LQFP-100 package equips an external bus interface (EBI) for access external device.

To save the connections between external device and this chip, EBI supports address bus and data bus multiplex mode. And, address latch enable (ALE) signal is used to differentiate the address and data cycle.

6.5.2 Features

External Bus Interface has the following functions:

- Supports external devices with max. 64 KB size (8-bit data width)/128 KB (16-bit data width)
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports 8-bit or 16-bit data width
- Supports variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD)
- Supports address bus and data bus multiplex mode to save the address pins
- Supports configurable idle cycle for different access condition: Write command finish (W2X), Read-to-Read (R2R)



6.6 General Purpose I/O (GPIO)

6.6.1 Overview

The NuMicro™ NUC230/240 series has up to 84 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 84 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B/C/D/E port has the maximum of 16 pins and GPIOF port has the maximum of 4 pins. Each of the 84 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 K Ω for V_{DD} is from 5.0 V to 2.5 V.

6.6.2 Features

- Four I/O modes:
 - Quasi-bidirectional
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
 - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
 - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function.

6.7 PDMA Controller (PDMA)

6.7.1 Overview

The NuMicro™ NUC230/240 series DMA contains nine-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA that transfers data to and from memory or transfer data to and from APB devices. For PDMA channel (PDMA CH0~CH8), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. Software can stop the PDMA operation by disable PDMA PDMACEN (PDMA_CSRx[0]). The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

The DMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU PIO mode and DMA transfer mode.



6.13 UART Interface Controller (UART)

6.13.1 Overview

The NuMicro NUC230/240 series provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART. Besides, only UART0 and UART1 support the flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave function and RS-485 function mode. Each UART Controller channel supports seven types of interrupts.

6.13.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 64/16/16 bytes (UART0/UART1/UART2) entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0 and UART1 support)
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0 and UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- UART0/UART1 can through DMA channels to receive/transmit data
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
 - Programmable data bit length, 5-, 6-, 7-, 8-bit character
 - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
 - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
 - Supports 3-/16-bit duration for normal mode
- LIN function mode
 - Supports LIN master/slave mode
 - Supports programmable break generation function for transmitter
 - Supports break detect function for receiver
- RS-485 function mode.
 - Supports RS-485 9-bit mode
 - Supports hardware or software direct enable control provided by RTS pin (UART0 and UART1 support)



6.19 USB Device Controller (USB_D)

6.19.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (USB_BUFSEGx)”.

There are 8 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, and BUS events. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If DRVSE0 (USB_DRVSE0[0]) is set to 1, the USB controller will force the output of USB_D+ and USB_D- to level low. After DRVSE0 bit is cleared to 0, host will enumerate the USB device again.

Please refer to *Universal Serial Bus Specification Revision 1.1* for details.

6.19.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Provides 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provides remote wake-up capability



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	-0.3	+7.0	V
Battery Power Supply	V_{BAT}	+2.4	+5.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.



PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Normal Run Mode at 32.768 kHz while(1){ executed from flash $V_{LDO} = 1.8\text{ V}$	I_{DD17}		141		μA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital module
						5.5V	32.768	X	X	V
	I_{DD18}		129		μA	5.5V	32.768	X	X	X
	I_{DD19}		138		μA	3.3V	32.768	X	X	V
	I_{DD20}		125		μA	3.3V	32.768	X	X	X
Operating Current Normal Run Mode at 10 kHz while(1){ executed from flash $V_{LDO} = 1.8\text{ V}$	I_{DD21}		125		μA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{DD22}		120		μA	5.5V	X	10	X	X
	I_{DD23}		125		μA	3.3V	X	10	X	V
	I_{DD24}		120		μA	3.3V	X	10	X	X
Operating Current Idle Mode at 72 MHz $V_{LDO} = 1.8\text{ V}$	I_{IDLE1}		42		mA	V_{DD}	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{IDLE2}		11		mA	5.5V	12 MHz	X	V	X
	I_{IDLE3}		41		mA	3.3V	12 MHz	X	V	V
	I_{IDLE4}		9		mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 50 MHz $V_{LDO} = 1.8\text{ V}$	I_{IDLE5}		28		mA	5.5V	12 MHz	X	V	V
	I_{IDLE6}		10		mA	5.5V	12 MHz	X	V	X
	I_{IDLE7}		27		mA	3.3V	12 MHz	X	V	V
	I_{IDLE8}		9		mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 12 MHz $V_{LDO} = 1.8\text{ V}$	I_{IDLE9}		7.5		mA	5.5V	12 MHz	X	X	V
	I_{IDLE10}		2.4		mA	5.5V	12 MHz	X	X	X
	I_{IDLE11}		6.5		mA	3.3V	12 MHz	X	X	V
	I_{IDLE12}		1.5		mA	3.3V	12 MHz	X	X	X
Operating Current Idle Mode at 4 MHz $V_{LDO} = 1.8\text{ V}$	I_{IDLE13}		3.3		mA	5.5V	4 MHz	X	X	V
	I_{IDLE14}		1.7		mA	5.5V	4 MHz	X	X	X
	I_{IDLE15}		2.4		mA	3.3V	4 MHz	X	X	V
	I_{IDLE16}		0.8		mA	3.3V	4 MHz	X	X	X
Operating Current Idle Mode at 32.768 kHz $V_{LDO} = 1.8\text{ V}$	I_{IDLE17}		133		μA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital module
						5.5V	32.768	X	X	V
	I_{IDLE18}		120		μA	5.5V	32.768	X	X	X



8.4.3 Low Voltage Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Quiescent Current	$AV_{DD}=5.5\text{ V}$	-	1	5	μA
Operation Temperature	-	-40	25	105	$^{\circ}\text{C}$
Threshold Voltage	-	1.6	2.0	2.4	V
Hysteresis	-	0	0	0	V

8.4.4 Brown-out Detector Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Temperature	-	-40	25	105	$^{\circ}\text{C}$
Quiescent Current	$AV_{DD}=5.5\text{ V}$	-	-	125	μA
Brown-out Voltage	BOD_VL[1:0]=11	4.2	4.4	4.6	V
	BOD_VL [1:0]=10	3.5	3.7	3.9	V
	BOD_VL [1:0]=01	2.6	2.7	2.8	V
	BOD_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

8.4.5 Power-on Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Temperature	-	-40	25	105	$^{\circ}\text{C}$
Reset Voltage	V+	-	2	-	V
Quiescent Current	$V_{in} > \text{reset voltage}$	-	1	-	nA



8.4.8.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V _{DD33}	LDO Output Voltage		3.0	3.3	3.6	V
C _{bp}	External Bypass Capacitor			1.0	-	uF

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DD}	Supply Voltage		1.62	1.8	1.98	V ^[2]
N _{ENDUR}	Endurance		10000			cycles ^[1]
T _{RET}	Data Retention	At 25°C	100			year
T _{ERASE}	Page Erase Time			20		ms
T _{MER}	Mass Erase Time			40		ms
T _{PROG}	Program Time			40		μs
I _{DD1}	Read Current		-	0.15	0.5	mA/MHz
I _{DD2}	Program/Erase Current				7	mA

1. Number of program/erase cycles.
2. V_{DD} is source from chip LDO output voltage.

This table is guaranteed by design, not test in production.