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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex® -M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc240lc2ae

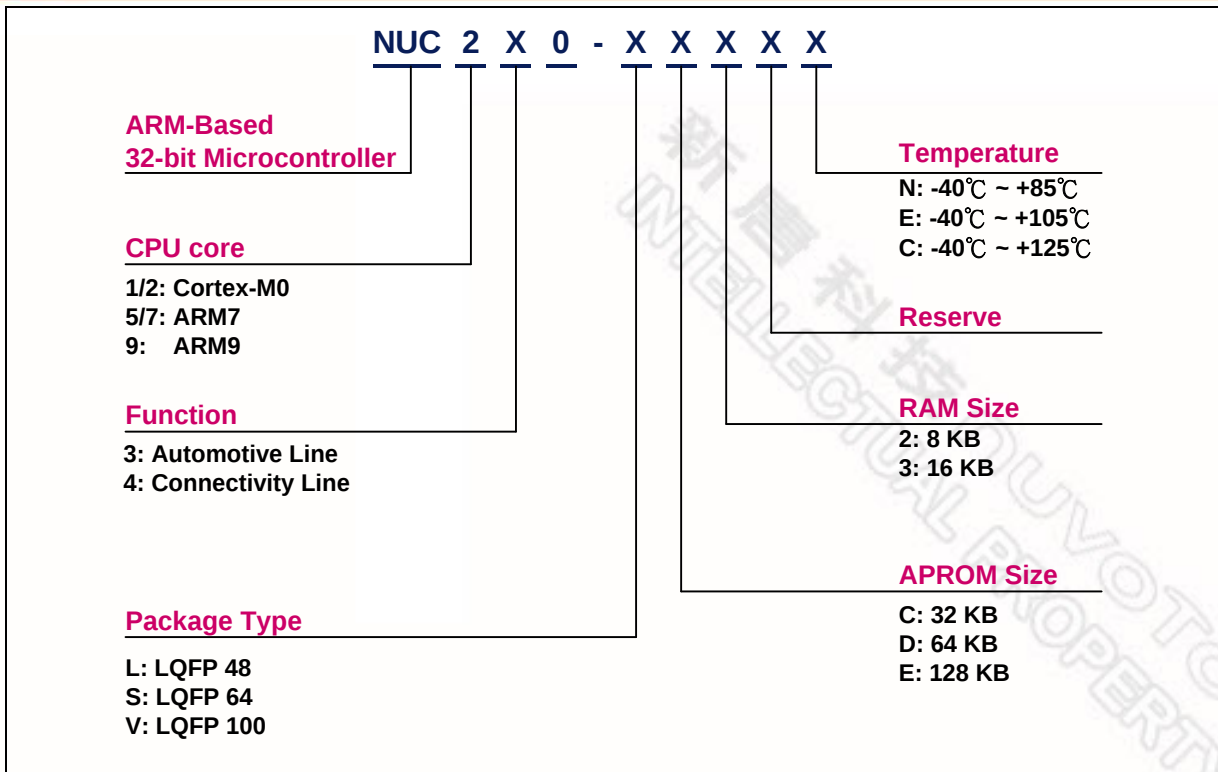


Figure 4-1 NuMicro™ NUC230/240 Series Selection Code



4.3 Pin Description

4.3.1 NuMicro™ NUC230 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	I/O	General purpose digital I/O pin.
2			PE.14	I/O	General purpose digital I/O pin.
3			PE.13	I/O	General purpose digital I/O pin.
4	1		PB.14	I/O	General purpose digital I/O pin.
			AD0	I/O	EBI Address/Data bus bit0
			INT0	I	External interrupt0 input pin.
			SPI3_SS1	I/O	2 nd SPI3 slave select pin.
5	2		PB.13	I/O	General purpose digital I/O pin.
			AD1	I/O	EBI Address/Data bus bit1
			ACMP1_O	O	Comparator1 output pin.
6	3	1	V _{BAT}	P	Power supply by batteries for RTC.
7	4	2	X32_OUT	O	External 32.768 kHz (low speed) crystal output pin.
8	5	3	X32_IN	I	External 32.768 kHz (low speed) crystal input pin.
9	6	4	PA.11	I/O	General purpose digital I/O pin.
			I2C1_SCL	I/O	I ² C1 clock pin.
			CAN1_RXD	I	Data receiver input pin for CAN1.
			nRD	O	EBI read enable output pin
10	7	5	PA.10	I/O	General purpose digital I/O pin.
			I2C1_SDA	I/O	I ² C1 data input/output pin.
			CAN1_TXD	O	Data transmitter output pin for CAN1.
			nWR	O	EBI write enable output pin
11	8	6	PA.9	I/O	General purpose digital I/O pin.
			I2C0_SCL	I/O	I ² C0 clock pin.
12	9	7	PA.8	I/O	General purpose digital I/O pin.
			I2C0_SDA	I/O	I ² C0 data input/output pin.
13			PD.8	I/O	General purpose digital I/O pin.
			SPI3_SS0	I/O	1 st SPI3 slave select pin.
14			PD.9	I/O	General purpose digital I/O pin.
			SPI3_CLK	I/O	SPI3 serial clock pin.
15			PD.10	I/O	General purpose digital I/O pin.



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			TM2_EXT	I	Timer2 external capture input pin.
			ACMP0_O	O	Comparator0 output pin.
			nWRL	O	EBI low byte write enable output pin
35	20	16	PB.3	I/O	General purpose digital I/O pin.
			UART0_nCTS	I	Clear to Send input pin for UART0.
			TM3_EXT	I	Timer3 external capture input pin.
			SC2_CD	I	SmartCard2 card detect pin.
			nWRH	O	EBI high byte write enable output pin
36	21	17	PD.6	I/O	General purpose digital I/O pin.
			CAN0_RXD	I	Data receiver input pin for CAN0.
37	22	18	PD.7	I/O	General purpose digital I/O pin.
			CAN0_TXD	O	Data transmitter output pin for CAN0.
38	23	19	PD.14	I/O	General purpose digital I/O pin.
			UART2_RXD	I	Data receiver input pin for UART2.
			CAN1_RXD	I	Data receiver input pin for CAN1.
39	24	20	PD.15	I/O	General purpose digital I/O pin.
			UART2_TXD	O	Data transmitter output pin for UART2.
			CAN1_TXD	O	Data transmitter output pin for CAN1.
40			PC.5	I/O	General purpose digital I/O pin.
			SPI0_MOSI1	I/O	2 nd SPI0 MOSI (Master Out, Slave In) pin.
41			PC.4	I/O	General purpose digital I/O pin.
			SPI0_MISO1	I/O	2 nd SPI0 MISO (Master In, Slave Out) pin.
42	25	21	PC.3	I/O	General purpose digital I/O pin.
			SPI0_MOSI0	I/O	1 st SPI0 MOSI (Master Out, Slave In) pin.
			I2S_DO	O	I ² S data output.
43	26	22	PC.2	I/O	General purpose digital I/O pin.
			SPI0_MISO0	I/O	1 st SPI0 MISO (Master In, Slave Out) pin.
			I2S_DI	I	I ² S data input.
44	27	23	PC.1	I/O	General purpose digital I/O pin.
			SPI0_CLK	I/O	SPI0 serial clock pin.
			I2S_BCLK	I/O	I ² S bit clock pin.
45	28	24	PC.0	I/O	General purpose digital I/O pin.



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
93	59	45	PF.1	I/O	General purpose digital I/O pin.
			XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
94	60	46	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V _{SS}	P	Ground pin for digital circuit.
96	62		V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	I/O	General purpose digital I/O pin.
			PS2_DAT	I/O	PS2 data pin.
98			PF.3	I/O	General purpose digital I/O pin.
			PS2_CLK	I/O	PS2 clock pin.
99	63	47	PV _{SS}	P	PLL ground.
100	64	48	PB.8	I/O	General purpose digital I/O pin.
			STADC	I	ADC external trigger input.
			TM0	I/O	Timer0 event counter input / toggle output.
			CLKO	O	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
45	32	24	PC.0	I/O	General purpose digital I/O pin.
			SPI0_SS0	I/O	1 st SPI0 slave select pin.
			I2S_LRCLK	I/O	I ² S left right channel clock.
46			PE.6	I/O	General purpose digital I/O pin.
47			PE.5	I/O	General purpose digital I/O pin.
			PWM5	I/O	PWM5 output/Capture input.
			TM1_EXT	I	Timer1 external capture input pin.
			TM1	O	Timer1 toggle output pin.
48			PB.11	I/O	General purpose digital I/O pin.
			TM3	I/O	Timer3 event counter input / toggle output.
			PWM4	I/O	PWM4 output/Capture input.
49			PB.10	I/O	General purpose digital I/O pin.
			TM2	I/O	Timer2 event counter input / toggle output.
			SPI0_SS1	I/O	2 nd SPI0 slave select pin.
50			PB.9	I/O	General purpose digital I/O pin.
			TM1	I/O	Timer1 event counter input / toggle output.
			SPI1_SS1	I/O	2 nd SPI1 slave select pin.
51			PE.4	I/O	General purpose digital I/O pin.
52			PE.3	I/O	General purpose digital I/O pin.
53			PE.2	I/O	General purpose digital I/O pin.
54			PE.1	I/O	General purpose digital I/O pin.
			PWM7	I/O	PWM7 output/Capture input.
55			PE.0	I/O	General purpose digital I/O pin.
			PWM6	I/O	PWM6 output/Capture input.
56			PC.13	I/O	General purpose digital I/O pin.
			SPI1_MOSI1	I/O	2 nd SPI1MOSI (Master Out, Slave In) pin.
57			PC.12	I/O	General purpose digital I/O pin.
			SPI1_MISO1	I/O	2 nd SPI1 MISO (Master In, Slave Out) pin.
58	33		PC.11	I/O	General purpose digital I/O pin.
			SPI1_MOSI0	I/O	1 st SPI1 MOSI (Master Out, Slave In) pin.
59	34		PC.10	I/O	General purpose digital I/O pin.
			SPI1_MISO0	I/O	1 st SPI1 MISO (Master In, Slave Out) pin.

5 BLOCK DIAGRAM

5.1 NuMicro™ NUC230 Block Diagram

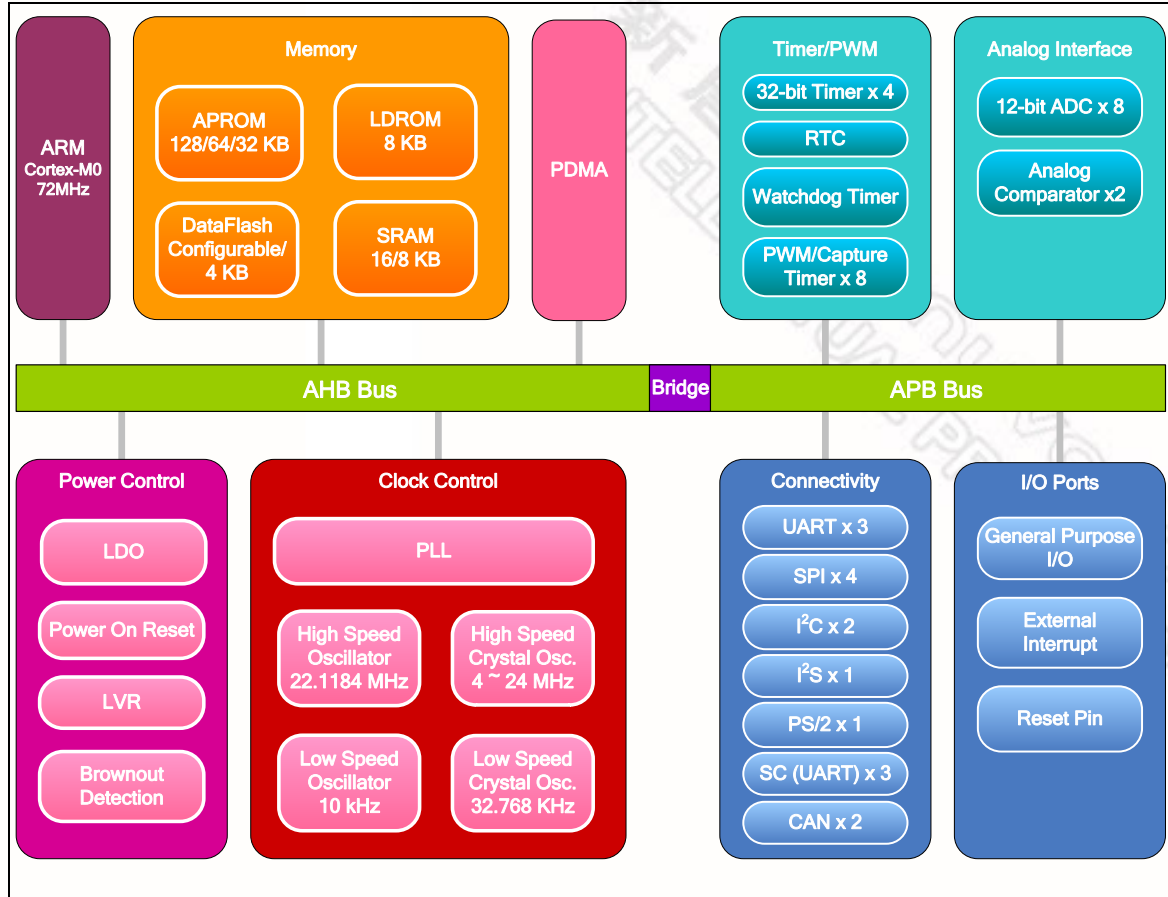


Figure 5-1 NuMicro™ NUC230 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processor. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

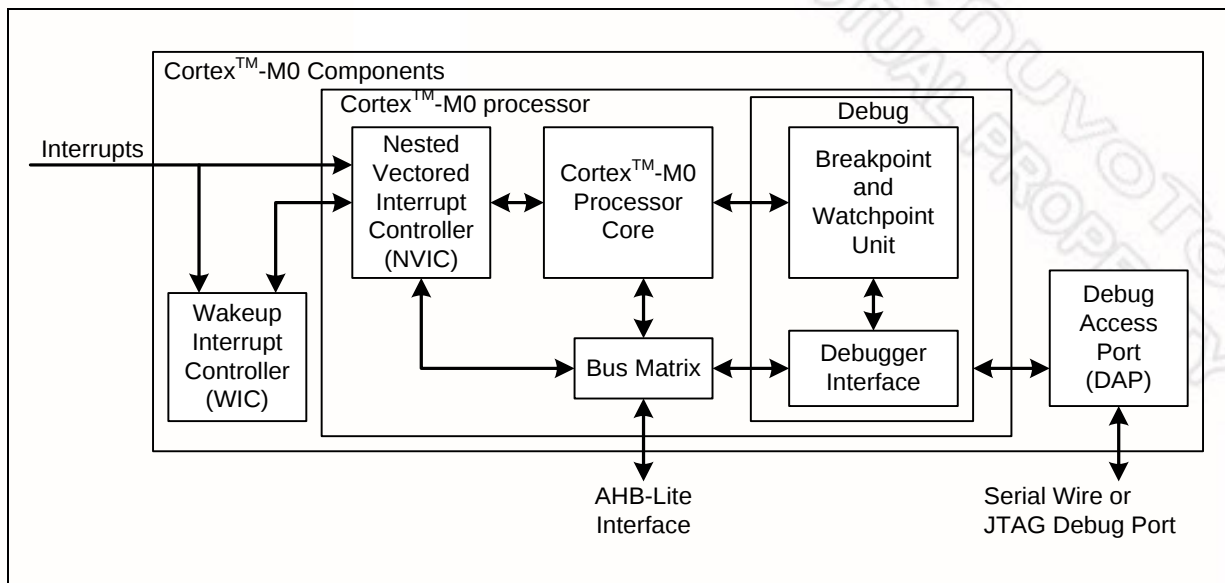


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
 - ARMv6-M Thumb® instruction set
 - Thumb-2 technology
 - ARMv6-M compliant 24-bit SysTick timer
 - A 32-bit hardware multiplier
 - System interface supported with little-endian data accesses
 - Ability to have deterministic, fixed-latency, interrupt handling
 - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
 - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
 - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature



6.2.6.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro™ NUC230/240 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6-2 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description
1 ~ 15	-	-	-	System exceptions
16	0	BOD_INT	Brown-out	Brown-out low voltage detected interrupt
17	1	WDT_INT	WDT	Watchdog Timer interrupt
18	2	EINT0	GPIO	External signal interrupt from PB.14 pin
19	3	EINT1	GPIO	External signal interrupt from PB.15 pin
20	4	GPAB_INT	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDEF_INT	GPIO	External interrupt from PC[15:0]/PD[15:0]/PE[15:0]/PF[3:0]
22	6	PWMA_INT	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	PWMB_INT	PWM4~7	PWM4, PWM5, PWM6 and PWM7 interrupt
24	8	TMR0_INT	TMR0	Timer 0 interrupt
25	9	TMR1_INT	TMR1	Timer 1 interrupt
26	10	TMR2_INT	TMR2	Timer 2 interrupt
27	11	TMR3_INT	TMR3	Timer 3 interrupt
28	12	UART02_INT	UART0/2	UART0 and UART2 interrupt
29	13	UART1_INT	UART1	UART1 interrupt
30	14	SPI0_INT	SPI0	SPI0 interrupt

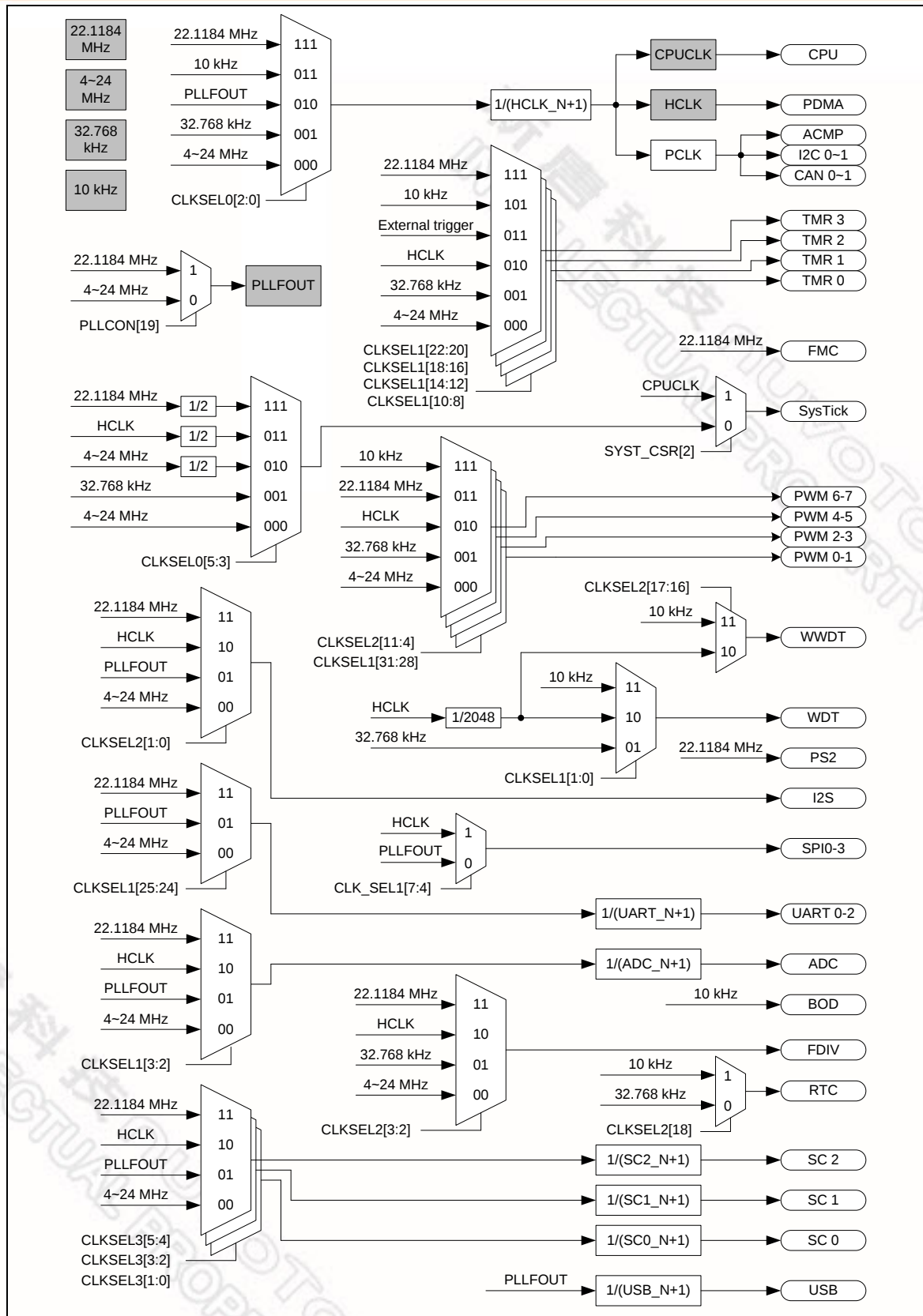


Figure 6-5 Clock Generator Global View Diagram

6.3.2 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-6.

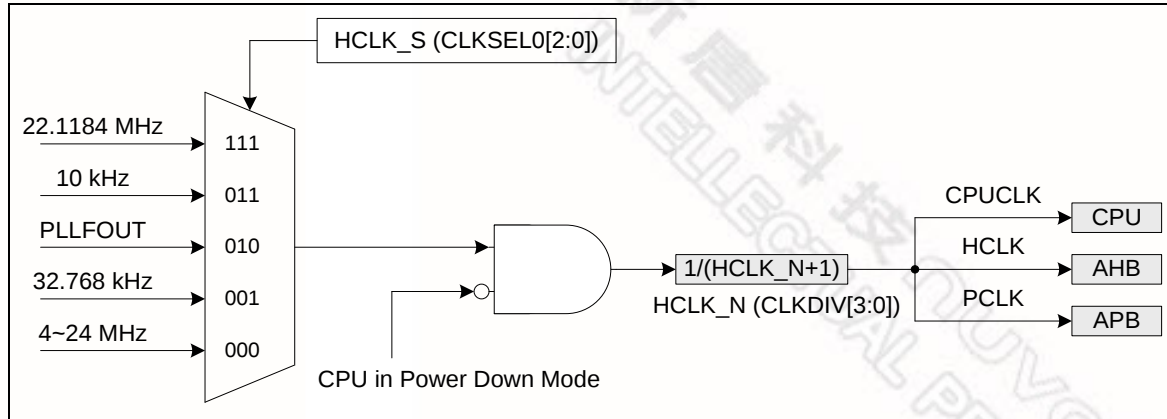


Figure 6-6 System Clock Block Diagram

The clock source of SysTick in Cortex™-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6-7.

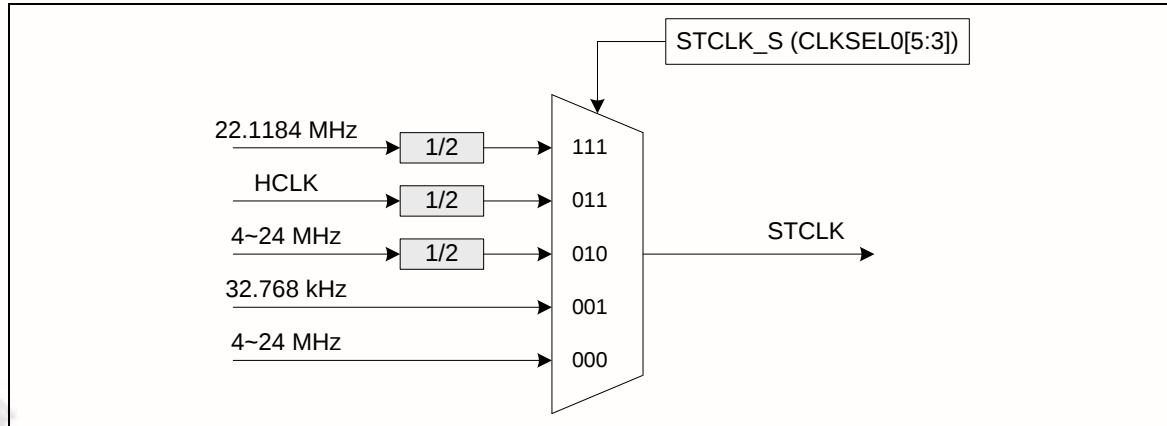


Figure 6-7 SysTick Clock Control Block Diagram



6.3.3 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
 - 10 kHz internal low speed RC oscillator clock
 - 32.768 kHz external low speed crystal oscillator clock
- RTC/WDT/Timer/PWM Peripherals Clock (when 32.768 kHz external low speed crystal oscillator or 10 kHz internal low speed RC oscillator is adopted as clock source)

6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1 (FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

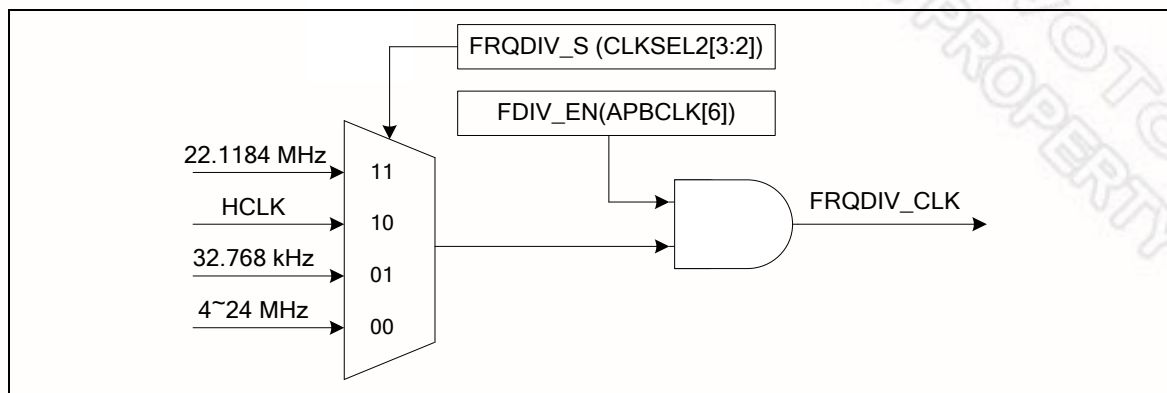


Figure 6-8 Clock Source of Frequency Divider

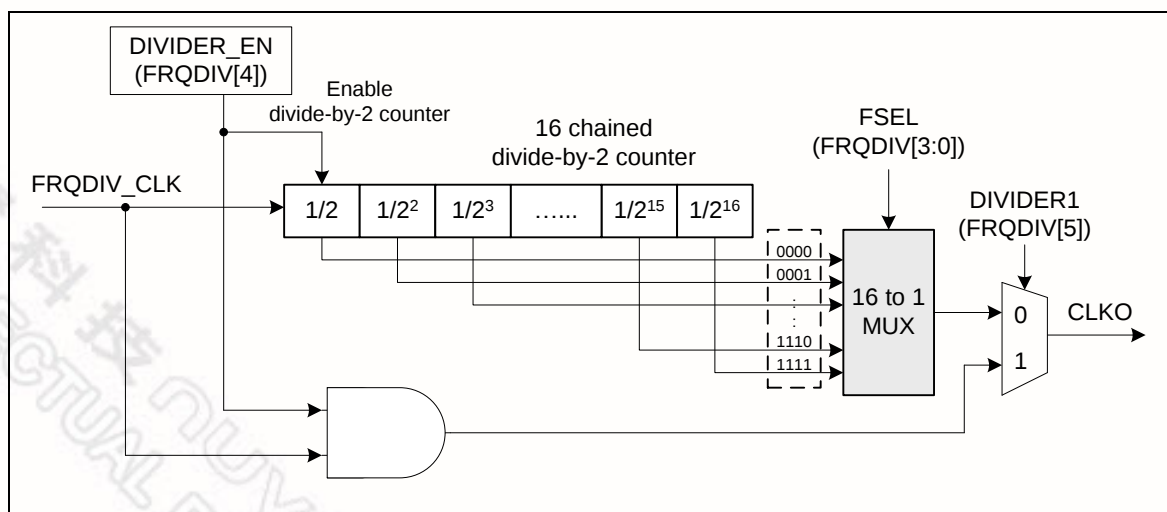


Figure 6-9 Frequency Divider Block Diagram

6.7.2 Features

- Supports nine PDMA channels and one CRC channel. Each PDMA channel can support a unidirectional transfer
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Hardware round robin priority scheme. DMA channel 0 has the highest priority and channel 8 has the lowest priority
- PDMA operation
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address direction: increment, fixed.
- Cyclic Redundancy Check (CRC)
 - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
 - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
 - CRC-8: $X^8 + X^2 + X + 1$
 - CRC-16: $X^{16} + X^{15} + X^2 + 1$
 - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
 - Supports programmable CRC seed value.
 - Supports programmable order reverse setting for input data and CRC checksum.
 - Supports programmable 1's complement setting for input data and CRC checksum.
 - Supports CPU PIO mode or DMA transfer mode.
 - Supports the follows write data length in CPU PIO mode
 - 8-bit write mode (byte): 1-AHB clock cycle operation.
 - 16-bit write mode (half-word): 2-AHB clock cycle operation.
 - 32-bit write mode (word): 4-AHB clock cycle operation.
 - Supports byte alignment transfer data length and word alignment transfer source address in CRC DMA mode.

6.8 Timer Controller (TIMER)

6.8.1 Overview

The timer controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.



6.14 Smart Card Host Interface (SC)

6.14.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal. It also support UART mode for full duplex asynchronous communications.

6.14.2 Features

- Supports up to three ISO7816-3 ports (SC0, SC1 and SC2)
 - ISO7816-3 T=0, T=1 compliant
 - EMV2000 compliant
 - Separates receive/ transmit 4 byte entry FIFO for data payloads.
 - Programmable transmission clock frequency.
 - Programmable receiver buffer trigger level.
 - Programmable guard time selection (11 ETU ~ 267 ETU).
 - A 24-bit and two 8-bit times for Answer to Request (ATR) and waiting times processing.
 - Supports auto inverse convention function.
 - Supports transmitter and receiver error retry and error number limiting function.
 - Supports hardware activation sequence, hardware warm reset sequence and hardware deactivation sequence process.
 - Supports hardware auto deactivation sequence when detecting the card removal.
- Supports up to three UART ports (UART3, UART4, UART5)
 - Full duplex, asynchronous communications.
 - Programmable data bit length, 5-, 6-, 7-, 8-bit character.
 - Separates receiving / transmitting 4 bytes entry FIFO for data payloads.
 - Supports programmable baud rate generator for each channel.
 - Supports programmable receiver buffer trigger level.
 - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SCx_EGTR [EGT] register.
 - Programmable even, odd or no parity bit generation and detection.
 - Programmable stop bit, 1 or 2 stop bit generation.



6.15 PS/2 Device Controller (PS2D)

6.15.1 Overview

PS/2 device controller provides a basic timing control for PS/2 communication. All communication between the device and the host is managed through the PS2_CLK and PS2_DATA pins. Unlike PS/2 keyboard or mouse device controller, the receive/transmit code needs to be translated as meaningful code by firmware. The device controller generates the PS2_CLK signal after receiving a "Request to Send" state, but host has ultimate control over communication. Data of PS2_DATA line sent from the host to the device is read on the rising edge and sent from the device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. Software can select 1 to 16 bytes for a continuous transmission.

6.15.2 Features

- Host communication inhibit and "Request-to-Send" state detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- Software override bus



6.17.2 Features

- Up to four sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32 bits
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Two slave select lines in Master mode
- Supports the Byte Reorder function
- Supports Byte or Word Suspend mode
- Variable output bus clock frequency in Master mode
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface

6.18 I²S Controller (I²S)

6.18.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 8-word depth FIFO for reading path and writing path respectively and is capable of handling 8-, 16-, 24- and 32-bit word sizes. PDMA controller handles the data movement between FIFO and memory.

6.18.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports monaural and stereo audio data
- Supports I²S and MSB justified data format
- Provides two 8-word FIFO data buffers, one for transmitting and the other for receiving
- Supports PDMA transfer



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	-0.3	+7.0	V
Battery Power Supply	V_{BAT}	+2.4	+5.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.



8.2 DC Electrical Characteristics

($V_{DD}-V_{SS}=5.5\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{OSC} = 50\text{ MHz}$ unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation Voltage	V_{DD}	2.5		5.5	V	$V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$ up to 72 MHz				
Power Ground	V_{SS} AV_{SS}	-0.3			V					
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	$V_{DD} > 2.5\text{ V}$				
Band-gap Voltage	V_{BG}	1.22	1.25	1.28	V	$V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$, $T_A = 25^\circ\text{C}$				
Analog Operating Voltage	AV_{DD}		V_{DD}		V	When system used analog function, please refer to NUC230/240 Series Technical Reference Manual chapter 6.5 for corresponding analog operating voltage				
RTC Operating Voltage	V_{BAT}	2.5		5.5	V					
Operating Current Normal Run Mode at 72 MHz while(1){ executed from flash $V_{LDO}=1.8\text{ V}$	I_{DD1}		50		mA	V_{DD}	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{DD2}		20		mA	5.5V	12 MHz	X	V	X
	I_{DD3}		48		mA	3.3V	12 MHz	X	V	V
Operating Current Normal Run Mode at 50 MHz while(1){ executed from flash $V_{LDO}=1.8\text{ V}$	I_{DD4}		18		mA	3.3V	12 MHz	X	V	X
	I_{DD5}		34		mA	5.5V	12 MHz	X	V	V
	I_{DD6}		15		mA	5.5V	12 MHz	X	V	X
	I_{DD7}		32		mA	3.3V	12 MHz	X	V	V
Operating Current Normal Run Mode at 12 MHz while(1){ executed from flash $V_{LDO}=1.8\text{ V}$	I_{DD8}		14		mA	3.3V	12 MHz	X	V	X
	I_{DD9}		8.5		mA	5.5V	12 MHz	X	X	V
	I_{DD10}		3.6		mA	5.5V	12 MHz	X	X	X
	I_{DD11}		7.5		mA	3.3V	12 MHz	X	X	V
Operating Current Normal Run Mode at 4 MHz while(1){ executed from flash $V_{LDO}=1.8\text{ V}$	I_{DD12}		2.6		mA	3.3V	12 MHz	X	X	X
	I_{DD13}		3.6		mA	5.5V	4 MHz	X	X	V
	I_{DD14}		2		mA	5.5V	4 MHz	X	X	X
	I_{DD15}		2.8		mA	3.3V	4 MHz	X	X	V
	I_{DD16}		1.2		mA	3.3V	4 MHz	X	X	X



PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Hysteresis voltage of PA, PB, PC, PD, PE, PF (Schmitt input)	V_{HY}		$0.2V_{DD}$		V	
Input Low Voltage XT1_IN ^[2]	V_{IL3}	0	-	0.8	V	$V_{DD} = 4.5V$
		0	-	0.4		$V_{DD} = 3.0V$
Input High Voltage XT1_IN ^[2]	V_{IH3}	3.5	-	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
		2.4	-	$V_{DD} + 0.2$		$V_{DD} = 3.0V$
Input Low Voltage X32I ^[2]	V_{IL4}	0	-	0.4	v	
Input High Voltage X32I ^[2]	V_{IH4}	1.2		1.8	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	$0.2V_{DD} - 0.2$	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	$0.7V_{DD}$	-	$V_{DD} + 0.5$	V	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	$V_{DD} = 4.5V, V_S = 2.4V$
	I_{SR12}	-50	-70	-90	μA	$V_{DD} = 2.7V, V_S = 2.2V$
	I_{SR12}	-40	-60	-80	μA	$V_{DD} = 2.5V, V_S = 2.0V$
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-24	-28	-32	mA	$V_{DD} = 4.5V, V_S = 2.4V$
	I_{SR22}	-4	-6	-8	mA	$V_{DD} = 2.7V, V_S = 2.2V$
	I_{SR22}	-3	-5	-7	mA	$V_{DD} = 2.5V, V_S = 2.0V$
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	$V_{DD} = 4.5V, V_S = 0.45V$
	I_{SK1}	7	10	13	mA	$V_{DD} = 2.7V, V_S = 0.45V$
	I_{SK1}	6	9	12	mA	$V_{DD} = 2.5V, V_S = 0.45V$
Brown-out Voltage with BOD_VL [1:0] = 00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out Voltage with BOD_VL [1:0] = 01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOD_VL [1:0] = 10b	$V_{BO3.7}$	3.5	3.7	3.9	V	
Brown-out Voltage with BOD_VL [1:0] = 11b	$V_{BO4.4}$	4.2	4.4	4.6	V	



8.4.8 USB PHY Specification

8.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High (driven)		2.0			V
V_{IL}	Input Low				0.8	V
V_{DI}	Differential Input Sensitivity	PADP-PADM	0.2			V
V_{CM}	Differential Common-mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
V_{OL}	Output Low (driven)		0		0.3	V
V_{OH}	Output High (driven)		2.8		3.6	V
V_{CRS}	Output Signal Cross Voltage		1.3		2.0	V
R_{PU}	Pull-up Resistor		1.425		1.575	k Ω
V_{TRM}	Termination Voltage for Upstream Port Pull-up (RPU)		3.0		3.6	V
Z_{DRV}	Driver Output Resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver Capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

8.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	$C_L=50p$	4		20	ns
T_{FF}	Fall Time	$C_L=50p$	4		20	ns
T_{FRFF}	Rise and Fall Time Matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

8.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VBUS}	VBUS Current (Steady State)	Standby		50		μA