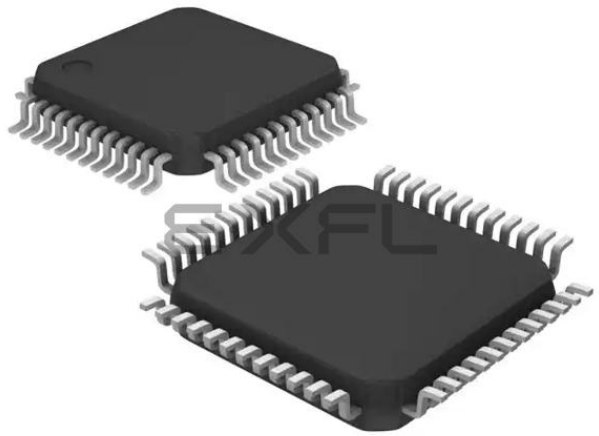

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc240le3ae

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1 GENERAL DESCRIPTION

The NuMicro™ NUC230/240 series 32-bit microcontrollers are embedded with the ARM® Cortex™-M0 core with a cost equivalent to traditional 8-bit MCU for industrial control and applications requiring rich communication interfaces. The NuMicro™ NUC230/240 series includes NUC230 and NUC240 product lines.

The NuMicro™ NUC230 CAN Line is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I^2C, I^2S, PWM Timer, GPIO, LIN, CAN, PS/2, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

The NuMicro™ NUC240 Connectivity Line with USB 2.0 full-speed and CAN functions is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I^2C, I^2S, PWM Timer, GPIO, LIN, CAN, PS/2, USB 2.0 FS Device, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I^2C	USB	LIN	CAN	PS/2	I^2S	SC
NUC230	●	●	●		●	●	●	●	●
NUC240	●	●	●	●	●	●	●	●	●

Table 1-1 NuMicro™ NUC230/240 Series Connectivity Support Table

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2.2 NuMicro™ NUC240 Features – Connectivity Line

- ARM® Cortex™-M0 core
  - Runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K/128K bytes Flash for program code
  - 8 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for 128 KB system, fixed 4 KB Data Flash for the 32 KB and 64 KB system
  - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
  - 8K/16K bytes embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ±3 % at -40 ℃ ~ +105 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 72 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Supports 4 selectable Watchdog Timer reset delay period(1026, 130, 18 or 3 WDT_CLK)

4.2.1.2 NuMicro™ NUC230SxxAE LQFP 64 pin

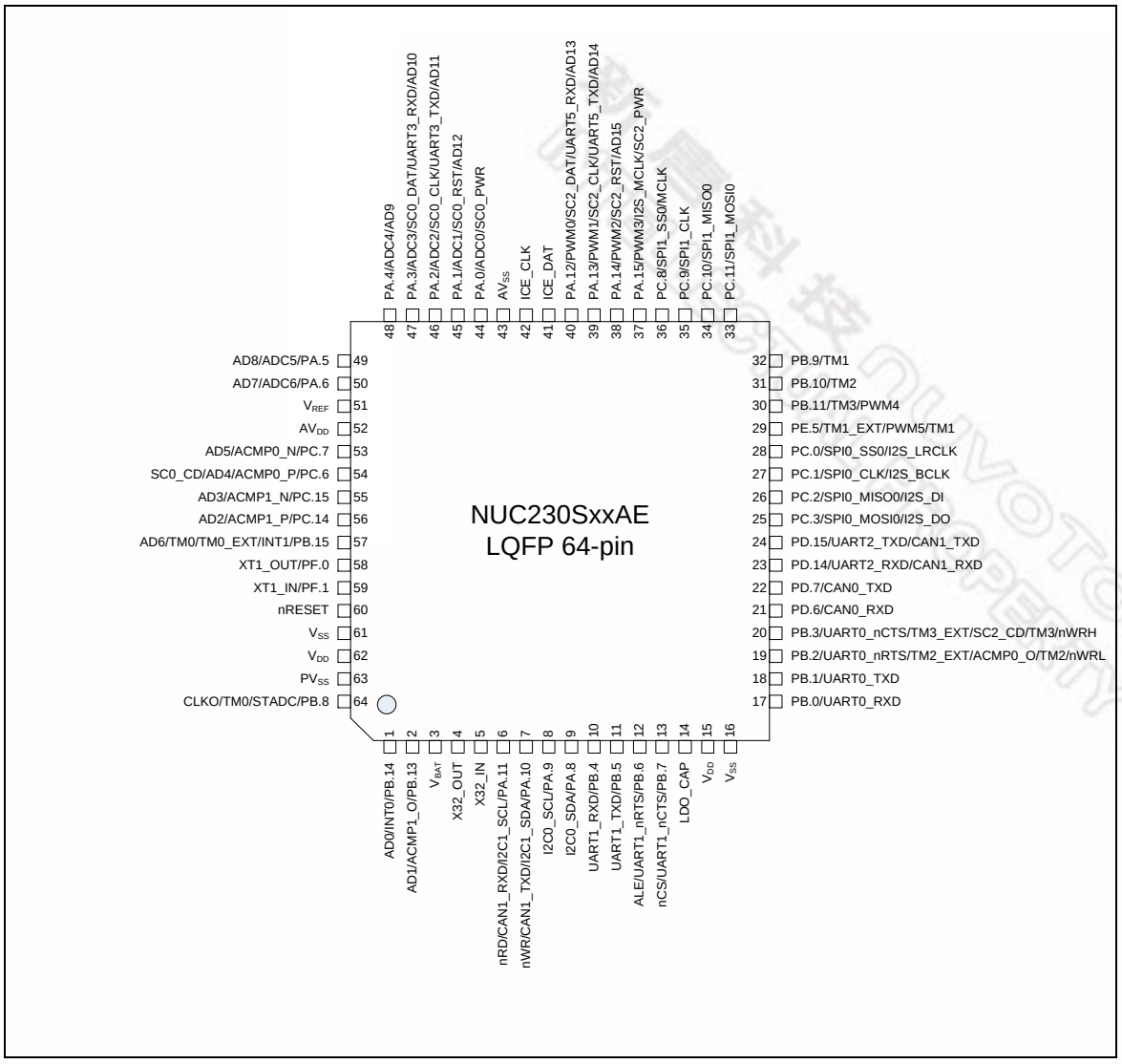

Figure 4-3 NuMicro™ NUC230SxxAE LQFP 64-pin Diagram

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4.2.1.3 NuMicro™ NUC230LxxAE LQFP 48 pin

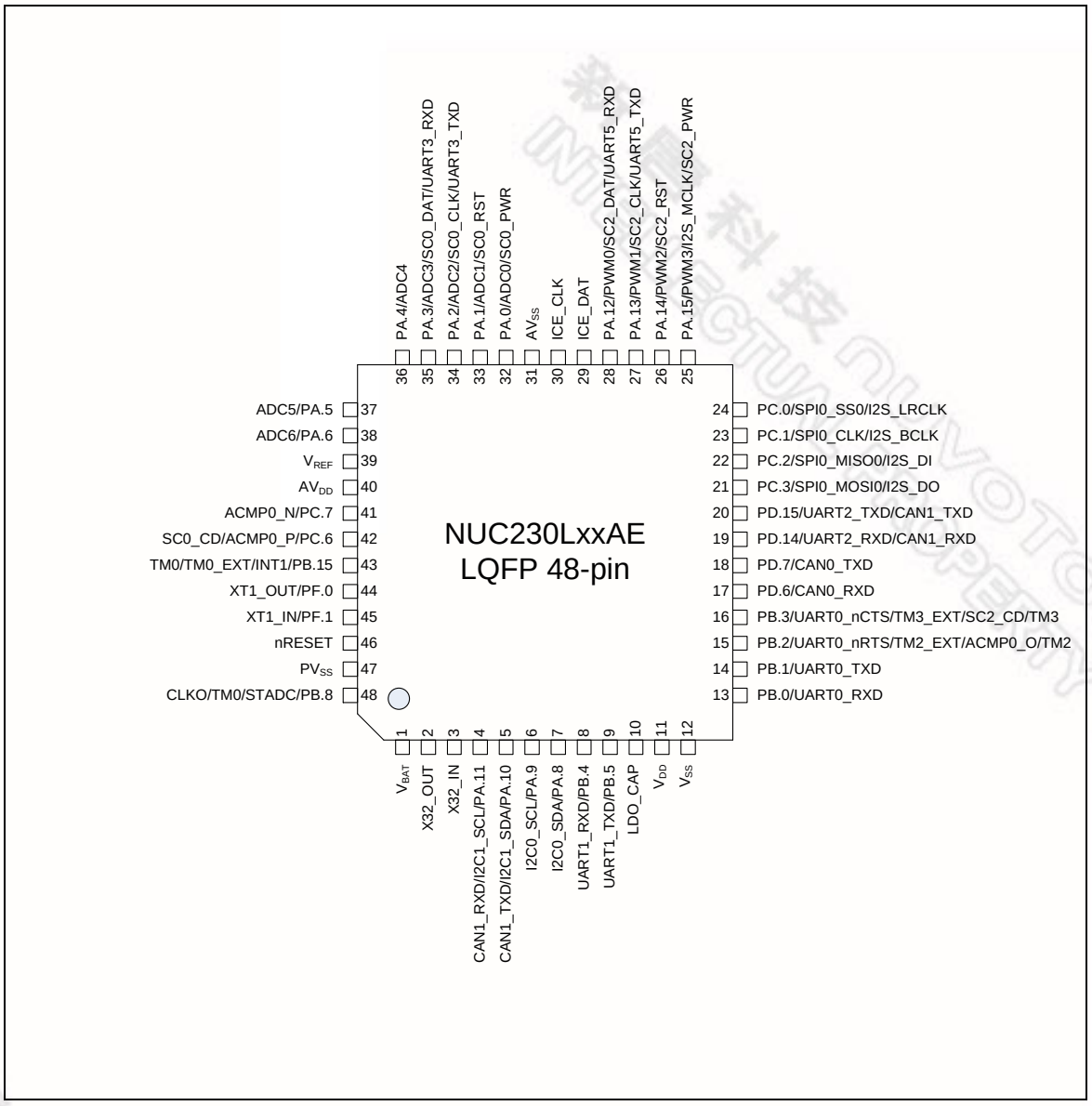

Figure 4-4 NuMicro™ NUC230LxxAE LQFP 48-pin Diagram

4.2.2.2 NuMicro™ NUC240SxxAE LQFP 64 pin

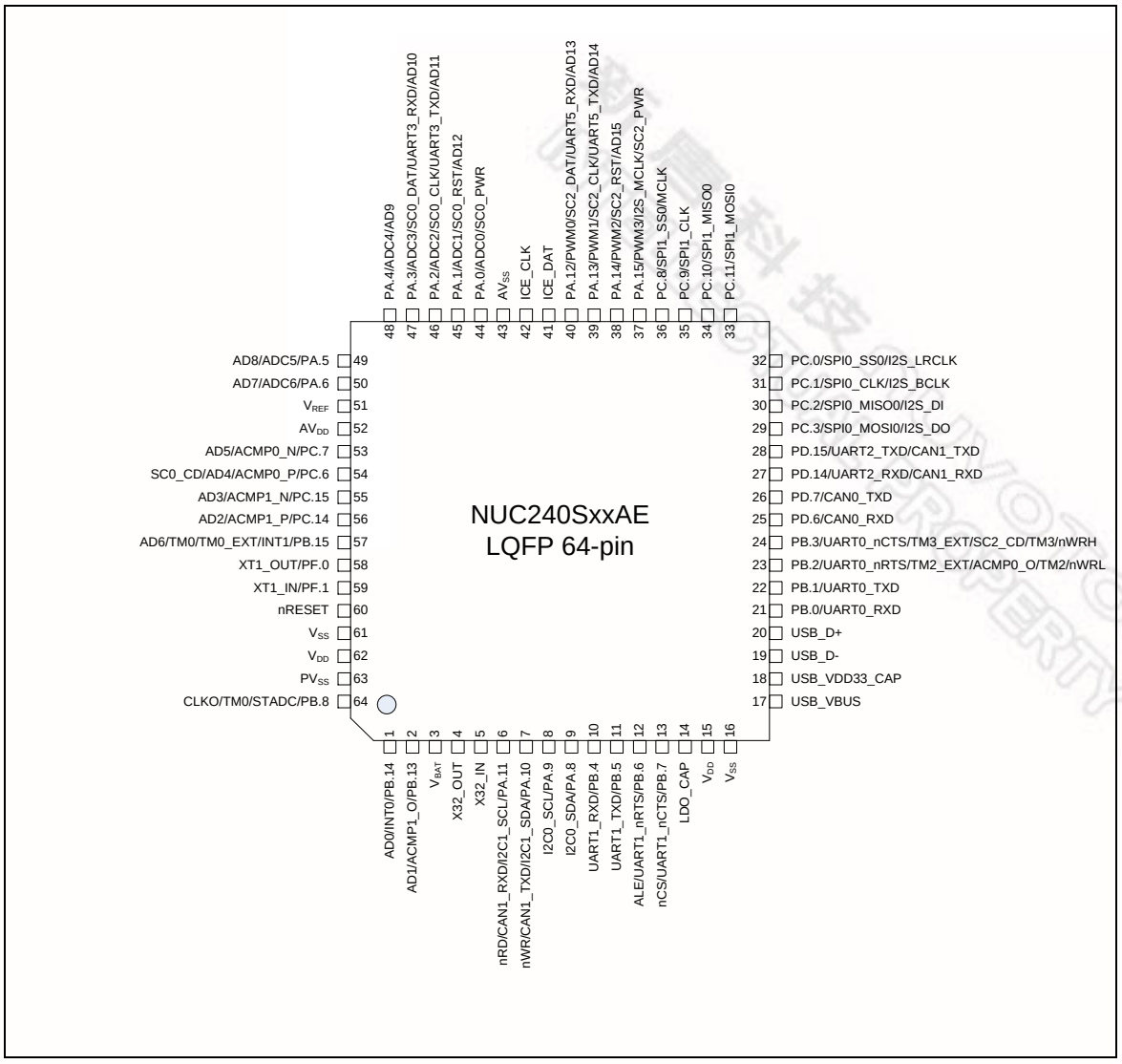

Figure 4-6 NuMicro™ NUC240SxxAE LQFP 64-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SPI1_CLK	**I/O**	SPI1 serial clock pin.
61	36		PC.8	**I/O**	General purpose digital I/O pin.
			MCLK	**O**	EBI clock output
			SPI1_SS0	**I/O**	1st SPI1 slave select pin.
62	37	25	PA.15	**I/O**	General purpose digital I/O pin.
			PWM3	**I/O**	PWM output/Capture input.
			I2S_MCLK	**O**	I^2S master clock output pin.
			SC2_PWR	**O**	SmartCard2 power pin.
63	38	26	PA.14	**I/O**	General purpose digital I/O pin.
			PWM2	**I/O**	PWM2 output/Capture input.
			SC2_RST	**O**	SmartCard2 reset pin.
			AD15	**I/O**	EBI Address/Data bus bit15
64	39	27	PA.13	**I/O**	General purpose digital I/O pin.
			PWM1	**I/O**	PWM1 output/Capture input.
			SC2_CLK	**O**	SmartCard2 clock pin.
			UART5_TXD	**O**	Data transmitter output pin for UART5.
			AD14	**I/O**	EBI Address/Data bus bit14
65	40	28	PA.12	**I/O**	General purpose digital I/O pin.
			PWM0	**I/O**	PWM0 output/Capture input.
			SC2_DAT	**O**	SmartCard2 data pin.
			UART5_RXD	**I**	Data receiver input pin for UART5.
			AD13	**I/O**	EBI Address/Data bus bit13
66	41	29	ICE_DAT	**I/O**	Serial wire debugger data pin.
67	42	30	ICE_CLK	**I**	Serial wire debugger clock pin.
68			V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V_{SS}	**P**	Ground pin for digital circuit.
70	43	31	AV_{SS}	**AP**	Ground pin for analog circuit.
71	44	32	PA.0	**I/O**	General purpose digital I/O pin.
			ADC0	**AI**	ADC0 analog input.
			SC0_PWR	**O**	SmartCard0 power pin.
72	45	33	PA.1	**I/O**	General purpose digital I/O pin.
			ADC1	**AI**	ADC1 analog input.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
60	35		PC.9	I/O	General purpose digital I/O pin.
			SPI1_CLK	I/O	SPI1 serial clock pin.
61	36		PC.8	I/O	General purpose digital I/O pin.
			MCLK	O	EBI clock output
			SPI1_SS0	I/O	1st SPI1 slave select pin.
62	37	25	PA.15	I/O	General purpose digital I/O pin.
			PWM3	I/O	PWM3 output/Capture input.
			I2S_MCLK	O	I2S master clock output pin.
			SC2_PWR	O	SmartCard2 power pin.
63	38	26	PA.14	I/O	General purpose digital I/O pin.
			PWM2	I/O	PWM2 output/Capture input.
			AD15	I/O	EBI Address/Data bus bit15
			SC2_RST	O	SmartCard2 reset pin.
64	39	27	PA.13	I/O	General purpose digital I/O pin.
			PWM1	I/O	PWM1 output/Capture input.
			AD14	I/O	EBI Address/Data bus bit14
			SC2_CLK	O	SmartCard2 clock pin.
		27	UART5_TXD	O	Data transmitter output pin for UART5.
65	40	28	PA.12	I/O	General purpose digital I/O pin.
			PWM0	I/O	PWM0 output/Capture input.
			AD13	I/O	EBI Address/Data bus bit13
			SC2_DAT	O	SmartCard2 data pin.
		28	UART5_RXD	I	Data receiver input pin for UART5.
66	41	29	ICE_DAT	I/O	Serial wire debugger data pin.
67	42	30	ICE_CLK	I	Serial wire debugger clock pin.
68			V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V_{SS}	P	Ground pin for digital circuit.
70	43	31	AV_{SS}	AP	Ground pin for analog circuit.
71	44	32	PA.0	I/O	General purpose digital I/O pin.
			ADC0	AI	ADC0 analog input.
			SC0_PWR	O	SmartCard0 power pin.
72	45	33	PA.1	I/O	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
92	58	44	PF.0	**I/O**	General purpose digital I/O pin.
			XT1_OUT	**O**	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	**I/O**	General purpose digital I/O pin.
			XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
94	60	46	nRESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V_{SS}	**P**	Ground pin for digital circuit.
96	62		V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	**I/O**	General purpose digital I/O pin.
			PS2_DAT	**I/O**	PS/2 data pin.
98			PF.3	**I/O**	General purpose digital I/O pin.
			PS2_CLK	**I/O**	PS/2 clock pin.
99	63	47	PV_{SS}	**P**	PLL ground.
100	64	48	PB.8	**I/O**	General purpose digital I/O pin.
			STADC	**I**	ADC external trigger input.
			TM0	**I/O**	Timer0 event counter input / toggle output.
			CLKO	**O**	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

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- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

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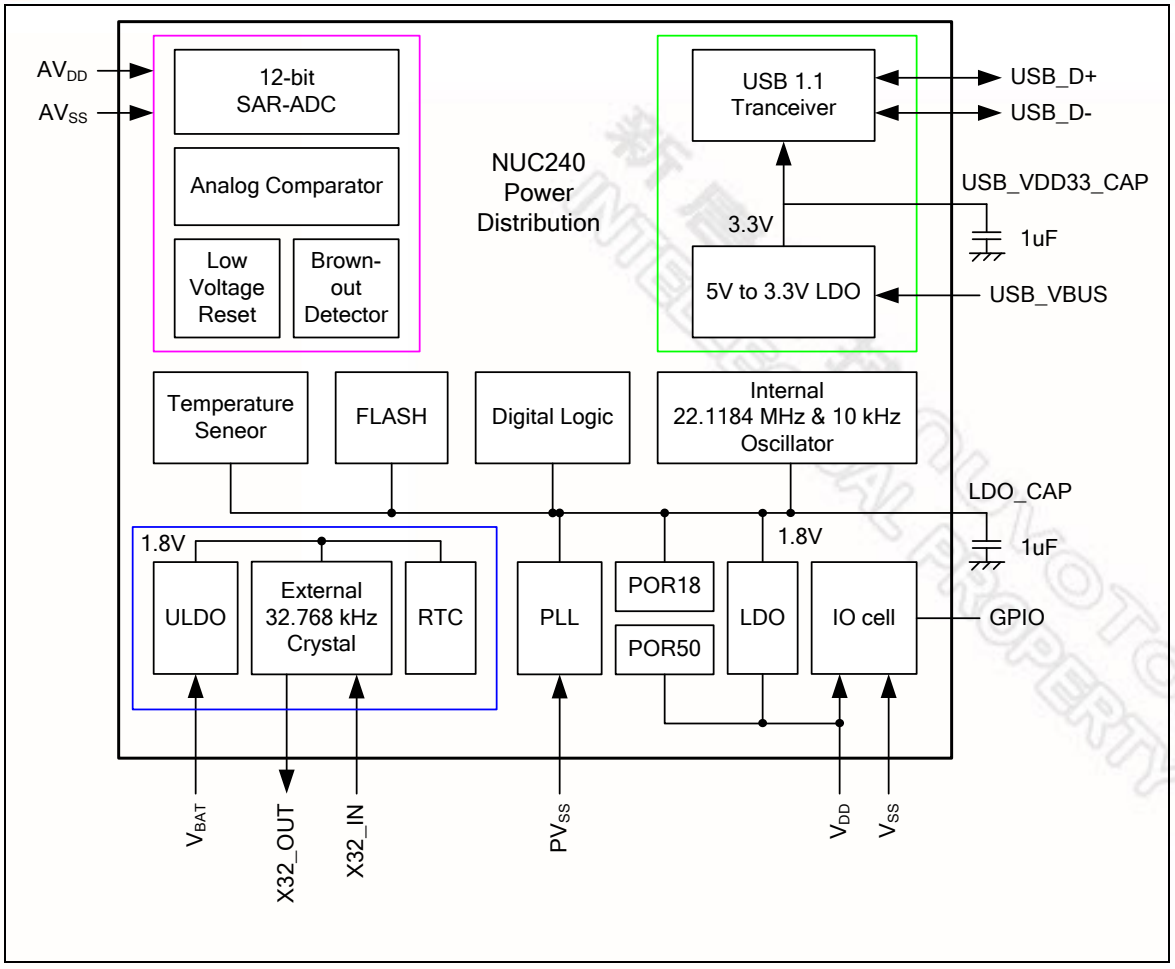

Figure 6-3 NuMicro™ NUC240 Power Distribution Diagram

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6.2.5 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

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6.2.6.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-4 Vector Table Format

6.2.6.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.7 System Control

The Cortex™-M0 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex™-M0 interrupt priority and Cortex™-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.6 General Purpose I/O (GPIO)

6.6.1 Overview

The NuMicro™ NUC230/240 series has up to 84 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 84 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B/C/D/E port has the maximum of 16 pins and GPIOF port has the maximum of 4 pins. Each of the 84 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} is from 5.0 V to 2.5 V.

6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function.

6.7 PDMA Controller (PDMA)

6.7.1 Overview

The NuMicro™ NUC230/240 series DMA contains nine-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA that transfers data to and from memory or transfer data to and from APB devices. For PDMA channel (PDMA CH0~CH8), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. Software can stop the PDMA operation by disable PDMA PDMACEN (PDMA_CSRx[0]). The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

The DMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU PIO mode and DMA transfer mode.

6.16 I²C Serial Interface Controller (I²C)

6.16.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.16.2 Features

The I²C bus uses two wires (I2Cn_SDA and I2Cn_SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C serial interface controller
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function

6.17 Serial Peripheral Interface (SPI)

6.17.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro™ NUC230/240 series contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a master or a slave device.

The SPI controller supports the variable bus clock function for special applications and 2-bit Transfer mode to connect 2 off-chip slave devices at the same time. This controller also supports the PDMA function to access the data buffer and also supports Dual I/O Transfer mode.

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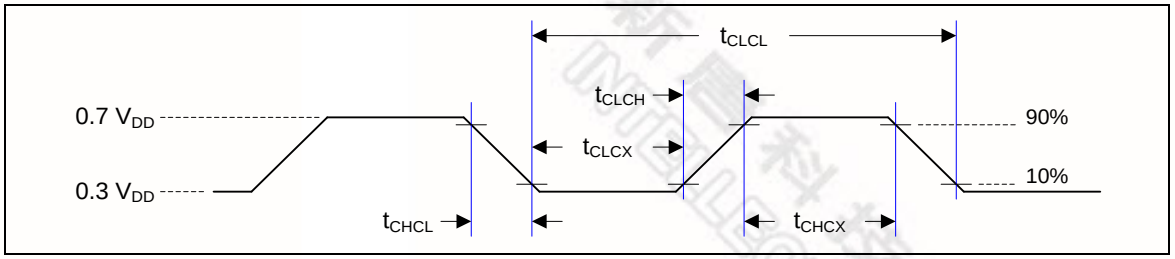
8.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=5.5 V, T_A = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation Voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5V ~ 5.5V up to 72 MHz				
Power Ground	V_{SS} AV_{SS}	-0.3			V					
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} > 2.5V				
Band-gap Voltage	V_{BG}	1.22	1.25	1.28	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = 25°C				
Analog Operating Voltage	AV_{DD}		V_{DD}		V	When system used analog function, please refer to NUC230/240 Series Technical Reference Manual chapter 6.5 for corresponding analog operating voltage				
RTC Operating Voltage	V_{BAT}	2.5		5.5	V					
Operating Current Normal Run Mode at 72 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD1}		50		mA	V_{DD}	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{DD2}		20		mA	5.5V	12 MHz	X	V	X
	I_{DD3}		48		mA	3.3V	12 MHz	X	V	V
	I_{DD4}		18		mA	3.3V	12 MHz	X	V	X
Operating Current Normal Run Mode at 50 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD5}		34		mA	5.5V	12 MHz	X	V	V
	I_{DD6}		15		mA	5.5V	12 MHz	X	V	X
	I_{DD7}		32		mA	3.3V	12 MHz	X	V	V
	I_{DD8}		14		mA	3.3V	12 MHz	X	V	X
Operating Current Normal Run Mode at 12 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD9}		8.5		mA	5.5V	12 MHz	X	X	V
	I_{DD10}		3.6		mA	5.5V	12 MHz	X	X	X
	I_{DD11}		7.5		mA	3.3V	12 MHz	X	X	V
	I_{DD12}		2.6		mA	3.3V	12 MHz	X	X	X
Operating Current Normal Run Mode at 4 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD13}		3.6		mA	5.5V	4 MHz	X	X	V
	I_{DD14}		2		mA	5.5V	4 MHz	X	X	X
	I_{DD15}		2.8		mA	3.3V	4 MHz	X	X	V
	I_{DD16}		1.2		mA	3.3V	4 MHz	X	X	X

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

8.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	105	℃
Operating Current	12 MHz at V_{DD} = 5V	-	2	-	mA
Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

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8.4.8.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V_{DD33}	LDO Output Voltage		3.0	3.3	3.6	V
C_{bp}	External Bypass Capacitor			1.0	-	uF

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		10000			cycles[1]
T_{RET}	Data Retention	At 25℃	100			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			40		μs
I_{DD1}	Read Current		-	0.15	0.5	mA/MHz
I_{DD2}	Program/Erase Current				7	mA

1. Number of program/erase cycles.
2. V_{DD} is source from chip LDO output voltage.

This table is guaranteed by design, not test in production.

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10 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.00	May 12, 2014	Preliminary version
1.01	Dec. 30,2014	1, Added EBI function 2, Rearranged the chepter sequence.

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