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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	45
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc240se3ae



6.3.3	Power-down Mode Clock	61
6.3.4	Frequency Divider Output	62
6.4	Flash Memory Controller (FMC)	63
6.4.1	Overview	63
6.4.2	Features	63
6.5	External Bus Interface (EBI)	64
6.5.1	Overview	64
6.5.2	Features	64
6.6	General Purpose I/O (GPIO)	65
6.6.1	Overview	65
6.6.2	Features	65
6.7	PDMA Controller (PDMA)	65
6.7.1	Overview	65
6.7.2	Features	66
6.8	Timer Controller (TIMER)	66
6.8.1	Overview	66
6.8.2	Features	67
6.9	PWM Generator and Capture Timer (PWM)	68
6.9.1	Overview	68
6.9.2	Features	69
6.10	Watchdog Timer (WDT)	70
6.10.1	Overview	70
6.10.2	Features	70
6.11	Window Watchdog Timer (WWDT)	71
6.11.1	Overview	71
6.11.2	Features	71
6.12	Real Time Clock (RTC)	71
6.12.1	Overview	71
6.12.2	Features	71
6.13	UART Interface Controller (UART)	72
6.13.1	Overview	72
6.13.2	Features	72
6.14	Smart Card Host Interface (SC)	73
6.14.1	Overview	73
6.14.2	Features	73



1 GENERAL DESCRIPTION

The NuMicro™ NUC230/240 series 32-bit microcontrollers are embedded with the ARM® Cortex™-M0 core with a cost equivalent to traditional 8-bit MCU for industrial control and applications requiring rich communication interfaces. The NuMicro™ NUC230/240 series includes NUC230 and NUC240 product lines.

The NuMicro™ NUC230 CAN Line is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I²C, I²S, PWM Timer, GPIO, LIN, CAN, PS/2, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

The NuMicro™ NUC240 Connectivity Line with USB 2.0 full-speed and CAN functions is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes embedded SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I²C, I²S, PWM Timer, GPIO, LIN, CAN, PS/2, USB 2.0 FS Device, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I ² C	USB	LIN	CAN	PS/2	I ² S	SC
NUC230	●	●	●		●	●	●	●	●
NUC240	●	●	●	●	●	●	●	●	●

Table 1-1 NuMicro™ NUC230/240 Series Connectivity Support Table



- 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
- Wake-up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog time-out
- Supports 4 selectable Watchdog Timer reset delay period(1026, 130, 18 or 3 WDT_CLK)
- Window Watchdog Timer
 - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
 - Supports software compensation by setting frequency compensate register (FCR)
 - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
 - Supports Alarm registers (second, minute, hour, day, month, year)
 - Selectable 12-hour or 24-hour mode
 - Automatic leap year recognition
 - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
 - Supports battery power pin (VBAT)
 - Supports wake-up function
- PWM/Capture
 - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
 - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
 - Supports One-shot or Auto-reload mode
 - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
 - Supports Capture interrupt
- UART
 - Up to six UART controllers (three UART controllers are shared with SC)
 - UART ports with flow control (TXD, RXD, nCTS and nRTS)
 - UART0 with 64-byte FIFO is for high speed
 - UART1/2(optional) with 16-byte FIFO for standard device
 - Supports IrDA (SIR) and LIN function
 - Supports RS-485 9-bit mode and direction control
 - Programmable baud-rate generator up to 1/16 system clock
 - Supports CTS wake-up function (UART0 and UART1 support)
 - Supports PDMA mode
- Smart Card Host (SC)
 - Supports up to three ISO-7816-3 ports
 - Compliant to ISO-7816-3 T=0, T=1
 - Separate receive / transmit 4 bytes entry FIFO for data payloads
 - Programmable transmission clock frequency
 - Programmable receiver buffer trigger level
 - Programmable guard time selection (11 ETU ~ 266 ETU)
 - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
 - Supports auto inverse convention function
 - Supports transmitter and receiver error retry and error limit function
 - Supports hardware activation sequence process
 - Supports hardware warm reset sequence process
 - Supports hardware deactivation sequence process
 - Supports hardware auto deactivation sequence when detecting the card is removal
 - Supports up to three UART ports
 - Full duplex, asynchronous communications
 - Supports receiving / transmitting 4-bytes FIFO
 - Supports programmable baud rate generator for each channel
 - Programmable even, odd or no parity bit generation and detection
 - Programmable stop bit, 1 or 2 stop bit generation

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ NUC230/240xxxAE Selection Guide

4.1.1 NuMicro™ NUC230 Automotive Line Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-bit)	Connectivity						I ² S	SC	Comp.	PWM	ADC (12-bit)	RTC	EBI	ISP/ICP/IAP	Package
							UART	SPI	I ² C	USB	LIN	CAN									
NUC230LC2AE	32	8	4	8	35	4	5	1	2	-	3	2	1	2	1	4	7	v	-	v	LQFP48
NUC230LD2AE	64	8	4	8	35	4	5	1	2	-	3	2	1	2	1	4	7	v	-	v	LQFP48
NUC230LE3AE	128	16	Config.	8	35	4	5	1	2	-	3	2	1	2	1	4	7	v	-	v	LQFP48
NUC230SC2AE	32	8	4	8	49	4	5	2	2	-	3	2	1	2	2	6	7	v	v	v	LQFP64
NUC230SD2AE	64	8	4	8	49	4	5	2	2	-	3	2	1	2	2	6	7	v	v	v	LQFP64
NUC230SE3AE	128	16	Config.	8	49	4	5	2	2	-	3	2	1	2	2	6	7	v	v	v	LQFP64
NUC230VE3AE	128	16	Config.	8	83	4	6	4	2	-	3	2	1	3	2	8	8	v	v	v	LQFP100

4.1.2 NuMicro™ NUC240 Connectivity Line Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-bit)	Connectivity						I ² S	SC	Comp.	PWM	ADC (12-bit)	RTC	EBI	ISP/ICP/IAP	Package
							UART	SPI	I ² C	USB	LIN	CAN									
NUC240LC2AE	32	8	4	8	31	4	4	1	2	1	2	2	1	1	1	4	7	v	-	v	LQFP48
NUC240LD2AE	64	8	4	8	31	4	4	1	2	1	2	2	1	1	1	4	7	v	-	v	LQFP48
NUC240LE3AE	128	16	Config.	8	31	4	4	1	2	1	2	2	1	1	1	4	7	v	-	v	LQFP48
NUC240SC2AE	32	8	4	8	45	4	5	2	2	1	3	2	1	2	2	4	7	v	v	v	LQFP64
NUC240SD2AE	64	8	4	8	45	4	5	2	2	1	3	2	1	2	2	4	7	v	v	v	LQFP64
NUC240SE3AE	128	16	Config.	8	45	4	5	2	2	1	3	2	1	2	2	4	7	v	v	v	LQFP64
NUC240VE3AE	128	16	Config.	8	79	4	6	4	2	1	3	2	1	3	2	8	8	v	v	v	LQFP100

4.2.1.3 NuMicro™ NUC230LxxAE LQFP 48 pin

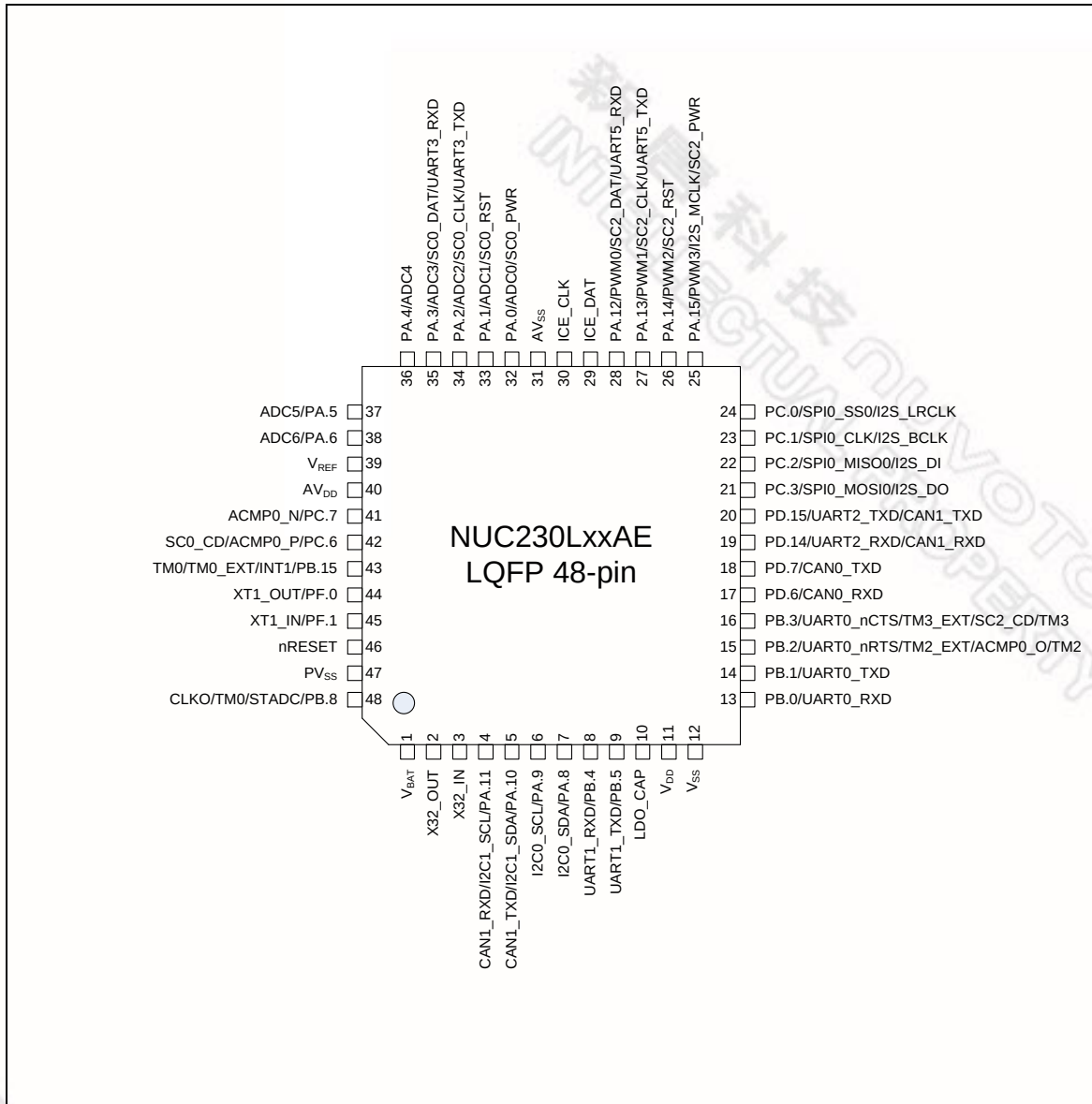


Figure 4-4 NuMicro™ NUC230LxxAE LQFP 48-pin Diagram

4.2.2.3 NuMicro™ NUC240LxxAE LQFP 48 pin

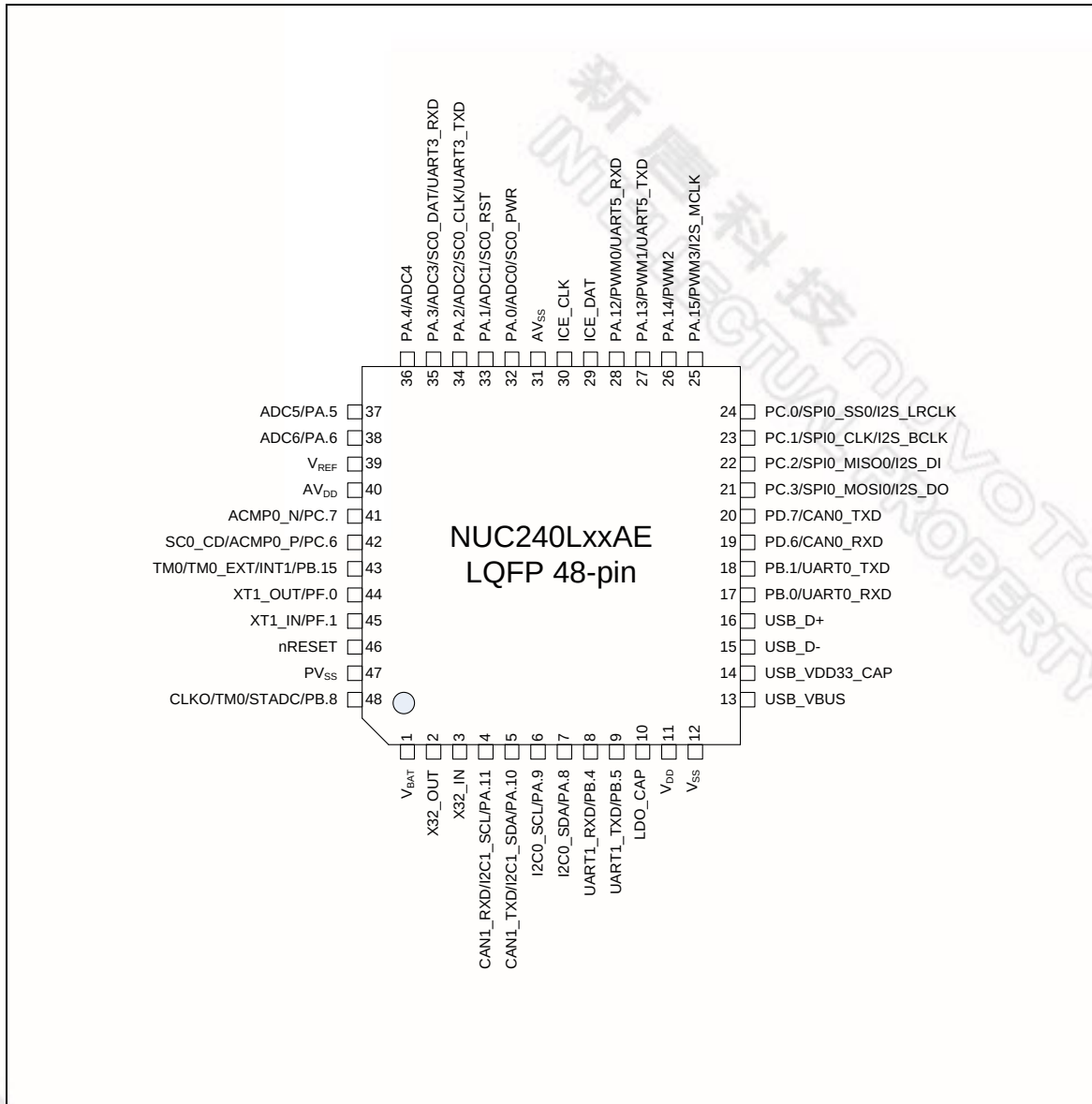


Figure 4-7 NuMicro™ NUC240LxxAE LQFP 48-pin Diagram



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SPI1_CLK	I/O	SPI1 serial clock pin.
61	36		PC.8	I/O	General purpose digital I/O pin.
			MCLK	O	EBI clock output
			SPI1_SS0	I/O	1 st SPI1 slave select pin.
62	37	25	PA.15	I/O	General purpose digital I/O pin.
			PWM3	I/O	PWM output/Capture input.
			I2S_MCLK	O	I ² S master clock output pin.
			SC2_PWR	O	SmartCard2 power pin.
63	38	26	PA.14	I/O	General purpose digital I/O pin.
			PWM2	I/O	PWM2 output/Capture input.
			SC2_RST	O	SmartCard2 reset pin.
			AD15	I/O	EBI Address/Data bus bit15
64	39	27	PA.13	I/O	General purpose digital I/O pin.
			PWM1	I/O	PWM1 output/Capture input.
			SC2_CLK	O	SmartCard2 clock pin.
			UART5_TXD	O	Data transmitter output pin for UART5.
			AD14	I/O	EBI Address/Data bus bit14
65	40	28	PA.12	I/O	General purpose digital I/O pin.
			PWM0	I/O	PWM0 output/Capture input.
			SC2_DAT	O	SmartCard2 data pin.
			UART5_RXD	I	Data receiver input pin for UART5.
			AD13	I/O	EBI Address/Data bus bit13
66	41	29	ICE_DAT	I/O	Serial wire debugger data pin.
67	42	30	ICE_CLK	I	Serial wire debugger clock pin.
68			V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V _{SS}	P	Ground pin for digital circuit.
70	43	31	AV _{SS}	AP	Ground pin for analog circuit.
71	44	32	PA.0	I/O	General purpose digital I/O pin.
			ADC0	AI	ADC0 analog input.
			SC0_PWR	O	SmartCard0 power pin.
72	45	33	PA.1	I/O	General purpose digital I/O pin.
			ADC1	AI	ADC1 analog input.



4.3.2 NuMicro™ NUC240 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	I/O	General purpose digital I/O pin.
2			PE.14	I/O	General purpose digital I/O pin.
3			PE.13	I/O	General purpose digital I/O pin.
4	1		PB.14	I/O	General purpose digital I/O pin.
			AD0	I/O	EBI Address/Data bus bit0
			INT0	I	External interrupt0 input pin.
			SPI3_SS1	I/O	2 nd SPI3 slave select pin.
5	2		PB.13	I/O	General purpose digital I/O pin.
			AD1	I/O	EBI Address/Data bus bit1
			ACMP1_O	O	Comparator1 output pin.
6	3	1	V _{BAT}	P	Power supply by batteries for RTC.
7	4	2	X32_OUT	O	External 32.768 kHz (low speed) crystal output pin.
8	5	3	X32_IN	I	External 32.768 kHz (low speed) crystal input pin.
9	6	4	PA.11	I/O	General purpose digital I/O pin.
			I2C1_SCL	I/O	I ² C1 clock pin.
			CAN1_RXD	I	Data receiver input pin for CAN1.
			nRD	O	EBI read enable output pin
10	7	5	PA.10	I/O	General purpose digital I/O pin.
			I2C1_SDA	I/O	I ² C1 data input/output pin.
			CAN1_TXD	O	Data transmitter output pin for CAN1.
			nWR	O	EBI write enable output pin
11	8	6	PA.9	I/O	General purpose digital I/O pin.
			I2C0_SCL	I/O	I ² C0 clock pin.
12	9	7	PA.8	I/O	General purpose digital I/O pin.
			I2C0_SDA	I/O	I ² C0 data input/output pin.
13			PD.8	I/O	General purpose digital I/O pin.
			SPI3_SS0	I/O	1 st SPI3 slave select pin.
14			PD.9	I/O	General purpose digital I/O pin.
			SPI3_CLK	I/O	SPI3 serial clock pin.
15			PD.10	I/O	General purpose digital I/O pin.
			SPI3_MISO0	I/O	1 st SPI3 MISO (Master In, Slave Out) pin.



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
79	51	39	V _{REF}	AP	Voltage reference input for ADC.
80	52	40	AV _{DD}	AP	Power supply for internal analog circuit.
81			PD.0	I/O	General purpose digital I/O pin.
			SPI2_SS0	I/O	1 st SPI2 slave select pin.
82			PD.1	I/O	General purpose digital I/O pin.
			SPI2_CLK	I/O	SPI2 serial clock pin.
83			PD.2	I/O	General purpose digital I/O pin.
			SPI2_MISO0	I/O	1 st SPI2 MISO (Master In, Slave Out) pin.
84			PD.3	I/O	General purpose digital I/O pin.
			SPI2_MOSI0	I/O	1 st SPI2 MOSI (Master Out, Slave In) pin.
85			PD.4	I/O	General purpose digital I/O pin.
			SPI2_MISO1	I/O	2 nd SPI2 MISO (Master In, Slave Out) pin.
86			PD.5	I/O	General purpose digital I/O pin.
			SPI2_MOSI1	I/O	2 nd SPI2 MOSI (Master Out, Slave In) pin.
87	53	41	PC.7	I/O	General purpose digital I/O pin.
			ACMP0_N	AI	Comparator0 negative input pin.
			AD5	I/O	EBI Address/Data bus bit5
			SC1_CD	I	SmartCard1 card detect pin.
88	54	42	PC.6	I/O	General purpose digital I/O pin.
			ACMP0_P	AI	Comparator0 positive input pin.
			SC0_CD	I	SmartCard0 card detect pin.
			AD4	I/O	EBI Address/Data bus bit4
89	55		PC.15	I/O	General purpose digital I/O pin.
			AD3	I/O	EBI Address/Data bus bit3
			ACMP1_N	AI	Comparator1 negative input pin.
90	56		PC.14	I/O	General purpose digital I/O pin.
			AD2	I/O	EBI Address/Data bus bit2
			ACMP1_P	AI	Comparator1 positive input pin.
91	57	43	PB.15	I/O	General purpose digital I/O pin.
			INT1	I	External interrupt1 input pin.
			TM0_EXT	I	Timer 0 external capture input pin.
			TM0	O	Timer0 toggle output pin.
			AD6	I/O	EBI Address/Data bus bit6



Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
92	58	44	PF.0	I/O	General purpose digital I/O pin.
			XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	I/O	General purpose digital I/O pin.
			XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
94	60	46	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
95	61		V _{SS}	P	Ground pin for digital circuit.
96	62		V _{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	I/O	General purpose digital I/O pin.
			PS2_DAT	I/O	PS/2 data pin.
98			PF.3	I/O	General purpose digital I/O pin.
			PS2_CLK	I/O	PS/2 clock pin.
99	63	47	PV _{SS}	P	PLL ground.
100	64	48	PB.8	I/O	General purpose digital I/O pin.
			STADC	I	ADC external trigger input.
			TM0	I/O	Timer0 event counter input / toggle output.
			CLKO	O	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

6.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.
- Battery power from V_{BAT} supplies the RTC and external 32.768 kHz crystal.

The outputs of internal voltage regulators, LDO and V_{DD33} , require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level with the digital power (V_{DD}). 錯誤! 找不到參照來源。 Figure 6-2 shows the NuMicro™ NUC230 power distribution, and Figure 6-3 shows the NuMicro™ NUC240 power distribution.

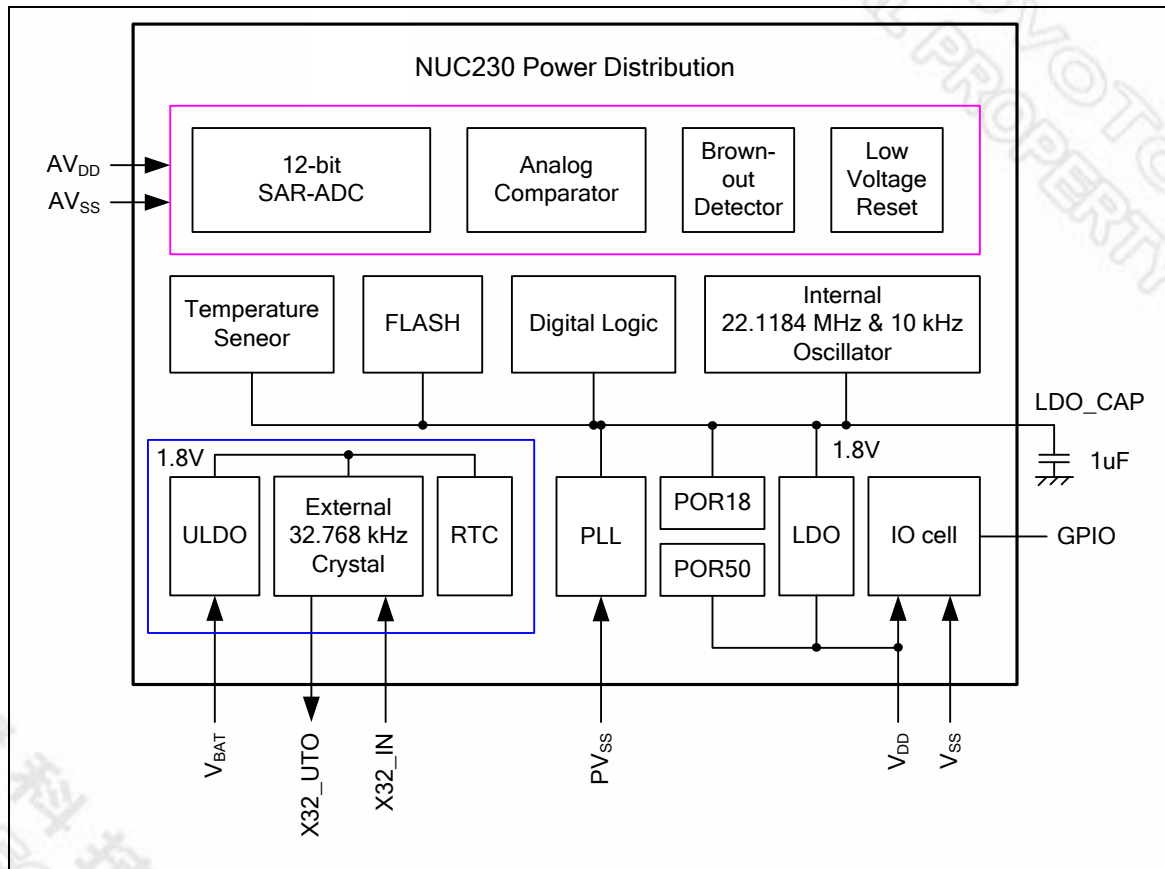


Figure 6-2 NuMicro™ NUC230 Power Distribution Diagram

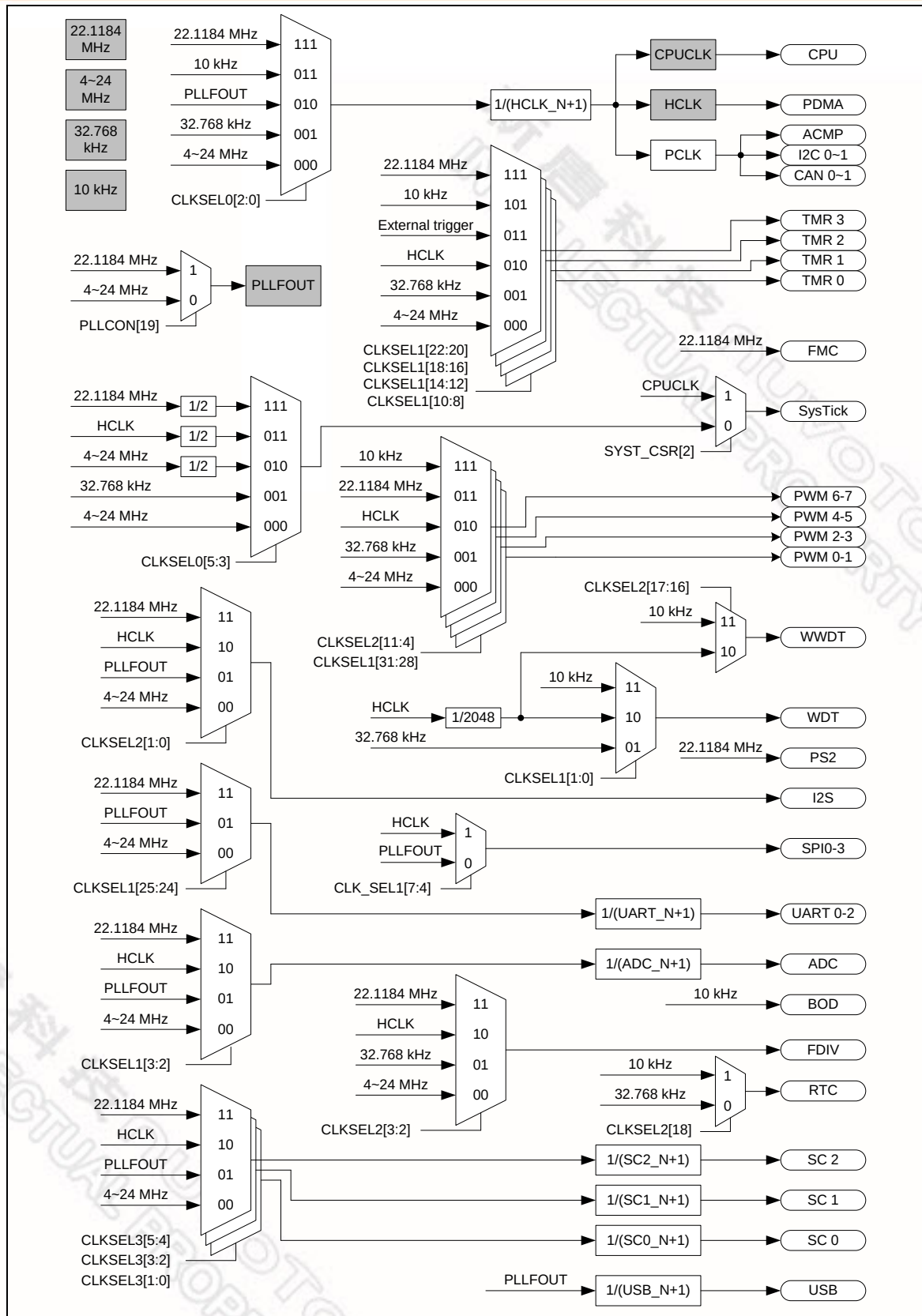


Figure 6-5 Clock Generator Global View Diagram

6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1 (FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

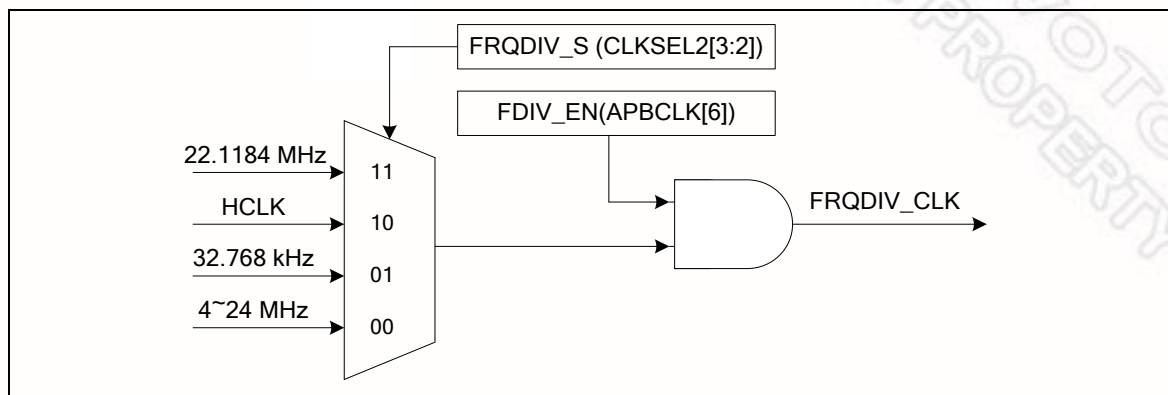


Figure 6-8 Clock Source of Frequency Divider

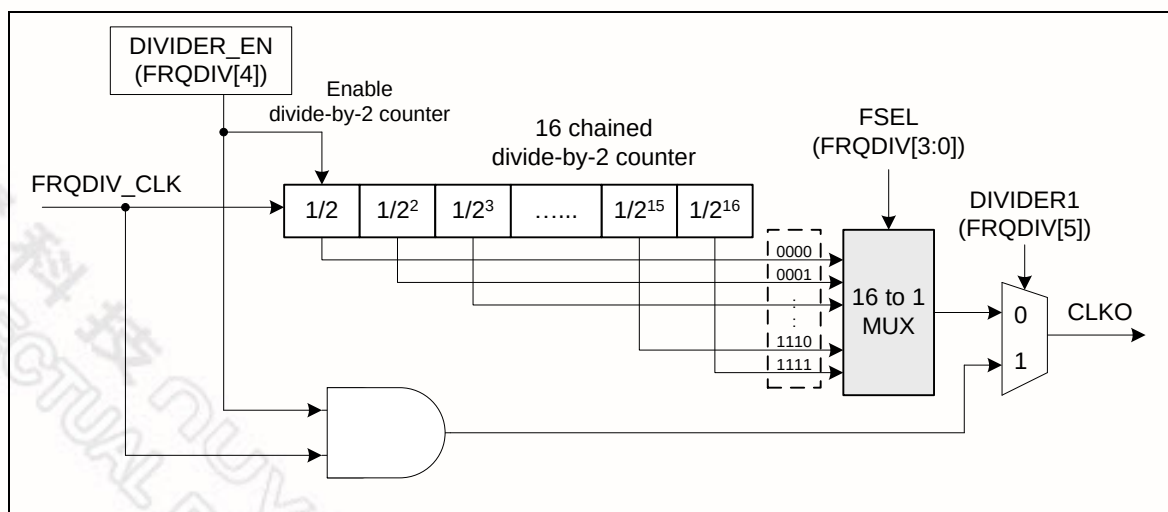


Figure 6-9 Frequency Divider Block Diagram



example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will be $1/900\text{ns} \approx 1000 \text{ kHz}$

6.9.2 Features

6.9.2.1 PWM Function:

- Up to 2 PWM groups (PWMA/PWMB) to support 8 PWM channels or 4 complementary PWM paired channels
- Each PWM group has two PWM generators with each PWM generator supporting one 8-bit prescaler, two clock divider, two PWM-timers, one Dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode
- Edge-aligned type or Center-aligned type option
- PWM trigger ADC start-to-conversion

6.9.2.2 Capture Function:

- Timing control logic shared with PWM Generators
- Supports 8 Capture input channels shared with 8 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)



6.10 Watchdog Timer (WDT)

6.10.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.10.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval ($2^4 \sim 2^{18}$) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of $(1 / \text{WDT_CLK}) * 63$
- Supports Watchdog Timer reset delay period
 - Selectable it includes (1026、130、18 or 3) * WDT_CLK reset delay period.
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG0[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz



6.20 Controller Area Network (CAN)

6.20.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface (Refer 錯誤! 找不到參照來源。). The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.20.2 Features

- Supports CAN protocol version 2.0 part A and B.
- Bit rates up to 1 MBit/s.
- 32 Message Objects.
- Each Message Object has its own identifier mask.
- Programmable FIFO mode (concatenation of Message Objects).
- Maskable interrupt.
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications.
- Programmable loop-back mode for self-test operation.
- 16-bit module interfaces to the AMBA APB bus.
- Supports wake-up function

6.21 Analog-to-Digital Converter (ADC)

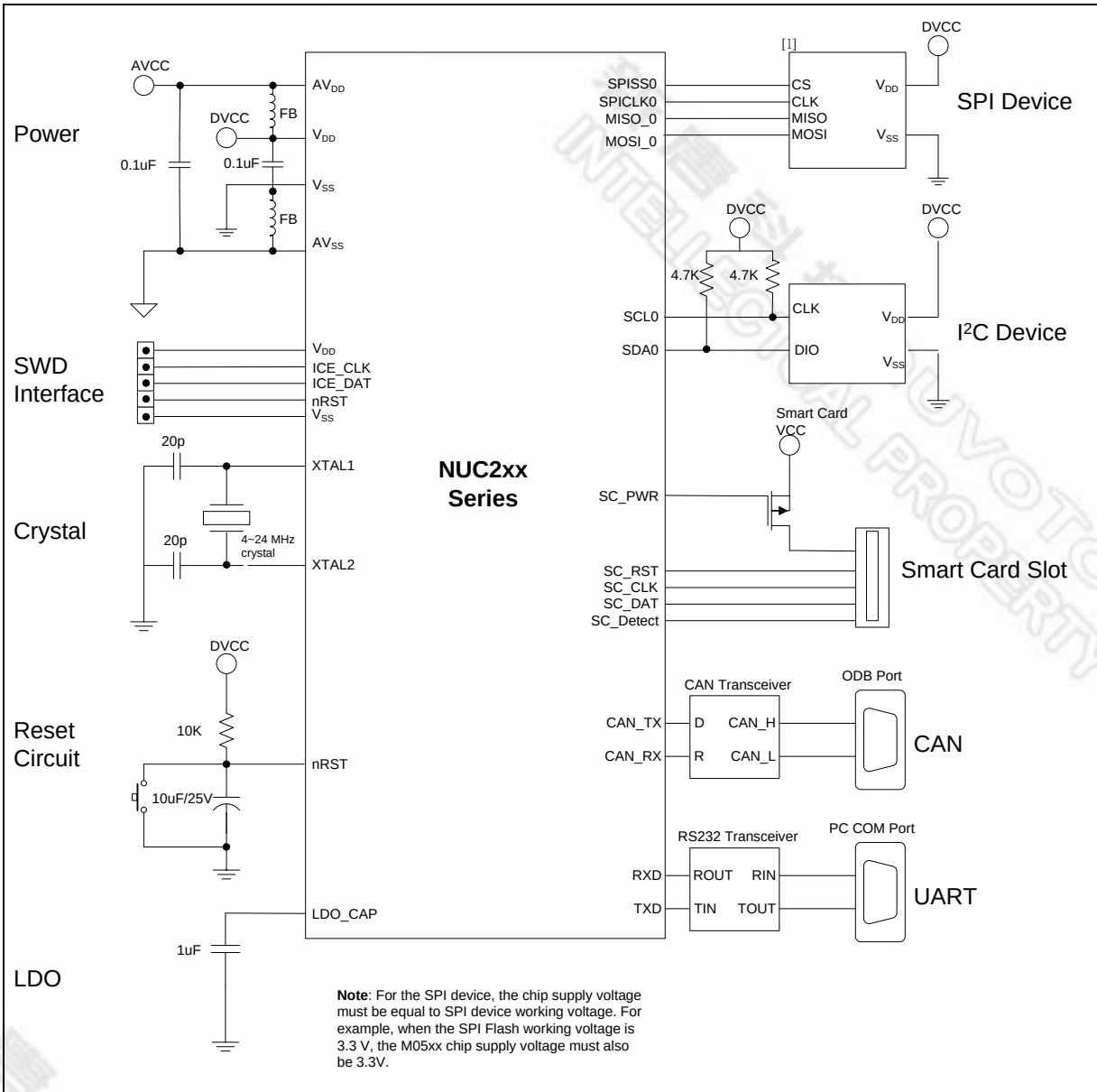
6.21.1 Overview

The NuMicro™ NUC230/240 series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM Center-aligned trigger and external STADC pin.

6.21.2 Features

- Analog input voltage range: 0~VREF
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels

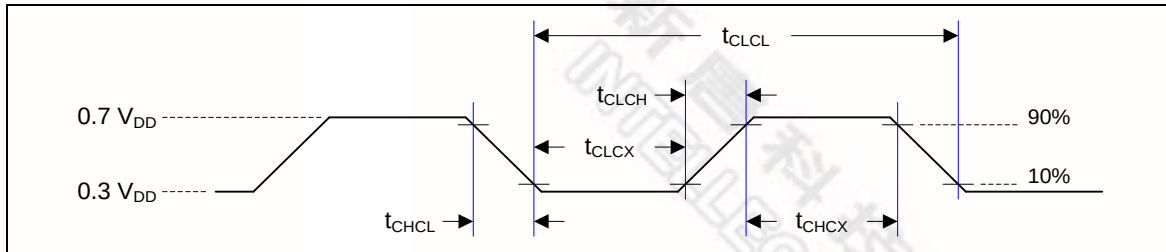
7 APPLICATION CIRCUIT





8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

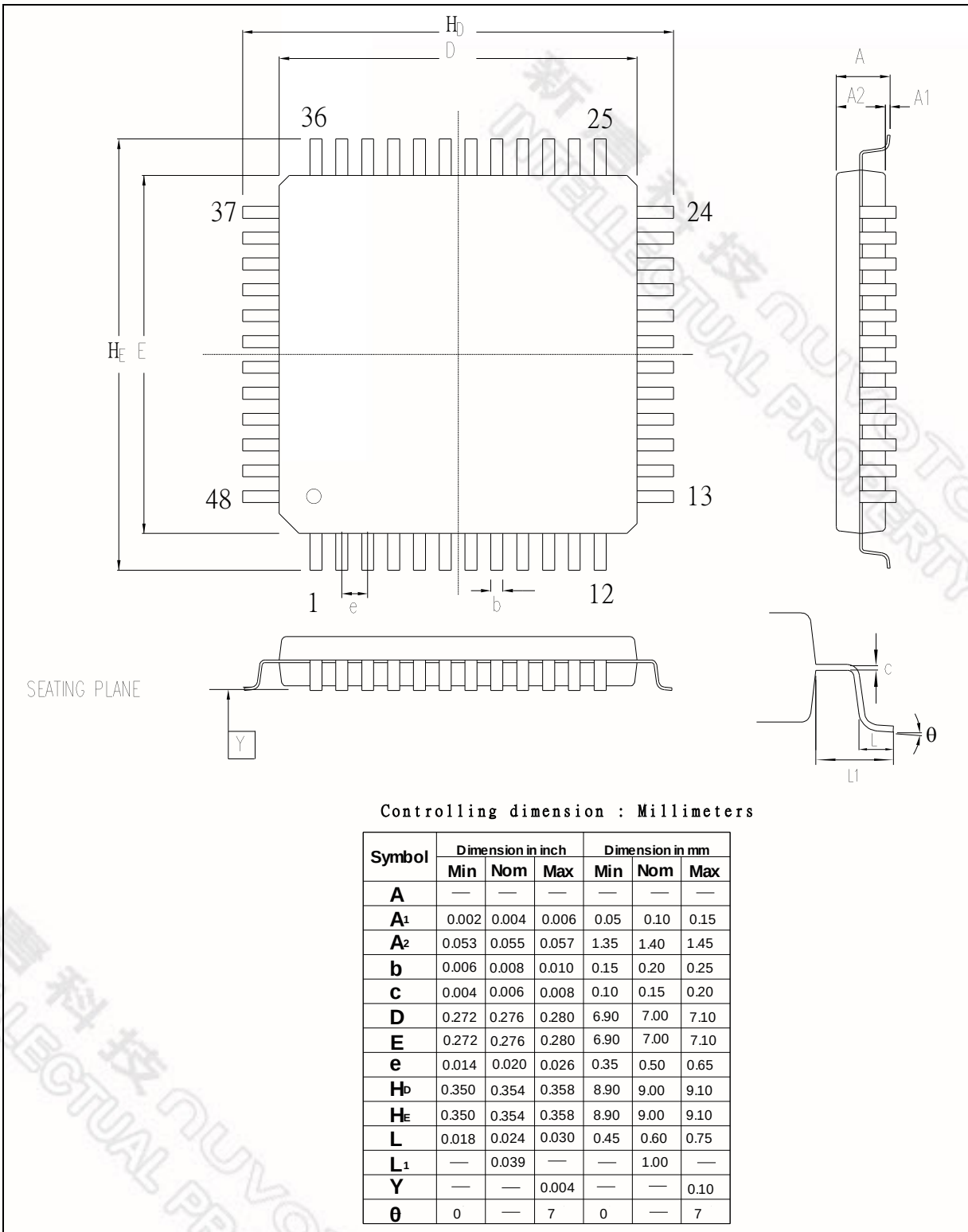
8.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	105	°C
Operating Current	12 MHz at $V_{DD} = 5V$	-	2	-	mA
Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

9.3 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)





10 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.00	May 12, 2014	Preliminary version
1.01	Dec. 30, 2014	1, Added EBI function 2, Rearranged the chepter sequence.

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