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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | HCS12X |
| Core Size | 16-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SCI, SPI |
| Peripherals | LCD, Motor control PWM, POR, PWM, WDT |
| Number of I/O | 117 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.35V ~ 5.5V |
| Data Converters | A/D 16x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12xhz256vagr |

## 2.3.2 Port C and Port D

Port C and port D pins can be used for either general-purpose I/O or the external data bus input/outputs DATA15-DATA0. Refer to the S12X_EBI block description chapter for information on external bus.

### 2.3.2.1 Port C I/O Register (PTC)

Module Base + 0x0051

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTC7 | PTC6 | PTC5 | PTC4 | PTC3 | PTC2 | PTC1 | PTC0 |
| XEBI: | DATA15 | DATA14 | DATA13 | DATA12 | DATA11 | DATA10 | DATA9 | DATA8 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-6. Port C I/O Register (PTC)**

Read: Anytime. Write: Anytime.

If the data direction bit of the associated I/O pin (DDRCx) is set to 1 (output), a write to the corresponding I/O Register bit sets the value to be driven to the Port C pin. If the data direction bit of the associated I/O pin (DDRCx) is set to 0 (input), a write to the corresponding I/O Register bit takes place but has no effect on the Port C pin.

If the associated data direction bit (DDRCx) is set to 1 (output), a read returns the value of the I/O register bit. If the associated data direction bit (DDRCx) is set to 0 (input), a read returns the value of the pin.

### 2.3.2.2 Port D I/O Register (PTD)

Module Base + 0x0051

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTD7 | PTD6 | PTD5 | PTD4 | PTD3 | PTD2 | PTD1 | PTD0 |
| XEBI: | DATA7 | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-7. Port D I/O Register (PTD)**

Read: Anytime. Write: Anytime.

If the data direction bit of the associated I/O pin (DDRDx) is set to 1 (output), a write to the corresponding I/O Register bit sets the value to be driven to the Port D pin. If the data direction bit of the associated I/O pin (DDRDx) is set to 0 (input), a write to the corresponding I/O Register bit takes place but has no effect on the Port D pin.

If the associated data direction bit (DDRDx) is set to 1 (output), a read returns the value of the I/O register bit. If the associated data direction bit (DDRDx) is set to 0 (input), a read returns the value of the pin.

### 2.3.3 Port E

Port E pins can be used for either general-purpose I/O, or the liquid crystal display (LCD) driver, or the external bus control outputs R/$\overline{W}$, $\overline{WE}$, $\overline{LSTRB}$, $\overline{LDS}$ and $\overline{RE}$, the free running clock outputs ECLK and ECLKX2, or the inputs $\overline{TAGHI}$, $\overline{TAGLO}$, MODA, MODB, EROMCTL, XCLKS and interrupts $\overline{IRQ}$ and $\overline{XIRQ}$. Refer to the LCD block description chapter for information on enabling and disabling the LCD and its frontplane drivers. Refer to the S12X_EBI block description chapter for information on external bus.

Port E pin PE[7] can be used for either general-purpose I/O, or as the free-running clock ECLKX2 output running at the core clock rate, or the frontplane driver FP22. The clock ECLKX2 output is always enabled in emulation modes.

Port E pin PE[4] can be used for either general-purpose I/O or as the free-running clock ECLK output running at the bus clock rate or at the programmed divided clock rate. The clock output is always enabled in emulation modes.

Port E pin PE[1] can be used for either general-purpose input or as the level- or falling edge-sensitive $\overline{IRQ}$ interrupt inpu. $\overline{IRQ}$ will be enabled by setting the IRQEN configuration bit and clearing the I-bit in the CPU's condition code register. It is inhibited at reset so this pin is initially configured as a simple input with a pull-up.

Port E pin PE[0] can be used for either general-purpose input or as the level-sensitive $\overline{XIRQ}$ interrupt input. $\overline{XIRQ}$ can be enabled by clearing the X-bit in the CPU's condition code register. It is inhibited at reset so this pin is initially configured as a high-impedance input with a pull-up.

#### 2.3.3.1 Port E I/O Register (PTE)

Module Base + 0x0051

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PTE7 | PTE6 | PTE5 | PTE4 | PTE3 | PTE2 | PTE1 | PTE0 |
| XEBI: | XCLKS[1] or ECLKX2 | MODB[1] or $\overline{TAGHI}$ | MODA[1] or $\overline{TAGLO}$ or $\overline{RE}$ | ECLK | EROMCTL[1] or $\overline{LSTRB}$ or $\overline{LDS}$ | R/$\overline{W}$ or $\overline{WE}$ | $\overline{IRQ}$ | $\overline{XIRQ}$ |
| LCD: | FP22 | | | | FP21 | FP20 | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | —[2] | —[2] |

**Figure 2-10. Port E I/O Register (PTE)**

1 Function active when $\overline{RESET}$ asserted.

2 These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Read: Anytime. Write: Anytime.

If the associated data direction bit (DDREx) is set to 1 (output), a read returns the value of the I/O register bit.

### 2.3.6.4 Port AD Reduced Drive Register (RDRAD)

Module Base + 0x0057

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | RDRAD7 | RDRAD6 | RDRAD5 | RDRAD4 | RDRAD3 | RDRAD2 | RDRAD1 | RDRAD0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-22. Port AD Reduced Drive Register (RDRAD)**

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

**Table 2-16. RDRAD Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>RDRAD[7:0] | **Reduced Drive Port A**<br>0 Full drive strength at output.<br>1 Associated pin drives at about 1/3 of the full drive strength. |

### 2.3.6.5 Port AD Pull Device Enable Register (PERAD)

Module Base + 0x0059

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PERAD7 | PERAD6 | PERAD5 | PERAD4 | PERAD3 | PERAD2 | PERAD1 | PERAD0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-23. Port AD Pull Device Enable Register (PERAD)**

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

**Table 2-17. PERAD Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PERAD[7:0] | **Pull Device Enable Port AD**<br>0 Pull-up or pull-down device is disabled.<br>1 Pull-up or pull-down device is enabled. |

### 2.3.7.6 Port L Polarity Select Register (PPSL)

Module Base + 0x0035

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PPSL7 | PPSL6 | PPSL5 | PPSL4 | PPSL3 | PPSL2 | PPSL1 | PPSL0 |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Figure 2-32. Port L Polarity Select Register (PPSL)**

Read: Anytime. Write: Anytime.

The Port L Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port L Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

**Table 2-24. PPSL Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>PPSL[7:0] | **Pull Select Port L**<br>0 A pull-up device is connected to the associated port L pin.<br>1 A pull-down device is connected to the associated port L pin. |

### 2.3.7.7 Port L Slew Rate Register (SRRL)

Module Base + 0x003B

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | SRRL7 | SRRL6 | SRRL5 | SRRL4 | SRRL3 | SRRL2 | SRRL1 | SRRL0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-33. Port L Slew Rate Register (SRRL)**

Read: Anytime. Write: Anytime.

This register enables the slew rate control and disables the digital input buffer for port pins PL[7:0].

**Table 2-25. SRRL Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>SRRL[7:0] | **Slew Rate Port L**<br>0 Disables slew rate control and enables digital input buffer.<br>1 Enables slew rate control and disables digital input buffer. |

CBEIF, PVIOL, and ACCERR are readable and writable, CCIF and BLANK are readable and not writable, remaining bits read 0 and are not writable in normal mode. FAIL is readable and writable in special mode. FAIL must be clear in special mode when starting a command write sequence.

**Table 3-15. FSTAT Field Descriptions**

| Field | Description |
|---|---|
| 7<br>CBEIF | **Command Buffer Empty Interrupt Flag** — The CBEIF flag indicates that the address, data and command buffers are empty so that a new command write sequence can be started. Writing a 0 to the CBEIF flag has no effect on CBEIF. Writing a 0 to CBEIF after writing an aligned word to the Flash address space, but before CBEIF is cleared, will abort a command write sequence and cause the ACCERR flag to be set. Writing a 0 to CBEIF outside of a command write sequence will not set the ACCERR flag. The CBEIF flag is cleared by writing a 1 to CBEIF. The CBEIF flag is used together with the CBEIE bit in the FCNFG register to generate an interrupt request (see Figure 3-32).<br>0 Command buffers are full.<br>1 Command buffers are ready to accept a new command. |
| 6<br>CCIF | **Command Complete Interrupt Flag** — The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is cleared and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active commands completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect on CCIF. The CCIF flag is used together with the CCIE bit in the FCNFG register to generate an interrupt request (see Figure 3-32).<br>0 Command in progress.<br>1 All commands are completed. |
| 5<br>PVIOL | **Protection Violation Flag** —The PVIOL flag indicates an attempt was made to program or erase an address in a protected area of the Flash memory during a command write sequence. Writing a 0 to the PVIOL flag has no effect on PVIOL. The PVIOL flag is cleared by writing a 1 to PVIOL. While PVIOL is set, it is not possible to launch a command or start a command write sequence.<br>0 No protection violation detected.<br>1 Protection violation has occurred. |
| 4<br>ACCERR | **Access Error Flag** — The ACCERR flag indicates an illegal access has occurred to the Flash memory caused by either a violation of the command write sequence (see Section 3.4.1.2, “Command Write Sequence”), issuing an illegal Flash command (see Table 3-17), launching the sector erase abort command terminating a sector erase operation early (see Section 3.4.2.6, “Sector Erase Abort Command”) or the execution of a CPU STOP instruction while a command is executing (CCIF = 0). Writing a 0 to the ACCERR flag has no effect on ACCERR. The ACCERR flag is cleared by writing a 1 to ACCERR.While ACCERR is set, it is not possible to launch a command or start a command write sequence. If ACCERR is set by an erase verify operation or a data compress operation, any buffered command will not launch.<br>0 No access error detected.<br>1 Access error has occurred. |
| 2<br>BLANK | **Flag Indicating the Erase Verify Operation Status** — When the CCIF flag is set after completion of an erase verify command, the BLANK flag indicates the result of the erase verify operation. The BLANK flag is cleared by the Flash module when CBEIF is cleared as part of a new valid command write sequence. Writing to the BLANK flag has no effect on BLANK.<br>0 Flash block verified as not erased.<br>1 Flash block verified as erased. |
| 1<br>FAIL | **Flag Indicating a Failed Flash Operation** — The FAIL flag will set if the erase verify operation fails (selected Flash block verified as not erased). Writing a 0 to the FAIL flag has no effect on FAIL. The FAIL flag is cleared by writing a 1 to FAIL.<br>0 Flash operation completed without error.<br>1 Flash operation failed. |

# BLO

## Branch if Carry Set (Same as BCS)

BLO

### Operation

If C = 1, then PC + $0002 + (REL9 << 1) ⇒ PC

Branch instruction to compare unsigned numbers.

Branch if RS1 < RS2:

```
SUB     R0,RS1,RS2
BLO     REL9
```

### CCR Effects

| N | Z | V | C |
|---|---|---|---|
| — | — | — | — |

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

### Code and CPU Cycles

| Source Form | Address Mode | Machine Code | | | | | | | | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|
| BLO REL9 | REL9 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | REL9 | PP/P |

# BMI Branch if Minus BMI

## Operation

If N = 1, then PC + $0002 + (REL9 << 1) ⇒ PC

Tests the Sign flag and branches if N = 1.

## CCR Effects

| N | Z | V | C |
|---|---|---|---|
| — | — | — | — |

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

## Code and CPU Cycles

| Source Form | Address Mode | Machine Code | | | | | | | | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|
| BMI REL9 | REL9 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | REL9 | PP/P |

# BRK Break BRK

## Operation

Put XGATE into Debug Mode (see Section 5.6.2, “Entering Debug Mode”)and signals a Software breakpoint to the S12X_DBG module (see section 4.9 of the **S12X_DBG Section**).

**NOTE**

It is not possible to single step over a BRK instruction. This instruction does not advance the program counter.

## CCR Effects

| N | Z | V | C |
|---|---|---|---|
| — | — | — | — |

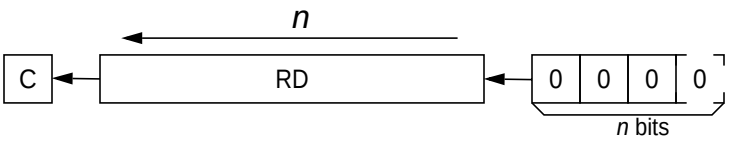
N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

## Code and CPU Cycles

| Source Form | Address Mode | Machine Code | | | | | | | | | | | | | | | | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BRK | INH | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PAff |

# LSL — Logical Shift Left — LSL

## Operation




*n* = RS or IMM4

Shifts the bits in register RD *n* positions to the left. The lower *n* bits of the register RD become filled with zeros. The carry flag will be updated to the bit contained in RD[16-n] before the shift for *n* > 0.

*n* can range from 0 to 16.

In immediate address mode, *n* is determined by the operand IMM4. *n* is considered to be 16 in IMM4 is equal to 0.

In dyadic address mode, *n* is determined by the content of RS. *n* is considered to be 16 if the content of RS is greater than 15.

## CCR Effects

| N | Z | V | C |
|---|---|---|---|
| Δ | Δ | Δ | Δ |

N: Set if bit 15 of the result is set; cleared otherwise.

Z: Set if the result is $0000; cleared otherwise.

V: Set if a two´s complement overflow resulted from the operation; cleared otherwise.
$RD[15]_{old}$ ^ $RD[15]_{new}$

C: Set if *n* > 0 and RD[16-n] = 1; if n = 0 unaffected.

## Code and CPU Cycles

| Source Form | Address Mode | Machine Code | | | | | | | | | | | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LSL RD, #IMM4 | IMM4 | 0 | 0 | 0 | 0 | 1 | RD | IMM4 | | 1 | 1 | 0 | 0 | P |
| LSL RD, RS | DYA | 0 | 0 | 0 | 0 | 1 | RD | RS | 1 | 0 | 1 | 0 | 0 | P |

### 7.3.2.5 CRG Interrupt Enable Register (CRGINT)

This register enables CRG interrupt requests.

Module Base +0x_04

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | RTIE | ILAF | 0 | LOCKIE | 0 | 0 | SCMIE | 0 |
| W | | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

1. ILAF is set to 1 when an illegal address reset occurs. Unaffected by system reset. Cleared by power on or low voltage reset.

= Unimplemented or Reserved

**Figure 7-8. CRG Interrupt Enable Register (CRGINT)**

Read: Anytime

Write: Anytime

**Table 7-3. CRGINT Field Descriptions**

| Field | Description |
|---|---|
| 7<br>RTIE | **Real Time Interrupt Enable Bit**<br>0 Interrupt requests from RTI are disabled.<br>1 Interrupt will be requested whenever RTIF is set. |
| 6<br>ILAF | **Illegal Address Reset Flag** — ILAF is set to 1 when an illegal address reset occurs. Refer to S12XMMC Block Guide for details. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 Illegal address reset has not occurred.<br>1 Illegal address reset has occurred. |
| 4<br>LOCKIE | **Lock Interrupt Enable Bit**<br>0 LOCK interrupt requests are disabled.<br>1 Interrupt will be requested whenever LOCKIF is set. |
| 1<br>SCMIE | **Self Clock Mode Interrupt Enable Bit**<br>0 SCM interrupt requests are disabled.<br>1 Interrupt will be requested whenever SCMIF is set. |

1. Read: Anytime
   Write: Anytime when out of initialization mode; exceptions are read-only RXACT and SYNCH, RXFRM (which is set by the module only), and INITRQ (which is also writable in initialization mode)

**NOTE**

The CANCTL0 register, except WUPE, INITRQ, and SLPRQ, is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

**Table 14-3. CANCTL0 Register Field Descriptions**

| Field | Description |
|---|---|
| 7<br>RXFRM(1) | **Received Frame Flag** — This bit is read and clear only. It is set when a receiver has received a valid message correctly, independently of the filter configuration. After it is set, it remains set until cleared by software or reset. Clearing is done by writing a 1. Writing a 0 is ignored. This bit is not valid in loopback mode.<br>0 No valid message was received since last clearing this flag<br>1 A valid message was received since last clearing of this flag |
| 6<br>RXACT | **Receiver Active Status** — This read-only flag indicates the MSCAN is receiving a message. The flag is controlled by the receiver front end. This bit is not valid in loopback mode.<br>0 MSCAN is transmitting or idle[2]<br>1 MSCAN is receiving a message (including when arbitration is lost)(2) |
| 5<br>CSWAI(3) | **CAN Stops in Wait Mode** — Enabling this bit allows for lower power consumption in wait mode by disabling all the clocks at the CPU bus interface to the MSCAN module.<br>0 The module is not affected during wait mode<br>1 The module ceases to be clocked during wait mode |
| 4<br>SYNCH | **Synchronized Status** — This read-only flag indicates whether the MSCAN is synchronized to the CAN bus and able to participate in the communication process. It is set and cleared by the MSCAN.<br>0 MSCAN is not synchronized to the CAN bus<br>1 MSCAN is synchronized to the CAN bus |
| 3<br>TIME | **Timer Enable** — This bit activates an internal 16-bit wide free running timer which is clocked by the bit clock rate. If the timer is enabled, a 16-bit time stamp will be assigned to each transmitted/received message within the active TX/RX buffer. Right after the EOF of a valid message on the CAN bus, the time stamp is written to the highest bytes (0x000E, 0x000F) in the appropriate buffer (see Section 14.3.3, "Programmer's Model of Message Storage"). The internal timer is reset (all bits set to 0) when disabled. This bit is held low in initialization mode.<br>0 Disable internal MSCAN timer<br>1 Enable internal MSCAN timer |
| 2<br>WUPE(4) | **Wake-Up Enable** — This configuration bit allows the MSCAN to restart from sleep mode or from power down mode (entered from sleep) when traffic on CAN is detected (see Section 14.4.5.5, "MSCAN Sleep Mode"). This bit must be configured before sleep mode entry for the selected function to take effect.<br>0 Wake-up disabled — The MSCAN ignores traffic on CAN<br>1 Wake-up enabled — The MSCAN is able to restart |

**Table 14-4. CANCTL1 Register Field Descriptions (continued)**

| Field | Description |
|---|---|
| 1<br>SLPAK | **Sleep Mode Acknowledge** — This flag indicates whether the MSCAN module has entered sleep mode (see Section 14.4.5.5, "MSCAN Sleep Mode"). It is used as a handshake flag for the SLPRQ sleep mode request. Sleep mode is active when SLPRQ = 1 and SLPAK = 1. Depending on the setting of WUPE, the MSCAN will clear the flag if it detects activity on the CAN bus while in sleep mode.<br>0 Running — The MSCAN operates normally<br>1 Sleep mode active — The MSCAN has entered sleep mode |
| 0<br>INITAK | **Initialization Mode Acknowledge** — This flag indicates whether the MSCAN module is in initialization mode (see Section 14.4.4.5, "MSCAN Initialization Mode"). It is used as a handshake flag for the INITRQ initialization mode request. Initialization mode is active when INITRQ = 1 and INITAK = 1. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0–CANIDAR7, and CANIDMR0–CANIDMR7 can be written only by the CPU when the MSCAN is in initialization mode.<br>0 Running — The MSCAN operates normally<br>1 Initialization mode active — The MSCAN has entered initialization mode |

### 14.3.2.3 MSCAN Bus Timing Register 0 (CANBTR0)

The CANBTR0 register configures various CAN bus timing parameters of the MSCAN module.

Module Base + 0x0002 — Access: User read/write(1)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 14-6. MSCAN Bus Timing Register 0 (CANBTR0)**

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

**Table 14-5. CANBTR0 Register Field Descriptions**

| Field | Description |
|---|---|
| 7-6<br>SJW[1:0] | **Synchronization Jump Width** — The synchronization jump width defines the maximum number of time quanta (Tq) clock cycles a bit can be shortened or lengthened to achieve resynchronization to data transitions on the CAN bus (see Table 14-6). |
| 5-0<br>BRP[5:0] | **Baud Rate Prescaler** — These bits determine the time quanta (Tq) clock which is used to build up the bit timing (see Table 14-7). |

**Table 14-6. Synchronization Jump Width**

| SJW1 | SJW0 | Synchronization Jump Width |
|---|---|---|
| 0 | 0 | 1 Tq clock cycle |
| 0 | 1 | 2 Tq clock cycles |
| 1 | 0 | 3 Tq clock cycles |
| 1 | 1 | 4 Tq clock cycles |

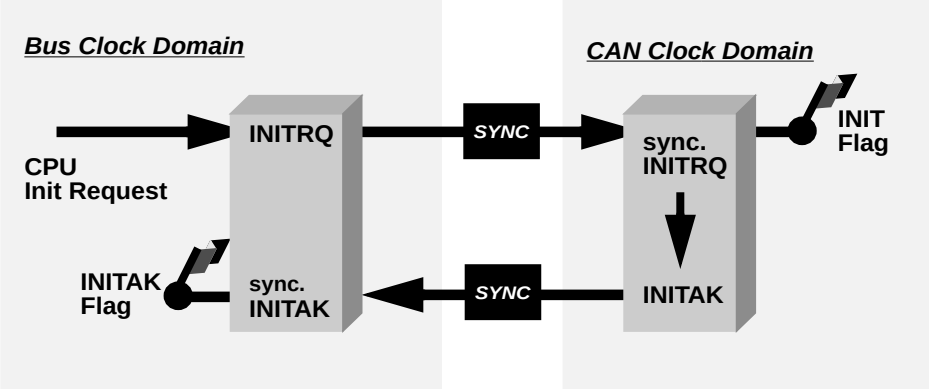



**Figure 14-45. Initialization Request/Acknowledge Cycle**

Due to independent clock domains within the MSCAN, INITRQ must be synchronized to all domains by using a special handshake mechanism. This handshake causes additional synchronization delay (see Figure 14-45).

If there is no message transfer ongoing on the CAN bus, the minimum delay will be two additional bus clocks and three additional CAN clocks. When all parts of the MSCAN are in initialization mode, the INITAK flag is set. The application software must use INITAK as a handshake indication for the request (INITRQ) to go into initialization mode.

**NOTE**

The CPU cannot clear INITRQ before initialization mode (INITRQ = 1 and INITAK = 1) is active.

## 14.4.5 Low-Power Options

If the MSCAN is disabled (CANE = 0), the MSCAN clocks are stopped for power saving.

If the MSCAN is enabled (CANE = 1), the MSCAN has two additional modes with reduced power consumption, compared to normal mode: sleep and power down mode. In sleep mode, power consumption is reduced by stopping all clocks except those to access the registers from the CPU side. In power down mode, all clocks are stopped and no power is consumed.

Table 14-38 summarizes the combinations of MSCAN and CPU modes. A particular combination of modes is entered by the given settings on the CSWAI and SLPRQ/SLPAK bits.

### 17.3.0.4 PIT Multiplex Register (PITMUX)

Module Base + 0x0003

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PMUX3 | PMUX2 | PMUX1 | PMUX0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 17-6. PIT Multiplex Register (PITMUX)**

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

**Table 17-4. PITMUX Field Descriptions**

| Field | Description |
|---|---|
| 3:0<br>PMUX[3:0] | **PIT Multiplex Bits for Timer Channel 3:0** — These bits select if the corresponding 16-bit timer is connected to micro time base 1 or 0. If PMUX is modified, the corresponding 16-bit timer is immediately switched to the other micro time base.<br>0 The corresponding 16-bit timer counts with micro time base 0.<br>1 The corresponding 16-bit timer counts with micro time base 1. |

### 17.3.0.5 PIT Interrupt Enable Register (PITINTE)

Module Base + 0x0004

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PINTE3 | PINTE2 | PINTE1 | PINTE0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 17-7. PIT Interrupt Enable Register (PITINTE)**

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

**Table 17-5. PITINTE Field Descriptions**

| Field | Description |
|---|---|
| 3:0<br>PINTE[3:0] | **PIT Time-out Interrupt Enable Bits for Timer Channel 3:0** — These bits enable an interrupt service request whenever the time-out flag PTF of the corresponding PIT channel is set. When an interrupt is pending (PTF set) enabling the interrupt will immediately cause an interrupt. To avoid this, the corresponding PTF flag has to be cleared first.<br>0 Interrupt of the corresponding PIT channel is disabled.<br>1 Interrupt of the corresponding PIT channel is enabled. |

### 19.3.2.16 Pulse Accumulator A Flag Register (PAFLG)

Module Base + 0x0021

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | PAOVF | PAIF |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 19-37. Pulse Accumulator A Flag Register (PAFLG)**

Read: Anytime

Write used in the flag clearing mechanism. Writing a one to the flag clears the flag. Writing a zero will not affect the current status of the bit.

**NOTE**

When TFFCA = 1, the flags cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference Section 19.3.2.6, “Timer System Control Register 1 (TSCR1)”.

All bits reset to zero.

PAFLG indicates when interrupt conditions have occurred. The flags can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (Reference TFFCA bit in Section 19.3.2.6, “Timer System Control Register 1 (TSCR1)”).

**Table 19-22. PAFLG Field Descriptions**

| Field | Description |
|---|---|
| 1<br>PAOVF | **Pulse Accumulator A Overflow Flag** — Set when the 16-bit pulse accumulator A overflows from 0xFFFF to 0x0000, or when 8-bit pulse accumulator 3 (PAC3) overflows from 0x00FF to 0x0000.<br>When PACMX = 1, PAOVF bit can also be set if 8-bit pulse accumulator 3 (PAC3) reaches 0x00FF followed by an active edge on IC3. |
| 0<br>PAIF | **Pulse Accumulator Input edge Flag** — Set when the selected edge is detected at the IC7 input pin. In event mode the event edge triggers PAIF and in gated time accumulation mode the trailing edge of the gate signal at the IC7 input pin triggers PAIF. |

### 19.3.2.17 Pulse Accumulators Count Registers (PACN3 and PACN2)

Module Base + 0x0022

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PACNT7(15) | PACNT6(14) | PACNT5(13) | PACNT4(12) | PACNT3(11) | PACNT2(10) | PACNT1(9) | PACNT0(8) |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 19-38. Pulse Accumulators Count Register 3 (PACN3)**

2 data entries, thus in this case the DBGCNT[0] is incremented after each separate entry. In Detail mode DBGCNT[0] remains cleared whilst the other DBGCNT bits are incremented on each trace buffer entry.

XGATE and CPU12X COFs occur independently of each other and the profile of COFs for the two sources is totally different. When both sources are being traced in Normal or Loop1 mode, for each COF from one source, there may be many COFs from the other source, depending on user code. COF events could occur far from each other in the time domain, on consecutive cycles or simultaneously. When a COF occurs in either source (S12X or XGATE) a trace buffer entry is made and the corresponding CDV or XDV bit is set. The current PC of the other source is simultaneously stored to the trace buffer even if no COF has occurred, in which case CDV/XDV remains cleared indicating the address is not associated with a COF, but is simply a snapshot of the PC contents at the time of the COF from the other source.

Single byte data accesses in Detail Mode are always stored to the low byte of the trace buffer (CDATAL or XDATAL) and the high byte is cleared. When tracing word accesses, the byte at the lower address is always stored to trace buffer byte3 and the byte at the higher address is stored to byte2

**Table 22-43. Trace Buffer Organization**

| Mode | 8-Byte Wide Word Buffer | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XGATE Detail | CXINF1 | CADRH1 | CADRM1 | CADRL1 | XDATAH1 | XDATAL1 | XADRM1 | XADRL1 |
| | CXINF2 | CADRH2 | CADRM2 | CADRL2 | XDATAH2 | XDATAL2 | XADRM2 | XADRL2 |
| CPU12X Detail | CXINF1 | CADRH1 | CADRM1 | CADRL1 | CDATAH1 | CDATAL1 | XADRM1 | XADRL1 |
| | CXINF2 | CADRH2 | CADRM2 | CADRL2 | CDATAH2 | CDATAL2 | XADRM2 | XADRL2 |
| Both Other Modes | XINF0 | | XPCM0 | XPCL0 | CINF0 | CPCH0 | CPCM0 | CPCL0 |
| | XINF1 | | XPCM1 | XPCL1 | CINF1 | CPCH1 | CPCM1 | CPCL1 |
| XGATE Other Modes | XINF1 | | XPCM1 | XPCL1 | XINF0 | | XPCM0 | XPCL0 |
| | XINF3 | | XPCM3 | XPCL3 | XINF2 | | XPCM2 | XPCL2 |
| CPU12X Other Modes | CINF1 | CPCH1 | CPCM1 | CPCL1 | CINF0 | CPCH0 | CPCM0 | CPCL0 |
| | CINF3 | CPCH3 | CPCM3 | CPCL3 | CINF2 | CPCH2 | CPCM2 | CPCL2 |

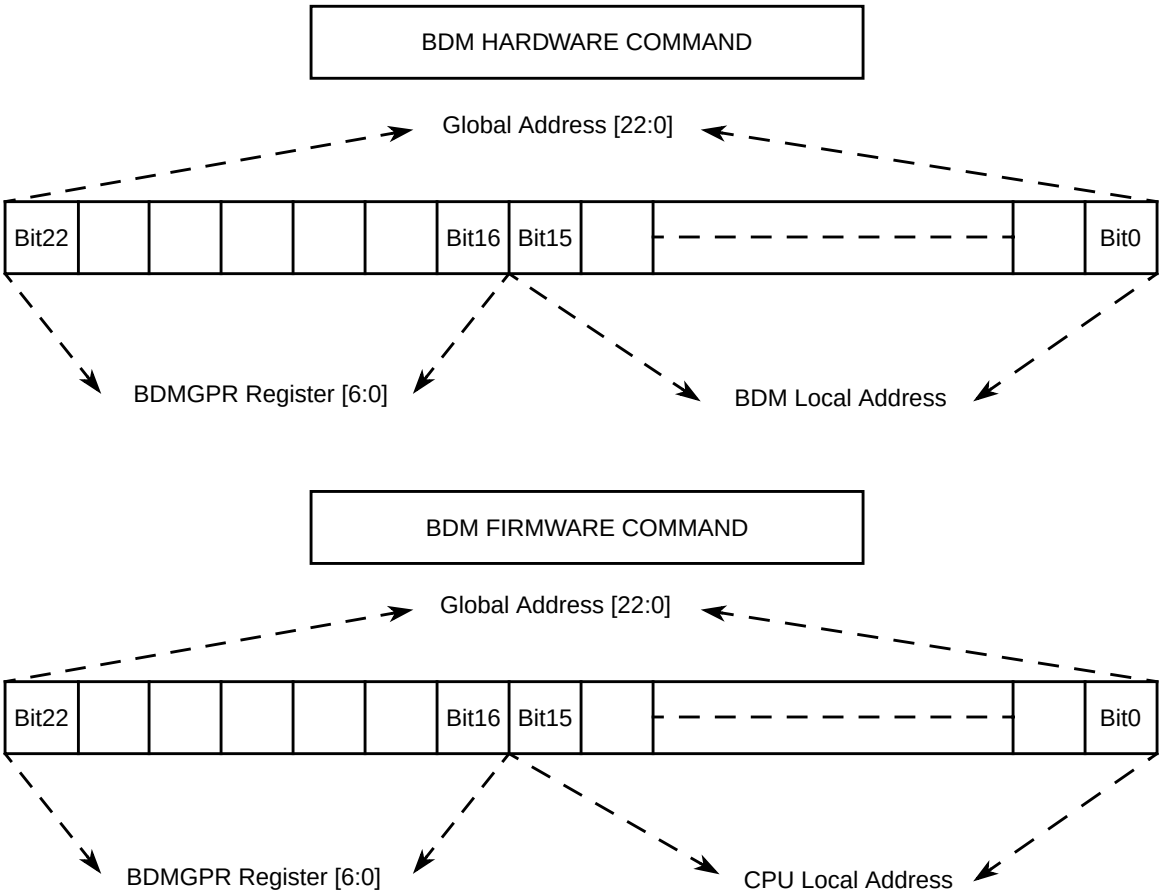



**Figure 25-22. BDMGPR Address Mapping**

## 25.4.3 Chip Access Restrictions

### 25.4.3.1 Illegal XGATE Accesses

A possible access error is flagged by the MMC and signalled to XGATE under the following conditions:

- XGATE performs misaligned word (in case of load-store or opcode or vector fetch accesses).
- XGATE accesses the register space (in case of opcode or vector fetch).
- XGATE performs a write to Flash in any modes (in case of load-store access).
- XGATE performs an access to a secured Flash in expanded modes (in case of load-store or opcode or vector fetch accesses).
- XGATE performs an access to an unimplemented area (in case of load-store or opcode or vector fetch accesses).
- XGATE performs a write to non-XGATE region in RAM (RAM protection mechanism) (in case of load-store access).

For further details refer to the XGATE Block Guide.

### 25.4.3.2 Illegal CPU Accesses

After programming the protection mechanism registers (see Figure 25-17, Figure 25-18, Figure 25-19, and Figure 25-20) and setting the RWPE bit (see Figure 25-17) there are 3 regions recognized by the MMC module:

1. XGATE RAM region
2. CPU RAM region
3. Shared Region (XGATE AND CPU)

If the RWPE bit is set the CPU write accesses into the XGATE RAM region are blocked. If the CPU tries to write the XGATE RAM region the AVIF bit is set and an interrupt is generated if enabled. Furthermore if the XGATE tries to write to outside of the XGATE RAM or shared regions and the RWPE bit is set, the write access is suppressed and the access error will be flagged to the XGATE module (see Section 25.4.3.1, “Illegal XGATE Accesses and the XGATE Block Guide).

The bottom address of the XGATE RAM region always starts at the lowest implemented RAM address.

The values stored in the boundary registers define the boundary addresses in 256 byte steps. The 256 byte block selected by any of the registers is always included in the respective region. For example setting the shared region lower boundary register (RAMSHL) to 0xC1 and the shared region upper boundary register (RAMSHU) to 0xE0 defines the shared region from address 0x0F_C100 to address 0x0F_E0FF in the global memory space (see Figure 25-20).

The interrupt requests generated by the MMC are listed in Table 25-23. Refer to the Device User Guide for the related interrupt vector address and interrupt priority.

The following conditions must be satisfied to ensure correct operation of the RAM protection mechanism:

- Value stored in RAMXGU must be lower than the value stored in RAMSHL.
- Value stored RAMSHL must be lower or equal than the value stored in RAMSHU.

## A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table A-2. ESD and Latch-up Test Conditions**

| Model | Description | Symbol | Value | Unit |
|---|---|---|---|---|
| Human Body | Series resistance | R1 | 1500 | Ohm |
| | Storage capacitance | C | 100 | pF |
| | Number of pulse per pin<br>Positive<br>Negative | <br>—<br>— | <br>3<br>3 | |
| Latch-up | Minimum input voltage limit | | –2.5 | V |
| | Maximum input voltage limit | | 7.5 | V |

**Table A-3. ESD and Latch-Up Protection Characteristics**

| Num | C | Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | C | Human Body Model (HBM) | $V_{HBM}$ | 2000 | — | V |
| 2 | C | Charge Device Model (CDM) | $V_{CDM}$ | 500 | — | V |
| 3 | C | Latch-up current at $T_A$ = 125°C<br>Positive<br>Negative | $I_{LAT}$ | <br>+100<br>–100 | <br>—<br>— | mA |
| 4 | C | Latch-up current at $T_A$ = 27°C<br>Positive<br>Negative | $I_{LAT}$ | <br>+200<br>–200 | <br>—<br>— | mA |

## 0x000E–0x000F External Bus Interface (S12XEBI) Map

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x000E | EBICTL0 | R | ITHRS | 0 | HDBE | ASIZ4 | ASIZ3 | ASIZ2 | ASIZ1 | ASIZ0 |
| | | W | | | | | | | | |
| 0x000F | EBICTL1 | R | EWAITE | 0 | 0 | 0 | 0 | EXSTR2 | EXSTR1 | EXSTR0 |
| | | W | | | | | | | | |

## 0x0010–0x0017 Module Mapping Control (S12XMMC) Map 2 of 4

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0010 | GPAGE | R | 0 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| | | W | | | | | | | | |
| 0x0011 | DIRECT | R | DP15 | DP14 | DP13 | DP12 | DP11 | DP10 | DP9 | DP8 |
| | | W | | | | | | | | |
| 0x0012 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0013 | MMCCTL1 | R | 0 | 0 | 0 | 0 | 0 | EROMON | ROMHM | ROMON |
| | | W | | | | | | | | |
| 0x0014 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0015 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0016 | RPAGE | R | RP7 | RP6 | RP5 | RP4 | RP3 | RP2 | RP1 | RP0 |
| | | W | | | | | | | | |
| 0x0017 | EPAGE | R | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 |
| | | W | | | | | | | | |

## 0x0018–0x001B Miscellaneous Peripheral

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0018 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0019 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x001A | PARTIDH | R | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| | | W | | | | | | | | |
| 0x001B | PARTIDL | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |

## 0x001C–0x001F Port Integration Module (PIM) Map 3 of 5

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x001C | ECLKCTL | R | NECLK | NCLKX2 | 0 | 0 | 0 | 0 | EDIV1 | EDIV0 |
| | | W | | | | | | | | |