Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12xhz512cal

2.3.6.6 Port AD Polarity Select Register (PPSAD)

Module Base + 0x005B

	7	6	5	4	3	2	1	0
R W	PPSAD7	PPSAD6	PPSAD5	PPSAD4	PPSAD3	PPSAD2	PPSAD1	PPSAD0
Reset	0	0	0	0	0	0	0	0

Figure 2-24. Port AD Polarity Select Register (PPSAD)

Read: Anytime. Write: Anytime.

The Port AD Polarity Select Register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled (PERADx = 1). The Port AD Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input).

In pull-down mode (PPSADx = 1), a rising edge on a port AD pin sets the corresponding PIFADx bit. In pull-up mode (PPSADx = 0), a falling edge on a port AD pin sets the corresponding PIFADx bit.

Table 2-18. PPSAD Field Descriptions

Field	Description
7:0 PPSAD[7:0]	**Polarity Select Port AD** 0 A pull-up device is connected to the associated port AD pin, and detects falling edge for interrupt generation. 1 A pull-down device is connected to the associated port AD pin, and detects rising edge for interrupt generation.

2.3.6.7 Port AD Interrupt Enable Register (PIEAD)

Module Base + 0x005D

	7	6	5	4	3	2	1	0
R W	PIEAD7	PIEAD6	PIEAD5	PIEAD4	PIEAD3	PIEAD2	PIEAD1	PIEAD0
Reset	0	0	0	0	0	0	0	0

Figure 2-25. Port AD Interrupt Enable Register (PIEAD)

Read: Anytime. Write: Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port AD.

Table 2-19. PIEAD Field Descriptions

Field	Description
7:0 PIEAD[7:0]	**Interrupt Enable Port AD** 0 Interrupt is disabled (interrupt flag masked). 1 Interrupt is enabled.

2.3.10.4 Port S Reduced Drive Register (RDRS)

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
Reset	0	0	0	0	0	0	0	0

Figure 2-53. Port S Reduced Drive Register (RDRS)

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

Table 2-39. RDRS Field Descriptions

Field	Description
7:0 RDRS[7:0]	**Reduced Drive Port S** 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

2.3.10.5 Port S Pull Device Enable Register (PERS)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R W	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
Reset	0	0	0	0	0	0	0	0

Figure 2-54. Port S Pull Device Enable Register (PERS)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input or wired-or (open drain) output pins. If a pin is configured as push-pull output, the corresponding Pull Device Enable Register bit has no effect.

Table 2-40. PERS Field Descriptions

Field	Description
7:0 PERS[7:0]	**Pull Device Enable Port S** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

2.4.4 Reduced Drive Register

If the port is used as an output the Reduced Drive Register allows the configuration of the drive strength.

2.4.5 Pull Device Enable Register

The Pull Device Enable Register turns on a pull-up or pull-down device. The pull device becomes active only if the pin is used as an input or as a wired-or output.

2.4.6 Polarity Select Register

The Polarity Select Register selects either a pull-up or pull-down device if enabled. The pull device becomes active only if the pin is used as an input or as a wired-or output.

2.4.7 Pin Configuration Summary

The following table summarizes the effect of various configuration in the Data Direction (DDR), Input/Output (I/O), reduced drive (RDR), Pull Enable (PE), Pull Select (PS) and Interrupt Enable (IE) register bits. The PS configuration bit is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is set to “1”.

Table 2-66. Pin Configuration Summary

DDR	IO	RDR	PE	PS	IE[1]	Function[2]	Pull Device	Interrupt
0	X	X	0	X	0	Input	Disabled	Disabled
0	X	X	1	0	0	Input	Pull Up	Disabled
0	X	X	1	1	0	Input	Pull Down	Disabled
0	X	X	0	0	1	Input	Disabled	Falling Edge
0	X	X	0	1	1	Input	Disabled	Rising Edge
0	X	X	1	0	1	Input	Pull Up	Falling Edge
0	X	X	1	1	1	Input	Pull Down	Rising Edge
1	0	0	X	X	0	Output to 0, Full Drive	Disabled	Disabled
1	1	0	X	X	0	Output to 1, Full Drive	Disabled	Disabled
1	0	1	X	X	0	Output to 0, Reduced Drive	Disabled	Disabled
1	1	1	X	X	0	Output to 1, Reduced Drive	Disabled	Disabled
1	0	0	X	0	1	Output to 0, Full Drive	Disabled	Falling Edge
1	1	0	X	1	1	Output to 1, Full Drive	Disabled	Rising Edge
1	0	1	X	0	1	Output to 0, Reduced Drive	Disabled	Falling Edge
1	1	1	X	1	1	Output to 1, Reduced Drive	Disabled	Rising Edge

1 Applicable only on Port AD.

2 Digital outputs are disabled and digital input logic is forced to “1” when an analog module associated with the port is enabled.

Table 4-5. EEPROM Protection Address Range

EPS[2:0]	Address Offset Range	Protected Size
000	0x0FC0 – 0x0FFF	64 bytes
001	0x0F80 – 0x0FFF	128 bytes
010	0x0F40 – 0x0FFF	192 bytes
011	0x0F00 – 0x0FFF	256 bytes
100	0x0EC0 – 0x0FFF	320 bytes
101	0x0E80 – 0x0FFF	384 bytes
110	0x0E40 – 0x0FFF	448 bytes
111	0x0E00 – 0x0FFF	512 bytes

4.3.2.6 EEPROM Status Register (ESTAT)

The ESTAT register defines the operational status of the module.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
W								
Reset	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-9. EEPROM Status Register (ESTAT — Normal Mode)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	FAIL	0
W								
Reset	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-10. EEPROM Status Register (ESTAT — Special Mode)

CBEIF, PVIOL, and ACCERR are readable and writable, CCIF and BLANK are readable and not writable, remaining bits read 0 and are not writable in normal mode. FAIL is readable and writable in special mode.

then ECLKDIV register bits PRDIV8 and EDIV[5:0] are to be set as described in Figure 4-17.

For example, if the oscillator clock frequency is 950 kHz and the bus clock frequency is 10 MHz, ECLKDIV bits EDIV[5:0] should be set to 0x04 (000100) and bit PRDIV8 set to 0. The resulting EECLK frequency is then 190 kHz. As a result, the EEPROM program and erase algorithm timings are increased over the optimum target by:

$$(200 - 190) / 200 \times 100 = 5\%$$

If the oscillator clock frequency is 16 MHz and the bus clock frequency is 40 MHz, ECLKDIV bits EDIV[5:0] should be set to 0x0A (001010) and bit PRDIV8 set to 1. The resulting EECLK frequency is then 182 kHz. In this case, the EEPROM program and erase algorithm timings are increased over the optimum target by:

$$(200 - 182) / 200 \times 100 = 9\%$$

CAUTION

Program and erase command execution time will increase proportionally with the period of EECLK. Because of the impact of clock synchronization on the accuracy of the functional timings, programming or erasing the EEPROM memory cannot be performed if the bus clock runs at less than 1 MHz. Programming or erasing the EEPROM memory with EECLK < 150 kHz should be avoided. Setting ECLKDIV to a value such that EECLK < 150 kHz can destroy the EEPROM memory due to overstress. Setting ECLKDIV to a value such that (1/EECLK+Tbus) < 5 µs can result in incomplete programming or erasure of the EEPROM memory cells.

If the ECLKDIV register is written, the EDIVLD bit is set automatically. If the EDIVLD bit is 0, the ECLKDIV register has not been written since the last reset. If the ECLKDIV register has not been written to, the EEPROM command loaded during a command write sequence will not execute and the ACCERR flag in the ESTAT register will set.

TFR Transfer from and to Special Registers TFR

Operation

TFR RD,CCR: CCR ⇒ RD[3:0]; 0 ⇒ RD[15:4]
TFR CCR,RD: RD[3:0] ⇒ CCR
TFR RD,PC: PC+4 ⇒ RD

Transfers the content of one RISC core register to another.
The TFR RD,PC instruction can be used to implement relative subroutine calls.

Example:

```
        TFR     R7,PC    ;Return address (RETADDR) is stored in R7
        BRA     SUBR     ;Relative branch to subroutine (SUBR)
RETADDR ...

SUBR    ...
        JAL     R7       ;Jump to return address (RETADDR)
```

CCR Effects

TFR RD,CCR, TFR RD,PC:

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

TFR CCR,RS:

N	Z	V	C
Δ	Δ	Δ	Δ

N: RS[3].
Z: RS[2].
V: RS[1].
C: RS[0].

Code and CPU Cycles

Source Form	Address Mode	Machine Code														Cycles
TFR RD,CCR CCR ⇒ RD	MON	0	0	0	0	0	RD	1	1	1	1	1	0	0	0	P
TFR CCR,RS RS ⇒ CCR	MON	0	0	0	0	0	RS	1	1	1	1	1	0	0	1	P
TFR RD,PCPC+4 ⇒ RD	MON	0	0	0	0	0	RD	1	1	1	1	1	0	1	0	P

under software control. Depending on the state of internal bits, the LCD can operate normally or the LCD clock generation can be turned off and the LCD32F4BV1 module enters a power conservation state.

This is a high level description only, detailed descriptions of operating modes are contained in Section 10.4.2, “Operation in Wait Mode”, Section 10.4.3, “Operation in Pseudo Stop Mode”, and Section 10.4.4, “Operation in Stop Mode”.

10.1.3 Block Diagram

Figure 10-1 is a block diagram of the LCD32F4BV1 module.

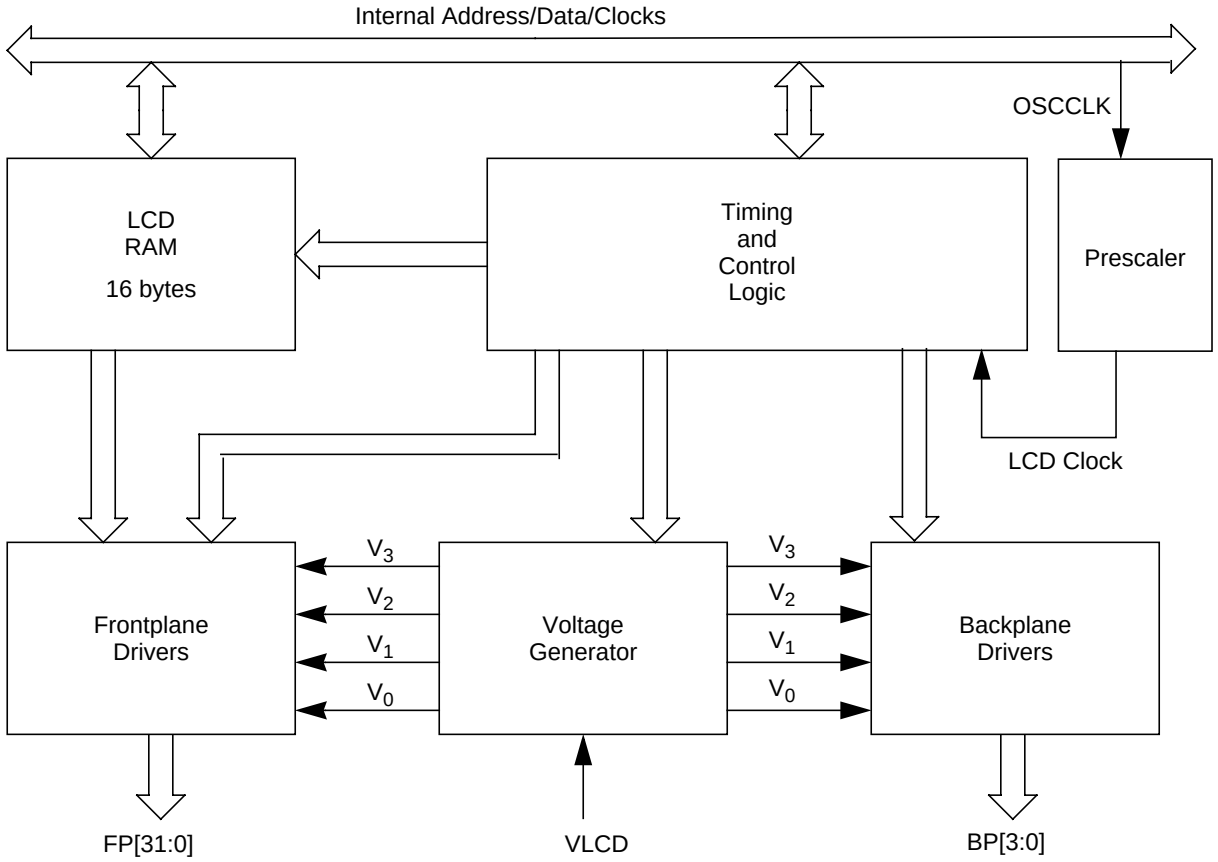

Figure 10-1. LCD32F4BV1 Block Diagram

10.4.5.3 1/2 Duty Multiplexed with 1/3 Bias Mode

Duty = 1/2:DUTY1 = 1, DUTY0 = 0

Bias = 1/3:BIAS = 1

V_0 = VSSX, V_1 = VLCD * 1/3, V_2 = VLCD * 2/3, V_3 = VLCD

- BP2 and BP3 are not used, a maximum of 64 segments are displayed.

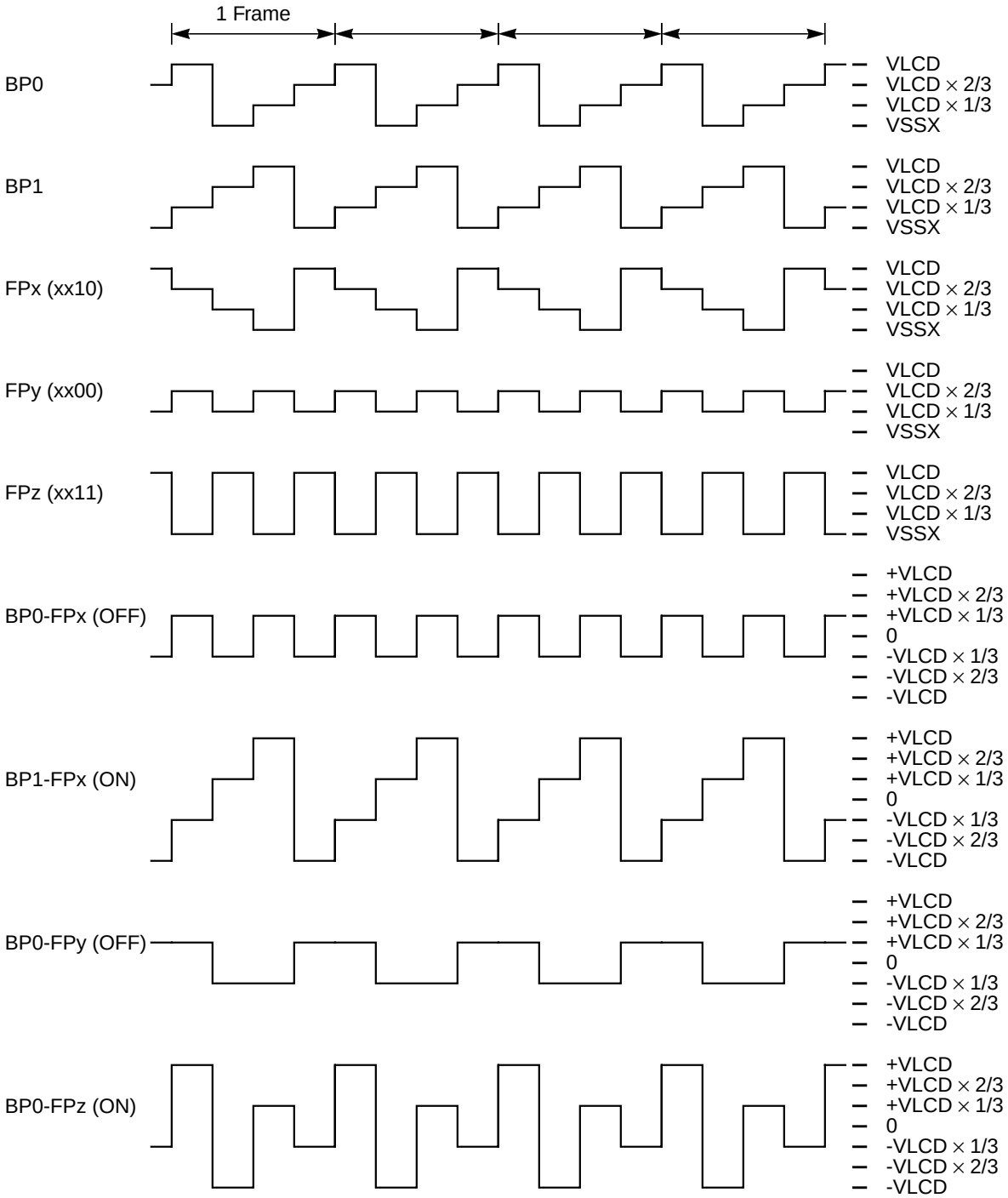

Figure 10-11. 1/2 Duty and 1/3 Bias

Chapter 11
Motor Controller (MC10B12CV2) Block Description

11.1 Introduction

The block MC10B12C is a PWM motor controller suitable to drive instruments in a cluster configuration or any other loads requiring a PWM signal. The motor controller has twelve PWM channels associated with two pins each (24 pins in total).

11.1.1 Features

The MC_10B12C includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- 7-bit resolution mode (fast mode): duty cycle can be changed by accessing only 1 byte/output
- Left, right, or center aligned PWM
- Output slew rate control
- This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module.

11.1.2 Modes of Operation

11.1.2.1 Functional Modes

11.1.2.1.1 PWM Resolution

The motor controller can be configured to either 11- or 7-bits resolution mode by clearing or setting the FAST bit. This bit influences all PWM channels. For details, please refer to Section 11.3.2.5, “Motor Controller Duty Cycle Registers”.

11.1.2.1.2 Dither Function

Dither function can be selected or deselected by setting or clearing the DITH bit. This bit influences all PWM channels. For details, please refer to Section 11.4.1.3.5, “Dither Bit (DITH)”.

11.2.2 M1C0M/M1C0P/M1C1M/M1C1P — PWM Output Pins for Motor 1

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 1. PWM output on M1C0M results in a positive current flow through coil 0 when M1C0P is driven to a logic high state. PWM output on M1C1M results in a positive current flow through coil 1 when M1C1P is driven to a logic high state.

11.2.3 M2C0M/M2C0P/M2C1M/M2C1P — PWM Output Pins for Motor 2

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 2. PWM output on M2C0M results in a positive current flow through coil 0 when M2C0P is driven to a logic high state. PWM output on M2C1M results in a positive current flow through coil 1 when M2C1P is driven to a logic high state.

11.2.4 M3C0M/M3C0P/M3C1M/M3C1P — PWM Output Pins for Motor 3

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 3. PWM output on M3C0M results in a positive current flow through coil 0 when M3C0P is driven to a logic high state. PWM output on M3C1M results in a positive current flow through coil 1 when M3C1P is driven to a logic high state.

11.2.5 M4C0M/M4C0P/M4C1M/M4C1P — PWM Output Pins for Motor 4

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 4. PWM output on M4C0M results in a positive current flow through coil 0 when M4C0P is driven to a logic high state. PWM output on M4C1M results in a positive current flow through coil 1 when M4C1P is driven to a logic high state.

11.2.6 M5C0M/M5C0P/M5C1M/M5C1P — PWM Output Pins for Motor 5

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 5. PWM output on M5C0M results in a positive current flow through coil 0 when M5C0P is driven to a logic high state. PWM output on M5C1M results in a positive current flow through coil 1 when M5C1P is driven to a logic high state.

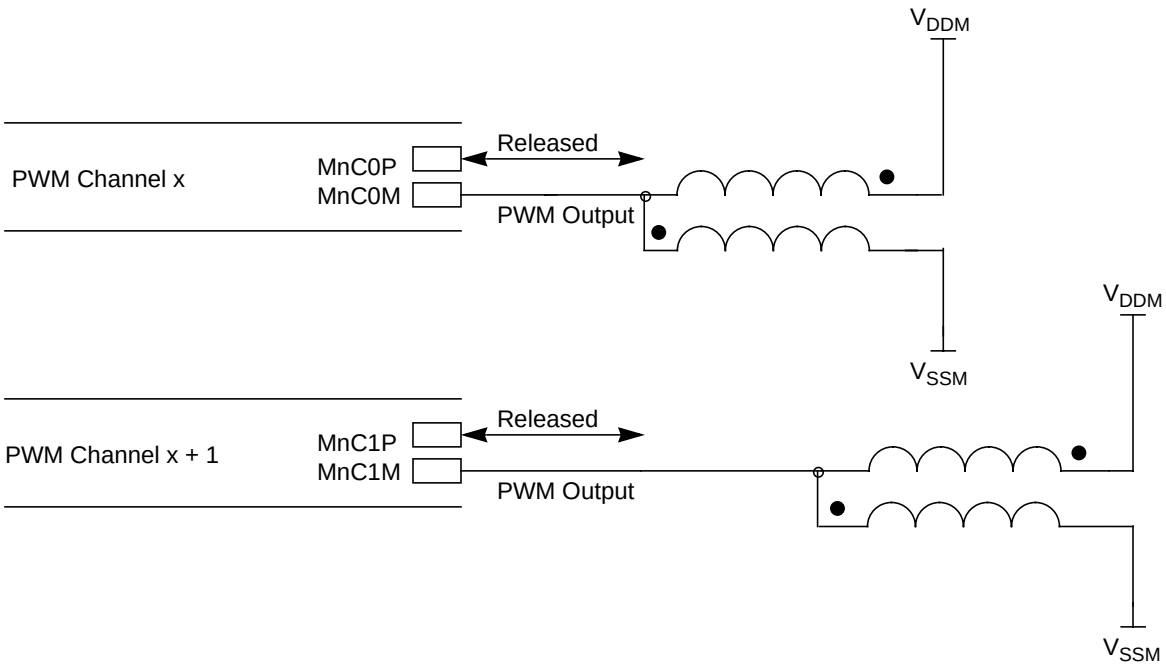

Figure 11-11. Typical Quad Half H-Bridge Mode Configuration

11.4.1.2 Relationship Between PWM Mode and PWM Channel Enable

The pair of motor controller channels cannot be placed into dual full H-bridge mode unless both motor controller channels have been enabled (MCAM[1:0] not equal to 00) and dual full H-bridge mode is selected for both PWM channels (MCOM[1:0] = 11). If only one channel is set to dual full H-bridge mode, this channel will operate in full H-bridge mode, the other as programmed.

11.4.1.3 Relationship Between Sign, Duty, Dither, RECIRC, Period, and PWM Mode Functions

11.4.1.3.1 PWM Alignment Modes

Each PWM channel can be programmed individually to three different alignment modes. The mode is determined by the MCAM[1:0] bits in the corresponding channel control register.

Left aligned (MCAM[1:0] = 01): The output will start active (low if RECIRC = 0 or high if RECIRC = 1) and will turn inactive (high if RECIRC = 0 or low if RECIRC = 1) after the number of counts specified by the corresponding duty cycle register.

15.3.2.5 SCI Alternative Control Register 2 (SCIACR2)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	BERRM1	BERRM0	BKDFE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-8. SCI Alternative Control Register 2 (SCIACR2)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 15-8. SCIACR2 Field Descriptions

Field	Description
2:1 BERRM[1:0]	**Bit Error Mode** — Those two bits determines the functionality of the bit error detect feature. See Table 15-9.
0 BKDFE	**Break Detect Feature Enable** — BKDFE enables the break detect circuitry. 0 Break detect circuit disabled 1 Break detect circuit enabled

Table 15-9. Bit Error Mode Coding

BERRM1	BERRM0	Function
0	0	Bit error detect circuit is disabled
0	1	Receive input sampling occurs during the 9th time tick of a transmitted bit (refer to Figure 15-19)
1	0	Receive input sampling occurs during the 13th time tick of a transmitted bit (refer to Figure 15-19)
1	1	Reserved

15.4.6.5 Baud Rate Tolerance

A transmitting device may be operating at a baud rate below or above the receiver baud rate. Accumulated bit time misalignment can cause one of the three stop bit data samples (RT8, RT9, and RT10) to fall outside the actual stop bit. A noise error will occur if the RT8, RT9, and RT10 samples are not all the same logical values. A framing error will occur if the receiver clock is misaligned in such a way that the majority of the RT8, RT9, and RT10 stop bit samples are a logic zero.

As the receiver samples an incoming frame, it re-synchronizes the RT clock on any valid falling edge within the frame. Re synchronization within frames will correct a misalignment between transmitter bit times and receiver bit times.

15.4.6.5.1 Slow Data Tolerance

Figure 15-28 shows how much a slow received frame can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

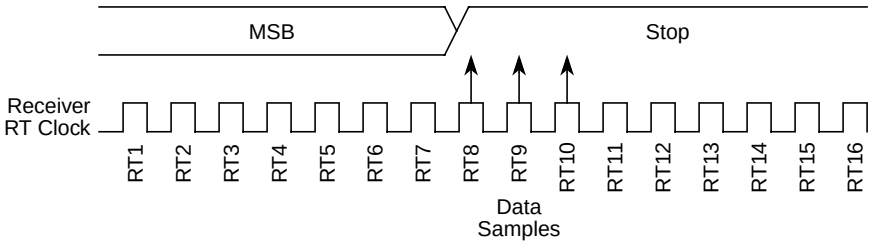

Figure 15-28. Slow Data

Let’s take RTr as receiver RT clock and RTt as transmitter RT clock.

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles +7 RTr cycles = 151 RTr cycles to start data sampling of the stop bit.

With the misaligned character shown in Figure 15-28, the receiver counts 151 RTr cycles at the point when the count of the transmitting device is 9 bit times x 16 RTt cycles = 144 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit data character with no errors is:

((151 – 144) / 151) x 100 = 4.63%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 7 RTr cycles = 167 RTr cycles to start data sampling of the stop bit.

With the misaligned character shown in Figure 15-28, the receiver counts 167 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is:

((167 – 160) / 167) X 100 = 4.19%

15.5.3.1.6 RXEDGIF Description

The RXEDGIF interrupt is set when an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD pin is detected. Clear RXEDGIF by writing a “1” to the SCIASR1 SCI alternative status register 1.

15.5.3.1.7 BERRIF Description

The BERRIF interrupt is set when a mismatch between the transmitted and the received data in a single wire application like LIN was detected. Clear BERRIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if the bit error detect feature is disabled.

15.5.3.1.8 BKDIF Description

The BKDIF interrupt is set when a break signal was received. Clear BKDIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if break detect feature is disabled.

15.5.4 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

15.5.5 Recovery from Stop Mode

An active edge on the receive input can be used to bring the CPU out of stop mode.

17.3.0.1 PIT Control and Force Load Micro Timer Register (PITCFLMT)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	PITE	PITSWAI	PITFRZ	0	0	0	0	0
W							PFLMT1	PFLMT0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-3. PIT Control and Force Load Micro Timer Register (PITCFLMT)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Table 17-1. PITCFLMT Field Descriptions

Field	Description
7 PITE	**PIT Module Enable Bit** — This bit enables the PIT module. If PITE is cleared, the PIT module is disabled and flag bits in the PITTF register are cleared. When PITE is set, individually enabled timers (PCE set) start down-counting with the corresponding load register values. 0 PIT disabled (lower power consumption). 1 PIT is enabled.
6 PITSWAI	**PIT Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode. 0 PIT operates normally in wait mode 1 PIT clock generation stops and freezes the PIT module when in wait mode
5 PITFRZ	**PIT Counter Freeze while in Freeze Mode Bit** — When during debugging a breakpoint (freeze mode) is encountered it is useful in many cases to freeze the PIT counters to avoid e.g. interrupt generation. The PITFRZ bit controls the PIT operation while in freeze mode. 0 PIT operates normally in freeze mode 1 PIT counters are stalled when in freeze mode
1:0 PFLMT[1:0]	**PIT Force Load Bits for Micro Timer 1:0** — These bits have only an effect if the corresponding micro timer is active and if the PIT module is enabled (PITE set). Writing a one into a PFLMT bit loads the corresponding 8-bit micro timer load register into the 8-bit micro timer down-counter. Writing a zero has no effect. Reading these bits will always return zero. **Note:** A micro timer force load affects all timer channels that use the corresponding micro time base.

Chapter 18
Pulse-Width Modulator (S12PWM8B8CV1)

18.1 Introduction

The PWM definition is based on the HC12 PWM definitions. It contains the basic features from the HC11 with some of the enhancements incorporated on the HC12: center aligned output mode and four available clock sources.The PWM module has eight channels with independent control of left and center aligned outputs on each channel.

Each of the eight channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs can be programmed as left aligned outputs or center aligned outputs.

18.1.1 Features

The PWM block includes these distinctive features:

- Eight independent PWM channels with programmable period and duty cycle
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches zero) or when the channel is disabled.
- Programmable center or left aligned outputs on individual channels
- Eight 8-bit channel or four 16-bit channel PWM resolution
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
- Programmable clock select logic
- Emergency shutdown

18.1.2 Modes of Operation

There is a software programmable option for low power consumption in wait mode that disables the input clock to the prescaler.

In freeze mode there is a software programmable option to disable the input clock to the prescaler. This is useful for emulation.

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 18.4.2.5, “Left Aligned Outputs” and Section 18.4.2.6, “Center Aligned Outputs” for more details).

Table 18-10. PWM Timer Counter Conditions

Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

18.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 18-19. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 18-19, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 18.4.2.3, “PWM Period and Duty”. The counter counts from 0 to the value in the period register – 1.

20.2 External Signal Description

Due to the nature of VREG_3V3 being a voltage regulator providing the chip internal power supply voltages, most signals are power supply signals connected to pads.

Table 20-1 shows all signals of VREG_3V3 associated with pins.

Table 20-1. Signal Properties

Name	Function	Reset State	Pull Up
V_{DDR}	Power input (positive supply)	—	—
V_{DDA}	Quiet input (positive supply)	—	—
V_{SSA}	Quiet input (ground)	—	—
V_{DD}	Primary output (positive supply)	—	—
V_{SS}	Primary output (ground)	—	—
V_{DDPLL}	Secondary output (positive supply)	—	—
V_{SSPLL}	Secondary output (ground)	—	—
V_{REGEN} (optional)	Optional Regulator Enable	—	—

NOTE

Check device level specification for connectivity of the signals.

20.2.1 VDDR — Regulator Power Input Pins

Signal V_{DDR} is the power input of VREG_3V3. All currents sourced into the regulator loads flow through this pin. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDR} and V_{SSR} (if V_{SSR} is not available V_{SS}) can smooth ripple on V_{DDR}.

For entering shutdown mode, pin V_{DDR} should also be tied to ground on devices without VREGEN pin.

20.2.2 VDDA, VSSA — Regulator Reference Supply Pins

Signals $V_{DDA}/V_{SSA,}$ which are supposed to be relatively quiet, are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDA} and V_{SSA} can further improve the quality of this supply.

20.2.3 VDD, VSS — Regulator Output1 (Core Logic) Pins

Signals V_{DD}/V_{SS} are the primary outputs of VREG_3V3 that provide the power supply for the core logic. These signals are connected to device pins to allow external decoupling capacitors (100 nF...220 nF, X7R ceramic).

In shutdown mode an external supply driving V_{DD}/V_{SS} can replace the voltage regulator.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x7FFF07	BDMCCRH	R	0	0	0	0	0	CCR10	CCR9	CCR8
		W								
0x7FFF08	BDMGPR	R	BGAE	BGP6	BGP5	BGP4	BGP3	BGP2	BGP1	BGP0
		W								
0x7FFF09	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x7FFF0A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x7FFF0B	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented, Reserved

= Implemented (do not alter)

X = Indeterminate

0 = Always read zero

Figure 21-2. BDM Register Summary (continued)

21.3.2.1 BDM Status Register (BDMSTS)

Register Global Address 0x7FFF01

	7	6	5	4	3	2	1	0
R	ENBDM	BDMACT	0	SDV	TRACE	CLKSW	UNSEC	0
W								
Reset								
Special Single-Chip Mode	0[1]	1	0	0	0	0	0[3]	0
Emulation Modes (if modes available)	1	0	0	0	0	1[2]	0	0
All Other Modes	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

= Implemented (do not alter)

0 = Always read zero

1 ENBDM is read as 1 by a debugging environment in special single chip mode when the device is not secured or secured but fully erased (non-volatile memory). This is because the ENBDM bit is set by the standard firmware before a BDM command can be fully transmitted and executed.

2 CLKSW is read as 1 by a debugging environment in emulation modes when the device is not secured and read as 0 when secured if emulation modes available.

3 UNSEC is read as 1 by a debugging environment in special single chip mode when the device is secured and fully erased, else it is 0 and can only be read if not secure (see also bit description).

Figure 21-3. BDM Status Register (BDMSTS)

Due to internal visibility of CPU accesses the CPU will be halted during XGATE or BDM access to any PRR. This rule applies also in normal modes to ensure that operation of the device is the same as in emulation modes.

A summary of PRR accesses:

- An aligned word access to a PRR will take 2 bus cycles.
- A misaligned word access to a PRRs will take 4 cycles. If one of the two bytes accessed by the misaligned word access is not a PRR, the access will take only 3 cycles.
- A byte access to a PRR will take 2 cycles.

Table 25-24. PRR Listing

PRR Name	PRR Local Address	PRR Location
PORTA	0x0000	PIM
PORTB	0x0001	PIM
DDRA	0x0002	PIM
DDRB	0x0003	PIM
PORTC	0x0004	PIM
PORTD	0x0005	PIM
DDRC	0x0006	PIM
DDRD	0x0007	PIM
PORTE	0x0008	PIM
DDRE	0x0009	PIM
MMCCTL0	0x000A	MMC
MODE	0x000B	MMC
PUCR	0x000C	PIM
RDRIV	0x000D	PIM
EBICTL0	0x000E	EBI
EBICTL1	0x000F	EBI
Reserved	0x0012	MMC
MMCCTL1	0x0013	MMC
ECLKCTL	0x001C	PIM
Reserved	0x001D	PIM
PORTK	0x0032	PIM
DDRK	0x0033	PIM