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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	HCS12X
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	117
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	28K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xhz384f1vag

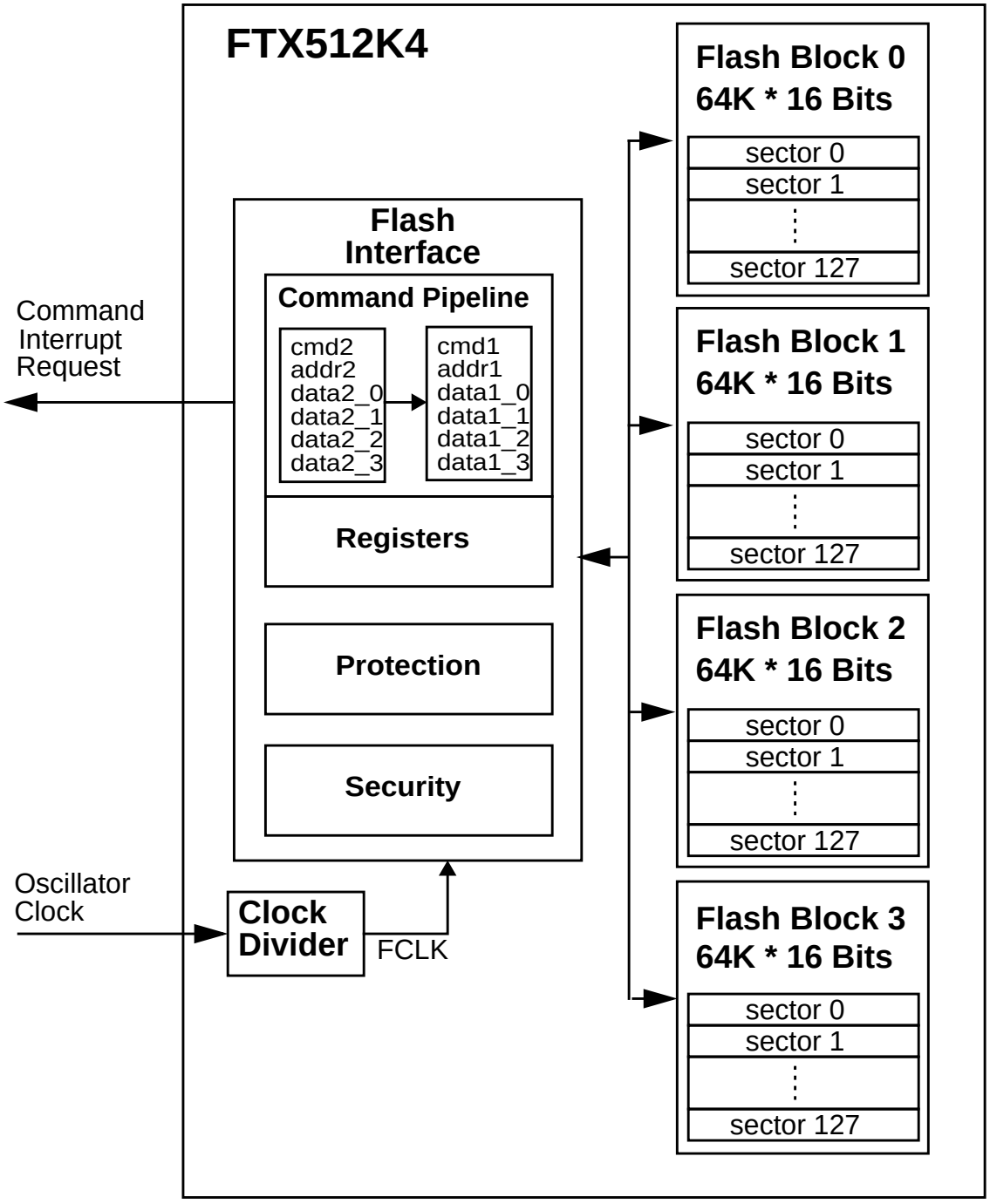

Figure 3-1. FTX512K4 Block Diagram

3.2 External Signal Description

The Flash module contains no signals that connect off-chip.

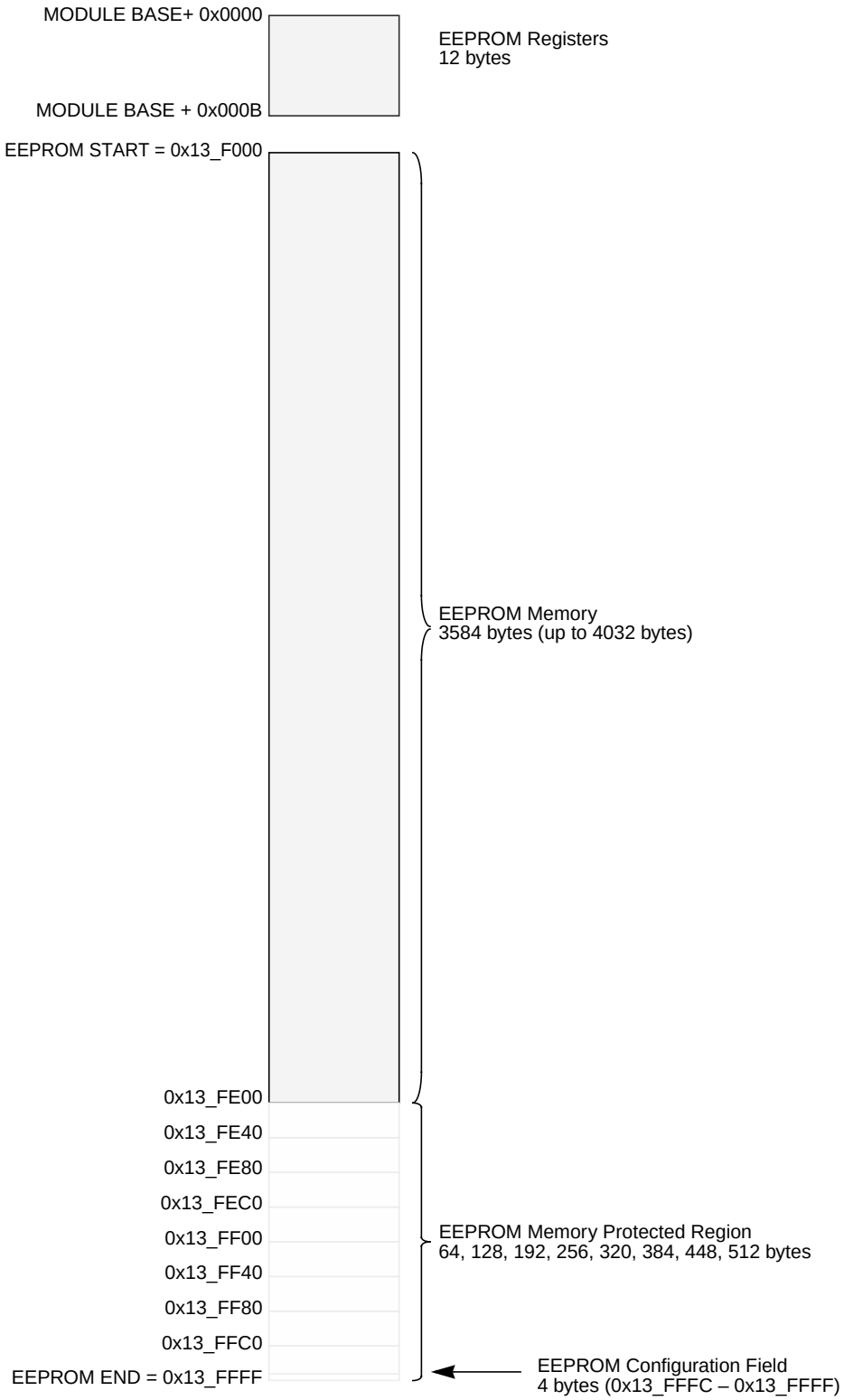

Figure 4-2. EEPROM Memory Map

Table 4-6. ESTAT Field Descriptions

Field	Description
7 CBEIF	**Command Buffer Empty Interrupt Flag** — The CBEIF flag indicates that the address, data, and command buffers are empty so that a new command write sequence can be started. The CBEIF flag is cleared by writing a 1 to CBEIF. Writing a 0 to the CBEIF flag has no effect on CBEIF. Writing a 0 to CBEIF after writing an aligned word to the EEPROM address space but before CBEIF is cleared will abort a command write sequence and cause the ACCERR flag to be set. Writing a 0 to CBEIF outside of a command write sequence will not set the ACCERR flag. The CBEIF flag is used together with the CBEIE bit in the ECNFG register to generate an interrupt request (see Figure 4-24). 0 Buffers are full. 1 Buffers are ready to accept a new command.
6 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is clear and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active commands completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect on CCIF. The CCIF flag is used together with the CCIE bit in the ECNFG register to generate an interrupt request (see Figure 4-24). 0 Command in progress. 1 All commands are completed.
5 PVIOL	**Protection Violation Flag** — The PVIOL flag indicates an attempt was made to program or erase an address in a protected area of the EEPROM memory during a command write sequence. The PVIOL flag is cleared by writing a 1 to PVIOL. Writing a 0 to the PVIOL flag has no effect on PVIOL. While PVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No failure. 1 A protection violation has occurred.
4 ACCERR	**Access Error Flag** — The ACCERR flag indicates an illegal access has occurred to the EEPROM memory caused by either a violation of the command write sequence (see Section 4.4.1.2, “Command Write Sequence”), issuing an illegal EEPROM command (see Table 4-8), launching the sector erase abort command terminating a sector erase operation early (see Section 4.4.2.5, “Sector Erase Abort Command”) or the execution of a CPU STOP instruction while a command is executing (CCIF = 0). The ACCERR flag is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR flag has no effect on ACCERR. While ACCERR is set, it is not possible to launch a command or start a command write sequence. If ACCERR is set by an erase verify operation, any buffered command will not launch. 0 No access error detected. 1 Access error has occurred.
2 BLANK	**Flag Indicating the Erase Verify Operation Status** — When the CCIF flag is set after completion of an erase verify command, the BLANK flag indicates the result of the erase verify operation. The BLANK flag is cleared by the EEPROM module when CBEIF is cleared as part of a new valid command write sequence. Writing to the BLANK flag has no effect on BLANK. 0 EEPROM block verified as not erased. 1 EEPROM block verified as erased.
1 FAIL	**Flag Indicating a Failed EEPROM Operation** — The FAIL flag will set if the erase verify operation fails (EEPROM block verified as not erased). The FAIL flag is cleared by writing a 1 to FAIL. Writing a 0 to the FAIL flag has no effect on FAIL. 0 EEPROM operation completed without error. 1 EEPROM operation failed.

Table 5-17. Instruction Set Summary (Sheet 3 of 3)

Functionality	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANDH RD, #IMM8	1	0	0	0	1	RD			IMM8							
BITL RD, #IMM8	1	0	0	1	0	RD			IMM8							
BITH RD, #IMM8	1	0	0	1	1	RD			IMM8							
ORL RD, #IMM8	1	0	1	0	0	RD			IMM8							
ORH RD, #IMM8	1	0	1	0	1	RD			IMM8							
XNORL RD, #IMM8	1	0	1	1	0	RD			IMM8							
XNORH RD, #IMM8	1	0	1	1	1	RD			IMM8							
Arithmetic Immediate Instructions																
SUBL RD, #IMM8	1	1	0	0	0	RD			IMM8							
SUBH RD, #IMM8	1	1	0	0	1	RD			IMM8							
CMPL RS, #IMM8	1	1	0	1	0	RS			IMM8							
CPCH RS, #IMM8	1	1	0	1	1	RS			IMM8							
ADDL RD, #IMM8	1	1	1	0	0	RD			IMM8							
ADDH RD, #IMM8	1	1	1	0	1	RD			IMM8							
LDL RD, #IMM8	1	1	1	1	0	RD			IMM8							
LDH RD, #IMM8	1	1	1	1	1	RD			IMM8							

NOTE

Remember that in parallel to additional actions caused by self clock mode or clock monitor reset[1] handling the clock quality checker continues to check the OSCCLK signal.

The clock quality checker enables the PLL and the voltage regulator (VREG) anytime a clock check has to be performed. An ongoing clock quality check could also cause a running PLL (f_{SCM}) and an active VREG during pseudo stop mode or wait mode.

7.4.1.5 Computer Operating Properly Watchdog (COP)

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus a system reset is initiated (see Section 7.4.1.5, “Computer Operating Properly Watchdog (COP)”). The COP runs with a gated OSCCLK. Three control bits in the COPCTL register allow selection of seven COP time-out periods.

When COP is enabled, the program must write 0x_55 and 0x_AA (in this order) to the ARMCOP register during the selected time-out period. Once this is done, the COP time-out period is restarted. If the program fails to do this and the COP times out, the part will reset. Also, if any value other than 0x_55 or 0x_AA is written, the part is immediately reset.

Windowed COP operation is enabled by setting WCOP in the COPCTL register. In this mode, writes to the ARMCOP register to clear the COP timer must occur in the last 25% of the selected time-out period. A premature write will immediately reset the part.

If PCE bit is set, the COP will continue to run in pseudo stop mode.

7.4.1.6 Real Time Interrupt (RTI)

The RTI can be used to generate a hardware interrupt at a fixed periodic rate. If enabled (by setting RTIE = 1), this interrupt will occur at the rate selected by the RTICTL register. The RTI runs with a gated OSCCLK. At the end of the RTI time-out period the RTIF flag is set to 1 and a new RTI time-out period starts immediately.

A write to the RTICTL register restarts the RTI time-out period.

If the PRE bit is set, the RTI will continue to run in pseudo stop mode.

7.4.2 Operating Modes

7.4.2.1 Normal Mode

The CRG block behaves as described within this specification in all normal modes.

1. A Clock Monitor Reset will always set the SCME bit to logical 1.

7.4.3.3.2 Wake-up from Full Stop (PSTP = 0)

The MCU requires an external interrupt or an external reset in order to wake-up from stop-mode.

If the MCU gets an external reset during full stop mode active, the CRG asynchronously restores all configuration bits in the register space to its default settings and will perform a maximum of 50 clock *check_windows* (see Section 7.4.1.4, “Clock Quality Checker”). After completing the clock quality check the CRG starts the reset generator. After completing the reset sequence processing begins by fetching the normal reset vector. Full stop-mode is left and the MCU is in run mode again.

If the MCU is woken-up by an interrupt and the fast wake-up feature is disabled (FSTWKP = 0 or SCME = 0), the CRG will also perform a maximum of 50 clock *check_window*s (see Section 7.4.1.4, “Clock Quality Checker”). If the clock quality check is successful, the CRG will release all system and core clocks and will continue with normal operation. If all clock checks within the Timeout-Window are failing, the CRG will switch to self-clock mode or generate a clock monitor reset (CMRESET) depending on the setting of the SCME bit.

If the MCU is woken-up by an interrupt and the fast wake-up feature is enabled (FSTWKP = 1 and SCME = 1), the system will immediately resume operation in self-clock mode (see Section 7.4.1.4, “Clock Quality Checker”). The SCMIF flag will not be set. The system will remain in self-clock mode with oscillator disabled until FSTWKP bit is cleared. The clearing of FSTWKP will start the oscillator and the clock quality check. If the clock quality check is successful, the CRG will switch all system clocks to oscillator clock. The SCMIF flag will be set. See application examples in Figure 7-23 and Figure 7-24.

Because the PLL has been powered-down during stop-mode the PLLSEL bit is cleared and the MCU runs on OSCCLK after leaving stop-mode. The software must manually set the PLLSEL bit again, in order to switch system and core clocks to the PLLCLK.

NOTE

In full stop mode or self-clock mode caused by the fast wake-up feature, the clock monitor and the oscillator are disabled.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000D ATDDIEN1	R	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
	W								
0x000E PORTAD0	R	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
	W								
0x000F PORTAD1	R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
	W								
0x0010–0x002F ATDDRxH–ATDDRxL	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
	W								
	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
	W								

= Unimplemented or Reserved u = Unaffected

Figure 9-2. ATD Register Summary (continued)

9.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence but will not start a new sequence.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	0	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 9-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime

Table 9-2. ATDCTL0 Field Descriptions

Field	Description
3:0 WRAP[3:0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 9-3.

- 1/3 duty (3 backplanes), 1/3 bias (4 voltage levels)
- 1/4 duty (4 backplanes), 1/3 bias (4 voltage levels)

The voltage levels required for the different operating modes are generated internally based on VLCD. Changing VLCD alters the differential RMS voltage across the segments in the ON and OFF states, thereby setting the display contrast.

The backplane waveforms are continuous and repetitive every frame. They are fixed within each operating mode and are not affected by the data in the LCD RAM.

The frontplane waveforms generated are dependent on the state (ON or OFF) of the LCD segments as defined in the LCD RAM. The LCD32F4BV1 driver hardware uses the data in the LCD RAM to construct the frontplane waveform to create a differential RMS voltage necessary to turn the segment ON or OFF.

The LCD duty is decided by the DUTY1 and DUTY0 bits in the LCD control register 0 (LCDCR0). The number of bias voltage levels is determined by the BIAS bit in LCDCR0. Table 10-8 summarizes the multiplex modes (duties) and the bias voltage levels that can be selected for each multiplex mode (duty). The backplane pins have their corresponding backplane waveform output BP[3:0] in high impedance state when in the OFF state as indicated in Table 10-8. In the OFF state the corresponding pins BP[3:0]can be used for other functionality, for example as general purpose I/O ports.

Table 10-8. LCD Duty and Bias

Duty	LCDCR0 Register		Backplanes				Bias (BIAS = 0)			Bias (BIAS = 1)		
	DUTY1	DUTY0	BP3	BP2	BP1	BP0	1/1	1/2	1/3	1/1	1/2	1/3
1/1	0	1	OFF	OFF	OFF	BP0	YES	NA	NA	YES	NA	NA
1/2	1	0	OFF	OFF	BP1	BP0	NA	YES	NA	NA	NA	YES
1/3	1	1	OFF	BP2	BP1	BP0	NA	NA	YES	NA	NA	YES
1/4	0	0	BP3	BP2	BP1	BP0	NA	NA	YES	NA	NA	YES

10.4.2 Operation in Wait Mode

The LCD32F4BV1 driver system operation during wait mode is controlled by the LCD stop in wait (LCDSWAI) bit in the LCD control register 1 (LCDCR1). If LCDSWAI is reset, the LCD32F4BV1 driver system continues to operate during wait mode. If LCDSWAI is set, the LCD32F4BV1 driver system is turned off during wait mode. In this case, the LCD waveform generation clocks are stopped and the LCD32F4BV1 drivers pull down to VSSX those frontplane and backplane pins that were enabled before entering wait mode. The contents of the LCD RAM and the LCD registers retain the values they had prior to entering wait mode.

10.4.3 Operation in Pseudo Stop Mode

The LCD32F4BV1 driver system operation during pseudo stop mode is controlled by the LCD run in pseudo stop (LCDRPSTP) bit in the LCD control register 1 (LCDCR1). If LCDRPSTP is reset, the LCD32F4BV1 driver system is turned off during pseudo stop mode. In this case, the LCD waveform generation clocks are stopped and the LCD32F4BV1 drivers pull down to VSSX those frontplane and backplane pins that were enabled before entering pseudo stop mode. If LCDRPSTP is set, the

11.3.2.4 Motor Controller Channel Control Registers

Each PWM channel has one associated control register to control output delay, PWM alignment, and output mode. The registers are named MCCC0... MCCC11. In the following, MCCC0 is described as a reference for all twelve registers.

Offset Module Base + 0x0010 . . . 0x001B

	7	6	5	4	3	2	1	0
R	MCOM1	MCOM0	MCAM1	MCAM0	0	0	CD1	CD0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-7. Motor Controller Control Register Channel0 .. 11 (MCCC0 .. MCCC11)

Table 11-6. MCCC0–MCCC11 Field Descriptions

Field	Description
7:6 MCOM[1:0]	**Output Mode** — MCOM1, MCOM0 control the PWM channel's output mode. See Table 11-7.
5:4 MCAM[1:0]	**PWM Channel Alignment Mode** — MCAM1, MCAM0 control the PWM channel's PWM alignment mode and operation. See Table 11-8. MCAM[1:0] and MCOM[1:0] are double buffered. The values used for the generation of the output waveform will be copied to the working registers either at once (if all PWM channels are disabled or MCPER is set to 0) or if a timer counter overflow occurs. Reads of the register return the most recent written value, which are not necessarily the currently active values.
1:0 CD[1:0]	**PWM Channel Delay** — Each PWM channel can be individually delayed by a programmable number of PWM timer counter clocks. The delay will be n/f_{TC}. See Table 11-9.

Table 11-7. Output Mode

MCOM[1:0]	Output Mode
00	Half H-bridge mode, PWM on MnCxM, MnCxP is released
01	Half H-bridge mode, PWM on MnCxP, MnCxM is released
10	Full H-bridge mode
11	Dual full H-bridge mode

Table 11-8. PWM Alignment Mode

MCAM[1:0]	PWM Alignment Mode
00	Channel disabled
01	Left aligned
10	Right aligned
11	Center aligned

19.3.2.16 Pulse Accumulator A Flag Register (PAFLG)

Module Base + 0x0021

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PAOVF	PAIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-37. Pulse Accumulator A Flag Register (PAFLG)

Read: Anytime

Write used in the flag clearing mechanism. Writing a one to the flag clears the flag. Writing a zero will not affect the current status of the bit.

NOTE

When TFFCA = 1, the flags cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference Section 19.3.2.6, “Timer System Control Register 1 (TSCR1)”.

All bits reset to zero.

PAFLG indicates when interrupt conditions have occurred. The flags can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (Reference TFFCA bit in Section 19.3.2.6, “Timer System Control Register 1 (TSCR1)”).

Table 19-22. PAFLG Field Descriptions

Field	Description
1 PAOVF	**Pulse Accumulator A Overflow Flag** — Set when the 16-bit pulse accumulator A overflows from 0xFFFF to 0x0000, or when 8-bit pulse accumulator 3 (PAC3) overflows from 0x00FF to 0x0000. When PACMX = 1, PAOVF bit can also be set if 8-bit pulse accumulator 3 (PAC3) reaches 0x00FF followed by an active edge on IC3.
0 PAIF	**Pulse Accumulator Input edge Flag** — Set when the selected edge is detected at the IC7 input pin. In event mode the event edge triggers PAIF and in gated time accumulation mode the trailing edge of the gate signal at the IC7 input pin triggers PAIF.

19.3.2.17 Pulse Accumulators Count Registers (PACN3 and PACN2)

Module Base + 0x0022

	7	6	5	4	3	2	1	0
R W	PACNT7(15)	PACNT6(14)	PACNT5(13)	PACNT4(12)	PACNT3(11)	PACNT2(10)	PACNT1(9)	PACNT0(8)
Reset	0	0	0	0	0	0	0	0

Figure 19-38. Pulse Accumulators Count Register 3 (PACN3)

19.4.1 Enhanced Capture Timer Modes of Operation

The enhanced capture timer has 8 input capture, output compare (IC/OC) channels, same as on the HC12 standard timer (timer channels TC0 to TC7). When channels are selected as input capture by selecting the IOSx bit in TIOS register, they are called input capture (IC) channels.

Four IC channels (channels 7–4) are the same as on the standard timer with one capture register each that memorizes the timer value captured by an action on the associated input pin.

Four other IC channels (channels 3–0), in addition to the capture register, also have one buffer each called a holding register. This allows two different timer values to be saved without generating any interrupts.

Four 8-bit pulse accumulators are associated with the four buffered IC channels (channels 3–0). Each pulse accumulator has a holding register to memorize their value by an action on its external input. Each pair of pulse accumulators can be used as a 16-bit pulse accumulator.

The 16-bit modulus down-counter can control the transfer of the IC registers and the pulse accumulators contents to the respective holding registers for a given period, every time the count reaches zero.

The modulus down-counter can also be used as a stand-alone time base with periodic interrupt capability.

19.4.1.1 IC Channels

The IC channels are composed of four standard IC registers and four buffered IC channels.

- An IC register is empty when it has been read or latched into the holding register.
- A holding register is empty when it has been read.

19.4.1.1.1 Non-Buffered IC Channels

The main timer value is memorized in the IC register by a valid input pin transition. If the corresponding NOVWx bit of the ICOVW register is cleared, with a new occurrence of a capture, the contents of IC register are overwritten by the new value. If the corresponding NOVWx bit of the ICOVW register is set, the capture register cannot be written unless it is empty. This will prevent the captured value from being overwritten until it is read.

19.4.1.1.2 Buffered IC Channels

There are two modes of operations for the buffered IC channels:

1. IC latch mode (LATQ = 1)

   The main timer value is memorized in the IC register by a valid input pin transition (see Figure 19-67 and Figure 19-68).

   The value of the buffered IC register is latched to its holding register by the modulus counter for a given period when the count reaches zero, by a write 0x0000 to the modulus counter or by a write to ICLAT in the MCCTL register.

   If the corresponding NOVWx bit of the ICOVW register is cleared, with a new occurrence of a capture, the contents of IC register are overwritten by the new value. In case of latching, the contents of its holding register are overwritten.

20.2 External Signal Description

Due to the nature of VREG_3V3 being a voltage regulator providing the chip internal power supply voltages, most signals are power supply signals connected to pads.

Table 20-1 shows all signals of VREG_3V3 associated with pins.

Table 20-1. Signal Properties

Name	Function	Reset State	Pull Up
V_{DDR}	Power input (positive supply)	—	—
V_{DDA}	Quiet input (positive supply)	—	—
V_{SSA}	Quiet input (ground)	—	—
V_{DD}	Primary output (positive supply)	—	—
V_{SS}	Primary output (ground)	—	—
V_{DDPLL}	Secondary output (positive supply)	—	—
V_{SSPLL}	Secondary output (ground)	—	—
V_{REGEN} (optional)	Optional Regulator Enable	—	—

NOTE

Check device level specification for connectivity of the signals.

20.2.1 VDDR — Regulator Power Input Pins

Signal V_{DDR} is the power input of VREG_3V3. All currents sourced into the regulator loads flow through this pin. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDR} and V_{SSR} (if V_{SSR} is not available V_{SS}) can smooth ripple on V_{DDR}.

For entering shutdown mode, pin V_{DDR} should also be tied to ground on devices without VREGEN pin.

20.2.2 VDDA, VSSA — Regulator Reference Supply Pins

Signals $V_{DDA}/V_{SSA,}$ which are supposed to be relatively quiet, are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDA} and V_{SSA} can further improve the quality of this supply.

20.2.3 VDD, VSS — Regulator Output1 (Core Logic) Pins

Signals V_{DD}/V_{SS} are the primary outputs of VREG_3V3 that provide the power supply for the core logic. These signals are connected to device pins to allow external decoupling capacitors (100 nF...220 nF, X7R ceramic).

In shutdown mode an external supply driving V_{DD}/V_{SS} can replace the voltage regulator.

25.3 Memory Map and Registers

25.3.1 Module Memory Map

A summary of the registers associated with the MMC block is shown in Figure 25-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000A	MMCCTL0	R	0	0	0	0	CS3E	CS2E	CS1E	CS0E
		W								
0x000B	MODE	R	MODC	MODB	MODA	0	0	0	0	0
		W								
0x0010	GPAGE	R	0	GP6	GP5	GP4	GP3	GP2	GP1	GP0
		W								
0x0011	DIRECT	R	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
		W								
0x0012	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0013	MMCCTL1	R	0	0	0	0	0	EROMON	ROMHM	ROMON
		W								
0x0014	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0015	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0016	RPAGE	R	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
		W								
0x0017	EPAGE	R	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
		W								
0x0030	PPAGE	R	PIX7	PIX6	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		W								
0x0031	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

Figure 25-2. MMC Register Summary

A.1.7 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE

Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to Section A.1.8, “Power Dissipation and Thermal Characteristics”.

Table A-4. Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, regulator and analog supply voltage	V_{DD5}	4.5	5	5.5	V
Digital logic supply voltage[1]	V_{DD}	2.35	2.5	2.75	V
PLL supply voltage[2]	V_{DDPLL}	2.35	2.5	2.75	V
Voltage difference V_{DDX} to V_{DDR} to V_{DDM} and V_{DDA}	Δ_{VDDX}	–0.1	0	0.1	V
Voltage difference V_{SSX} to V_{SSR} to V_{SSM} and V_{SSA}	Δ_{VSSX}	–0.1	0	0.1	V
Oscillator	f_{osc}	0.5	—	16	MHz
Bus frequency	f_{bus}	0.5	—	40	MHz
MC9S12XHZ512**C** Operating junction temperature range Operating ambient temperature range[2]	 T_J T_A	 –40 –40	 — 27	 100 85	°C
MC9S12XHZ512**V** Operating junction temperature range Operating ambient temperature range[2]	 T_J T_A	 –40 –40	 — 27	 120 105	°C
MC9S12XHZ512**M** Operating junction temperature range Operating ambient temperature range[2]	 T_J T_A	 –40 –40	 — 27	 140 125	°C

1 The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.

2 Please refer to Section A.1.8, “Power Dissipation and Thermal Characteristics” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

Table A-14. NVM Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External oscillator clock	f_{NVMOSC}	0.5	—	80[1]	MHz
2	D	Bus frequency for programming or erase operations	f_{NVMBUS}	1	—	—	MHz
3	D	Operating frequency	f_{NVMOP}	150	—	200	kHz
4	P	Single word programming time	t_{swpgm}	46[2]	—	74.5[3]	µs
5	D	Flash burst programming consecutive word [4]	t_{bwpgm}	20.4[2]	—	31[3]	µs
6	D	Flash burst programming time for 64 words[4]	t_{brpgm}	1331.2[2]	—	2027.5[3]	µs
7	P	Sector erase time	t_{era}	20[5]	—	26.7[3]	ms
8	P	Mass erase time	t_{mass}	100[5]	—	133[3]	ms
9	D	Blank check time Flash per block	t_{check}	11[6]	—	65546[7]	t_{cyc}
10	D	Blank check time EEPROM per block	t_{check}	11[6]	—	2058[7]	t_{cyc}

1 Restrictions for oscillator in crystal mode apply.

2 Minimum programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3 Maximum erase and programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections Section A.3.1.1, “Single Word Programming” – Section A.3.1.4, “Mass Erase” for guidance.

4 Burst programming operations are not applicable to EEPROM

5 Minimum erase times are achieved under maximum NVM operating frequency, f_{NVMOP}

6 Minimum time, if first word in the array is not blank

7 Maximum time to complete check on an erased block

A.5 Reset, Oscillator, and PLL

This section summarizes the electrical characteristics of the various startup scenarios for oscillator and phase-locked loop (PLL).

A.5.1 Startup

Table A-17 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block Guide.

Table A-17. Startup Characteristics

Conditions are shown in Table A-4unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reset input pulse width, minimum input time	PW_{RSTL}	2	—	—	t_{osc}
2	D	Startup from reset	n_{RST}	192	—	196	n_{osc}
3	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20	—	—	ns
4	D	Wait recovery startup time	t_{WRS}	—	—	14	t_{cyc}
5	D	Fast wakeup from STOP[1]	t_{fws}	—	50	—	µs

1 V_{DD1} filter capacitor 220 nF, V_{DD5} = 5 V, T= 25°C

A.5.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.5.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when V_{DD5} is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG flags register has not been set.

A.5.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.5.1.4 Stop Recovery

Out of stop the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

Table A-18. Oscillator Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1a	C	Crystal oscillator range (loop controlled Pierce)	f_{OSC}	4.0	—	16	MHz
1b	C	Crystal oscillator range (full swing Pierce)[1, 2]	f_{OSC}	0.5	—	40	MHz
2	P	Startup current	i_{OSC}	100	—	—	µA
3	C	Oscillator start-up time (loop controlled Pierce)	t_{UPOSC}	—	—[3]	50[4]	ms
4	D	Clock quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock monitor failure assert frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency	f_{EXT}	0.5	—	80	MHz
7	D	External square wave pulse width low	t_{EXTL}	5	—	—	ns
8	D	External square wave pulse width high	t_{EXTH}	5	—	—	ns
9	D	External square wave rise time	t_{EXTR}	—	—	1	ns
10	D	External square wave fall time	t_{EXTF}	—	—	1	ns
11	D	Input capacitance (EXTAL, XTAL inputs)	C_{IN}	—	7	—	pF
12	P	EXTAL pin input high voltage[5]	$V_{IH,EXTAL}$	0.75* V_{DDPLL}	—	—	V
	T	EXTAL pin input high voltage[5]	$V_{IH,EXTAL}$	—	—	V_{DDPLL} + 0.3	V
13	P	EXTAL pin input low voltage[5]	$V_{IL,EXTAL}$	—	—	0.25* V_{DDPLL}	V
	T	EXTAL pin input low voltage[5]	$V_{IL,EXTAL}$	V_{SSPLL} – 0.3	—	—	V
14	C	EXTAL pin input hysteresis[5]	$V_{HYS,EXTAL}$	—	250	—	mV

1 Depending on the crystal a damping series resistor might be necessary

2 $\overline{XCLKS}$ = 0

3 f_{osc} = 4 MHz, C = 22 pF.

4 Maximum value is for extreme cases using high Q, low frequency crystals

5 If full swing Pierce oscillator/external clock circuitry is used. ($\overline{XCLKS}$ = 0)

0x0200–0x027F Port Integration Module (PIM) Map 5 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x021F	SRRP	R	SRRP7	SRRP6	SRRP5	SRRP4	SRRP3	SRRP2	SRRP1	SRRP0
		W								
0x0220–0x022F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0230	PTL	R	PTL7	PTL6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
		W								
0x0231	PTIL	R	PTIL7	PTIL6	PTIL5	PTIL4	PTIL3	PTIL2	PTIL1	PTIL0
		W								
0x0232	DDRL	R	DDRL7	DDRL6	DDRL5	DDRL4	DDRL3	DDRL2	DDRL1	DDRL0
		W								
0x0233	RDRL	R	RDRL7	RDRL6	RDRL5	RDRL4	RDRL3	RDRL2	RDRL1	RDRL0
		W								
0x0234	PERL	R	PERL7	PERL6	PERL5	PERL4	PERL3	PERL2	PERL1	PERL0
		W								
0x0235	PPSL	R	PPSL7	PPSL6	PPSL5	PPSL4	PPSL3	PPSL2	PPSL1	PPSL0
		W								
0x0236	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0237	SRRL	R	SRRL7	SRRL6	SRRL5	SRRL4	SRRL3	SRRL2	SRRL1	SRRL0
		W								
0x0238	PTU	R	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
		W								
0x0239	PTIU	R	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
		W								
0x023A	DDRU	R	DDRU7	DDRU7	DDRU	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		W								
0x023B	SRRU	R	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
		W								
0x023C	PERU	R	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		W								
0x023D	PPSU	R	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		W								
0x023E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x023F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0240	PTV	R	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
		W								
0x0241	PTIV	R	PTIV7	PTIV6	PTIV5	PTIV4	PTIV3	PTIV2	PTIV1	PTIV0
		W								
0x0242	DDRV	R	DDRV7	DDRV7	DDRV	DDRV4	DDRV3	DDRV2	DDRV1	DDRV0
		W								
0x0243	SRRV	R	SRRV7	SRRV6	SRRV5	SRRV4	SRRV3	SRRV2	SRRV1	SRRV0
		W								
0x0244	PERV	R	PERV7	PERV6	PERV5	PERV4	PERV3	PERV2	PERV1	PERV0
		W								

0x0200–0x027F Port Integration Module (PIM) Map 5 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x025C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025D	PIEAD	R	PIEAD7	PIEAD6	PIEAD5	PIEAD4	PIEAD3	PIEAD2	PIEAD1	PIEAD0
		W								
0x025E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025F	PIFAD	R	PIFAD7	PIFAD6	PIFAD5	PIFAD4	PIFAD3	PIFAD2	PIFAD1	PIFAD0
		W								
0x0260–0x027F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0280–0x0287 Stepper Stall Detector (SSD4) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0280	RTZ4CTL	R	ITG	DCOIL	RCIR	POL	0	0	STEP	
		W								
0x0281	MDC4CTL	R	MCZIE	MODMC	RDMCL	PRE	0	MCEN	0	AOVIE
		W					FLMC			
0x0282	SSD4CTL	R	RTZE	SDCPU	SSDWAI	FTST	0	0	ACLKS	
		W								
0x0283	SSD4FLG	R	MCZIF	0	0	0	0	0	0	AOVIF
		W								
0x0284	MDC4CNT(hi)	R	MDCCNT[15:8]							
		W								
0x0285	MDC4CNT(lo)	R	MDCCNT[7:0]							
		W								
0x0286	ITG4ACC(hi)	R	ITGACC[15:8]							
		W								
0x0287	ITG4ACC(lo)	R	ITGACC[7:0]							
		W								

0x0288–0x028F Stepper Stall Detector (SSD0) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0288	RTZ0CTL	R	ITG	DCOIL	RCIR	POL	0	0	STEP	
		W								
0x0289	MDC0CTL	R	MCZIE	MODMC	RDMCL	PRE	0	MCEN	0	AOVIE
		W					FLMC			
0x028A	SSD0CTL	R	RTZE	SDCPU	SSDWAI	FTST	0	0	ACLKS	
		W								
0x028B	SSD0FLG	R	MCZIF	0	0	0	0	0	0	AOVIF
		W								
0x028C	MDC0CNT(hi)	R	MDCCNT[15:8]							
		W								

0x0380–0x03BF XGATE Map (Sheet 3 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03AD	XGR6 (lo)	R	XGR6[7:0]							
		W								
0x03AE	XGR7 (hi)	R	XGR7[15:8]							
		W								
0x03AF	XGR7 (lo)	R	XGR7[7:0]							
		W								
0x03B0–0x03BF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x03C0–0x07FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03C0 –0x07FF	Reserved	R	0	0	0	0	0	0	0	0
		W								