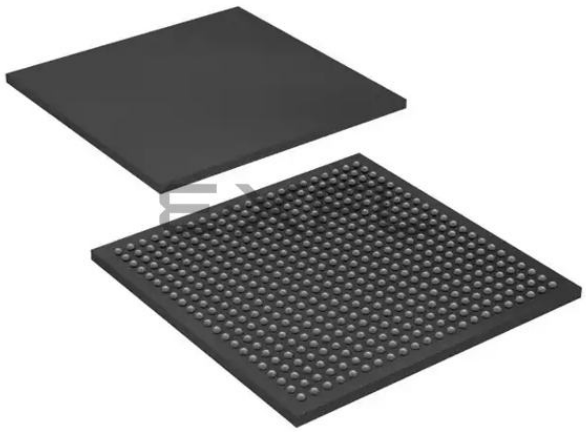

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4800
Total RAM Bits	49152
Number of I/O	303
Number of Gates	120000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1m120f484c6

Tables 2 and 3 show the Mercury™ FineLine BGA™ device package sizes, options, and I/O pin counts.

Table 2. Mercury Package Sizes

Feature	484-Pin FineLine BGA	780-Pin FineLine BGA
Pitch (mm)	1.00	1.00
Area (mm^2)	529	841
Length × width (mm × mm)	23 × 23	29 × 29

Table 3. Mercury Package Options & I/O Count

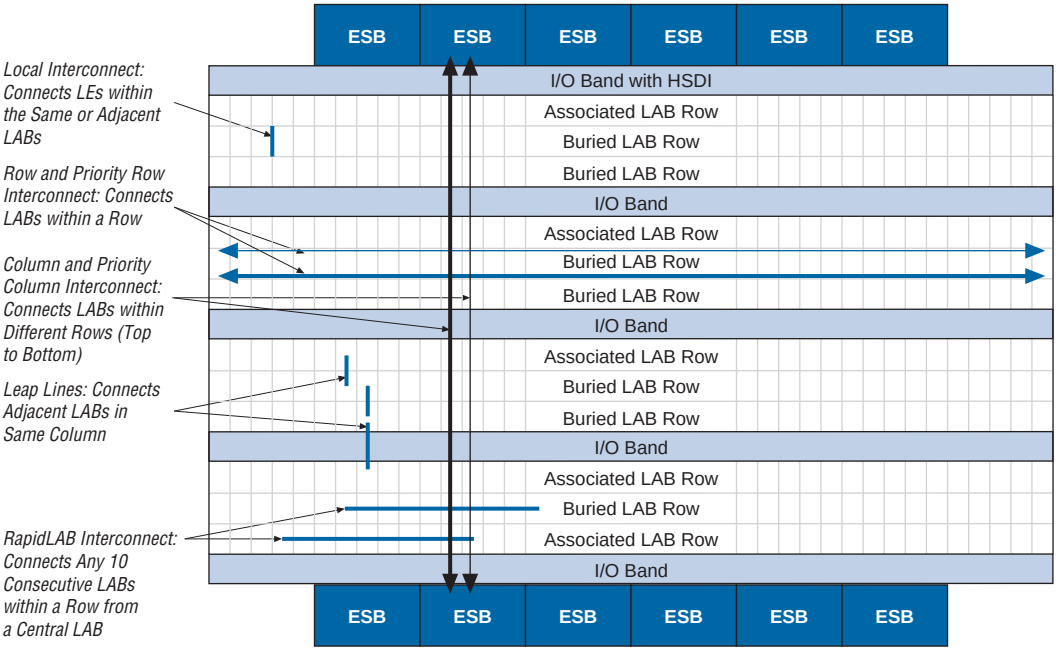
Device	484-Pin FineLine BGA	780-Pin FineLine BGA
EP1M120	303	
EP1M350		486

General Description

Mercury devices integrate high-speed differential transceivers and support for CDR with a speed-optimized PLD architecture. These transceivers are implemented through the dedicated serializer, deserializer, and clock recovery circuitry in the HSDI and incorporate support for the LVDS, LVPECL, and 3.3-V PCML I/O standards. This circuitry, together with enhanced I/O elements (IOEs) and support for numerous I/O standards, allows Mercury devices to meet high-speed interface requirements.

Mercury devices are the first PLDs optimized for core performance. These LUT-based, enhanced memory devices use a network of fast routing resources to achieve optimal performance. These resources are ideal for data-path, register-intensive, mathematical, digital signal processing (DSP), or communications designs.

Figure 1. Mercury Architecture Block Diagram *Note (1)*



Note to Figure 1:

(1) Figure 1 shows an EP1M120 device. Mercury devices have a varying number of rows, columns, and ESBs, as shown in Table 5.

Table 5 lists the resources available in Mercury devices.

Table 5. Mercury Device Resources

Device	LAB Rows	LAB Columns	I/O Row Bands	ESBs
EP1M120	12	40	5	12
EP1M350	18	80	4	28

Mercury devices provide four dedicated clock input pins and six dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on Mercury devices can also feed logic. Dedicated clocks can also be used with the Mercury general purpose PLLs for clock management.

Each I/O row band also provides two additional I/O pins that can drive two row-global signals. Row-global signals can drive register control inputs for the LAB row associated with that particular I/O row band.

High-Speed Differential Interface

The top I/O or HSDI band in Mercury devices contains dedicated circuitry for supporting differential standards at speeds up to 1.25 Gbps. Mercury devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, and 3.3-V PCML I/O standards. Two dedicated high-speed PLLs (separate from the general purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, clock recovery units (CRUs) at each receiver channel enable CDR. EP1M120 devices support eight input channels, eight output channels, and two dedicated clock inputs for feeding the receiver and/or transmitter PLLs. EP1M350 devices support 18 input channels, 18 output channels, and two dedicated clock inputs.

Mercury devices have optional built-in 100-Ω termination resistors on HSDI differential receiver data pins and the `HSDI_CLK1` and `HSDI_CLK2` pins.

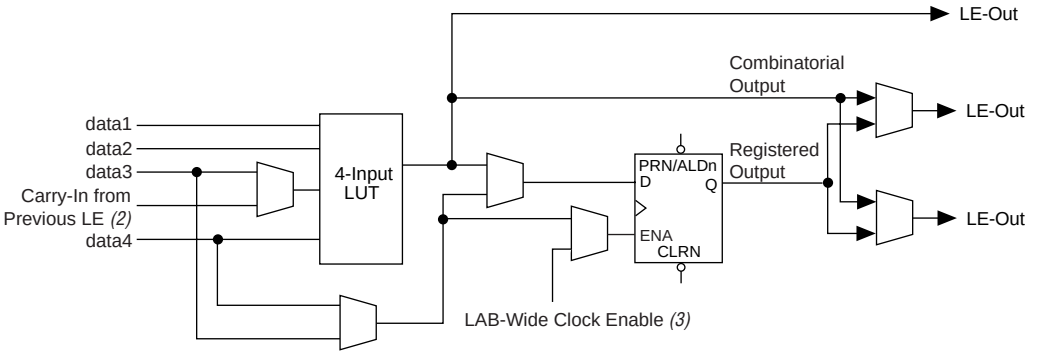
Designers can use the HSDI circuitry for the following applications:

- Gigabit Ethernet backplanes
- ATM, SONET
- RapidIO
- POS-PHY Level 4
- Fibre Channel
- SDTV

The HSDI band supports one of two possible modes:

- Source-synchronous mode
- Clock data recovery (CDR) mode

Figure 8. Normal-Mode LE *Note (1)*



Notes to Figure 8:

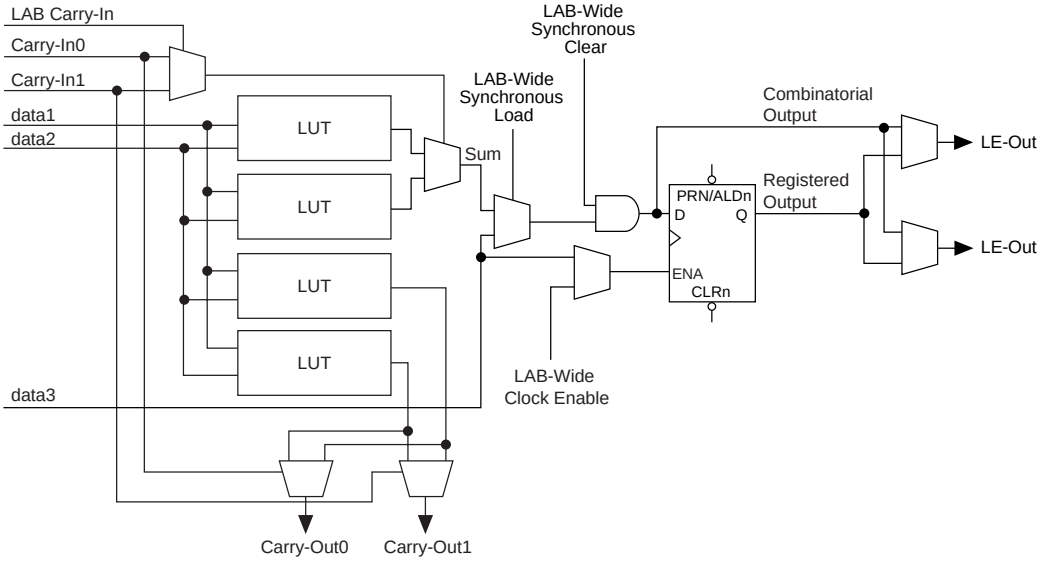
(1) LEs in normal mode support register packing.
(2) When using the carry-in in normal mode, the packed register feature is unavailable.
(3) There are two LAB-wide clock enables per LAB in addition to LE-specific clock enables.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. A LE in arithmetic mode contains four 2-input LUTs. The first two 2-input LUTs compute two summations based on a possible carry of `1` or `0`; the other two LUTs generate carry outputs for the two possible chains of the carry-select look-ahead (CSLA) circuitry. As shown in Figure 9, the LAB carry-in signal selects the appropriate carry-in chain (either `carry-in0` or `carry-in1`). The logic level of the chain selected in turn selects which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, this output is the signal comprised of the sum `data1` + `data2` + *carry*, where *carry* is `0` or `1`. The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of `1` and the other for a carry of `0`. The `carry-in0` signal acts as the carry select for the `carry-out0` output; `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output. Figure 9 shows a Mercury LE in arithmetic mode.

The arithmetic mode also offers clock enable, counter enable, synchronous up / down control, synchronous clear, and synchronous load options. The counter enable and synchronous up / down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in a LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 9. Arithmetic Mode LE



Carry-Select Look-Ahead Chain

The CSLA chain provides a very fast carry-forward function between LEs in arithmetic mode or multiplier mode. The CSLA chain uses the redundant carry calculation to increase the speed of carry functions. The LE can calculate sum and carry values for a possible carry-in of `1` and carry-in of `0` in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit drive forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the CSLA chain. CSLA chains can begin in any LE within a LAB.

The CSLA chain's speed advantage results from the parallel pre-computation of carry chains. Instead of including every LUT in the critical path, only the propagation delays between LAB carry-in generation circuits (LE 4 and LE 10) make up the critical path. This feature allows the Mercury architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 10 shows the CSLA circuitry in a LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. A lab-wide carry-in bit selects which chain is used for the addition of given inputs. The actual carry-in signal for that selected chain, `carry-in0` or `carry-in1`, selects the carry-out to carry forward, which is routed to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven to local, row, or column interconnects.

Figure 12. Partial Product Formation

For a typical 16 × 16-bit binary tree multiplier, five stages are needed to determine the final product. The Mercury LE multiplier mode allows the partial product formation stage (Stage 1) and the first sum of stages (Stage 2) to be combined in a single stage, shown in Figure 13. This feature, combined with the direct connection between RapidLAB lines and LEs in multiplier mode, allows the fast dedicated implementation of multipliers.

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications relative to the global clock.

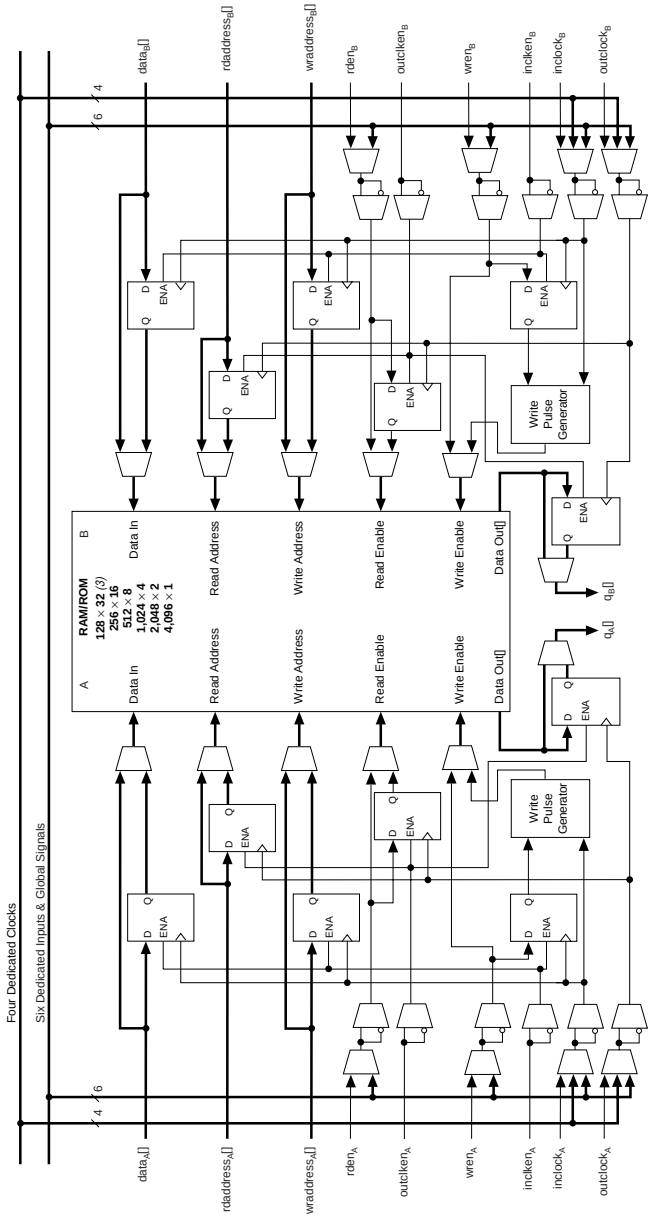
ESBs are grouped together in rows at the top and bottom of the device for fast horizontal communication. The ESB row interconnect can be driven by any ESB in the row. The row interconnect drives the ESB local interconnect, which in turn drives the ESB ports. ESB outputs drive the ESB local interconnect, which can drive row interconnect as well as all types of column interconnect, including leap lines. The leap lines allow fast access between ESBs and the adjacent LAB row.

When implementing memory, each ESB can be configured in any of the following sizes for quad port and true dual-port memory modes: 256 × 16; 512 × 8; 1,024 × 4; 2,048 × 2; or 4,096 × 1. For dual-port and single-port modes, the ESB can be configured for 128 × 32 in addition to the list above. For variable port width RAMs, any port width ratio combination must be 1, 2, 4, 8, or 16. For example, a RAM with data ports of width 1 and 16 or 2 and 32 will work, but not 1 and 32.

The ESB can also be split in half and used for two independent 2,048-bit single-port or dual-port RAM blocks. For example, one half of the ESB can be used as a 128 × 16 memory single-port memory while the other half can be used for a 1,024 × 2 dual-port memory. This effectively doubles the number of RAMs a Mercury device can implement for its given number of ESBs. The Quartus II software automatically merges two logical memory functions in a design into an ESB; the designer does not need to merge the functions manually.

By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 256 × 16 RAM blocks can be combined to form a 256 × 32 RAM block, and two 512 × 8 RAM blocks can be combined to form a 512 × 16 RAM block. Memory performance does not degrade for memory blocks up to 4,096 words deep. Each ESB can implement a 4,096-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays. To create a high-speed memory block more than 4,096 words deep, the Quartus II software will automatically combine ESBs with LE control logic.

Figure 19. ESB in Read/Write Clock Mode *Notes (1), (2)*



Notes to Figure 19:

(1) Only half of the ESB, either A or B, is used for dual-port configuration.
(2) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(3) This configuration is supported for dual-port configuration.

Zero Bus Turnaround SRAM Interface Support

In addition to DDR SDRAM support, Mercury device I/O pins also support interfacing with ZBT SRAM blocks at up to 200 MHz. ZBT SRAM blocks are designed to eliminate dead bus cycles when turning a bidirectional bus around between reads and writes, or writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can read or write on every clock cycle.

To avoid bus contention, the output t_{ZX} delay ensures that the clock-to-low-impedance time ($\mathbf{t_{ZX}}$) is greater than the clock-to-high-impedance time ($\mathbf{t_{XZ}}$). Time delay control of clocks to the OE/output and input register, using a single general purpose PLL, enable the Mercury device to meet ZBT $\mathbf{t_{CO}}$ and $\mathbf{t_{SU}}$ times.

Programmable Drive Strength

The output buffer for each Mercury device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL standard has several levels of drive strength that can be controlled by the user. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, and 3.3-V GTL+ support a minimum or maximum setting. The minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. The maximum setting provides higher drive strength that allows for faster switching and is the default setting. Using settings below the maximum provides signal slew-rate control to reduce system noise and signal overshoot. Table 11 shows the possible settings for the I/O standards with drive strength control.

Table 11. Programmable Drive Strength	
I/O Standard	**I_{OH}/I_{OL} Current Strength Setting**
LVTTL (3.3 V)	4 mA
	8 mA
	12 mA
	16 mA
	24 mA (default)
LVTTL (2.5 V)	4 mA
	8 mA
	12 mA
	16 mA (default)
LVTTL (1.8 V)	2 mA
	4 mA (default)
SSTL-3 class I and II SSTL-2 class I and II HSTL class I and II GTL+ (3.3 V)	Minimum
	Maximum (default)

Open-Drain Output

Mercury devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices.

Slew-Rate Control

The output buffer for each Mercury device I/O pin has a programmable output slew rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges.

Dedicated Fast Lines & I/O Pins

Mercury devices incorporate dedicated bidirectional pins for signals with high internal fanout, such as PCI control signals. These pins are called dedicated fast I/O pins (FAST1, FAST2, FAST3, FAST4, FAST5, and FAST6) and can drive the six global fast lines throughout the device, ideal for fast clock, clock enable, clear, preset, or high fanout logic signal distribution. The dedicated fast I/O pins have the same IOE as a regular I/O pin. The dedicated fast lines can also be driven by a LE local interconnect to generate internal global signals.

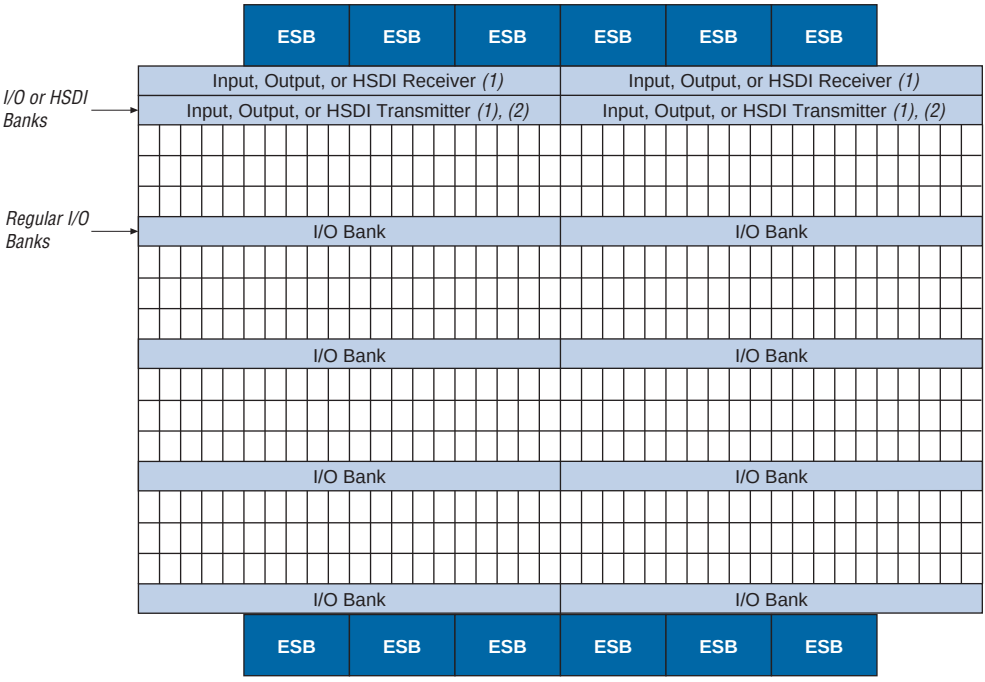
In addition to the device global fast lines, each LAB row has two dedicated fast lines local to the row. This is ideal for high fanout control signals for a section of a design that may fit into a single LAB row. Each I/O band (with the exception of the top I/O band) has two dedicated row-global fast I/O pins to drive the row-global fast resources for the associated LAB. The dedicated local fast I/O pins have the same IOE as a regular I/O pin. The LE local interconnect can drive dedicated row-global fast lines to generate internal global signals specific to a row. There are no pin connections for buried LAB rows; LE local interconnects drive the row-global signals in those rows.

I/O Standard Support

Mercury device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.8-V
- 2.5-V
- 3.3-V PCI
- 3.3-V PCI-X
- 3.3-V AGP (1×, 2×)
- LVDS
- LVPECL
- 3.3-V PCML
- GTL+
- HSTL class I and II
- SSTL-3 class I and II
- SSTL-2 class I and II
- CTT

Figure 30. I/O Bank Layout



Notes to Figure 30:

(1) If HSDI I/O channels are not used, the HSDI banks can be used as regular I/O banks.

(2) When used as regular I/O banks, these banks must be set to the same V_{CCIO} level, but can have separate V_{REF} bank settings.

For more information on I/O standards, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

MultiVolt I/O Interface

The Mercury architecture supports the MultiVolt I/O interface feature, which allows Mercury devices in all packages to interface with devices with different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

Table 16. Mercury JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a Mercury device via the JTAG port with a ByteBlasterMV™ download cable, or using a Jam STAPL or Jam Byte-Code file via an embedded processor.
SignalTap Instructions	These instructions monitor internal device operation with the SignalTap embedded logic analyzer.

The Mercury device instruction register length is 10 bits. The Mercury device USERCODE register length is 32 bits. Tables 17 and 18 show the boundary-scan register length and device IDCODE information for Mercury devices.

Table 17. Mercury Boundary-Scan Register Length

Device	Boundary-Scan Register Length (Bits)
EP1M120	1,125
EP1M350	1,695

Table 18. 32-Bit Mercury Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP1M120	0000	0011 0000 0000 0000	000 0110 1110	1
EP1M350	0000	0011 0000 0000 0001	000 0110 1110	1

Notes to Table 18:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

Table 28. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage				V_{CCIO} – 0.4	V
V_{IH}	High-level input voltage		V_{CCIO}			V
V_{OL}	Low-level output voltage				V_{CCIO} – 0.4	V
V_{OH}	High-level output voltage		V_{CCIO}			V
V_T	Output termination voltage			V_{CCIO}		V
V_{ID}	Differential input voltage		400		800	mV
V_{OD}	Differential output voltage		400	700	800	mV
t_R	Rise time (20 to 80%)				200	ps
t_F	Fall time (20 to 80%)				200	ps
t_{DSKEW}	Differential skew				25	ps
R_1 *(11)*	Output load		90	100	110	Ω
R_2 *(11)*	Receiver differential input resistor		45	50	55	Ω

Table 29. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage		0		2,000	mV
V_{IH}	High-level input voltage		400		2,470	mV
V_{OL}	Low-level output voltage		1,400		1,650	mV
V_{OH}	High-level output voltage		2,275		2,470	mV
V_{ID}	Differential input voltage		400	600	1,200	mV
V_{OD}	Differential output voltage		525	1,050	1,200	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps
t_{DSKEW}	Differential skew				25	ps
R_L	Receiver differential input resistor			100		Ω

Table 42. Bus Hold Parameters

Parameter	Conditions	VCCIO Level						Units
		1.8 V		2.5 V		3.3 V		
		Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–200		–300		–500	µA

Table 43. Mercury Device Capacitance *Note (13)*

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{IO}	I/O pin capacitance		13.5		pF
C_{CLK}	Input capacitance on CLK[4..1] pins		16.9		pF
C_{RXHSDI}	Input capacitance on HSDI receiver pins		8.0		pF
C_{TXHSDI}	Input capacitance on HSDI transmitter pins		18.0		pF
$C_{CLKHSDI}$	Input capacitance on HSDI clock pins		7.5		pF
$C_{FLEXLVDSRX}$	Input capacitance on flexible LVDS receiver pins		13.4		pF
$C_{FLEXLVDSTX}$	Input capacitance on flexible LVDS transmitter pins		13.4		pF

Table 51. EP1M350 External Bidirectional Timing Parameters *Note (1)*

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	0.60		0.57		0.71		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	3.95	2.00	3.97	2.00	4.75	ns
$t_{XZBIDIR}$		3.90		3.93		4.70	ns
$t_{ZXBIDIR}$ *(2)*		3.90		3.93		4.70	ns
$t_{ZXBIDIR}$ *(3)*		4.10		4.13		4.94	ns
$t_{INSUBIDIRPLL}$	0.69		0.70		0.82		ns
$t_{INHBIDIRPLL}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.23	0.50	2.23	0.50	2.69	ns
$t_{XZBIDIRPLL}$		2.19		2.18		2.63	ns
$t_{ZXBIDIRPLL}$ *(2)*		2.19		2.18		2.63	ns
$t_{ZXBIDIRPLL}$ *(3)*		2.39		2.38		2.87	ns

Notes to Tables 46 – 51:

(1) Timing will vary by I/O pin placement. Therefore, use the Quartus II software to determine exact I/O timing for each pin.

(2) This parameter is measured with the **Increase t_{ZX} Delay to Output Pin** option set to **Off**.

(3) This parameter is measured with the **Increase t_{ZX} Delay to Output Pin** option set to **On**.

Power Consumption

Detailed power consumption information for Mercury devices will be released when available.

Configuration & Operation

The Mercury architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The Mercury architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up and before and during configuration. Together, the configuration and initialization processes are called command mode; normal device operation is called user mode.

Revision History

The information contained in the *Mercury Programmable Logic Device Family Data Sheet* version 2.2 supersedes information published in previous versions.

Version 2.2

The following changes were made to the *Mercury Programmable Logic Device Family Data Sheet* version 2.2:

- Updated the condition values (symbols I_I and I_{OZ}) in Table 22.

Version 2.1

The following changes were made to the *Mercury Programmable Logic Device Family Data Sheet* version 2.1:

- Updated Table 8.
- Updated EP1M350 regular I/O banks in Table 13.
- Updated *Note (6)* in Table 14.

Version 2.0

The following changes were made to the *Mercury Programmable Logic Device Family Data Sheet* version 2.0:

- Changed all references to PCML to 3.3-V PCML.
- Updated Table 4.
- Updated "High-Speed Differential Interface" on page 8.
- Added Tables 6 through 8.
- Added Figures 34 and 35.
- Updated I/O specifications in Tables 28 and 29.
- Updated Mercury device capacitance in Table 43.
- Updated EP1M120 device timing in Tables 46 through 49.
- Added EP1M350 device timing in Tables 50 and 51.

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