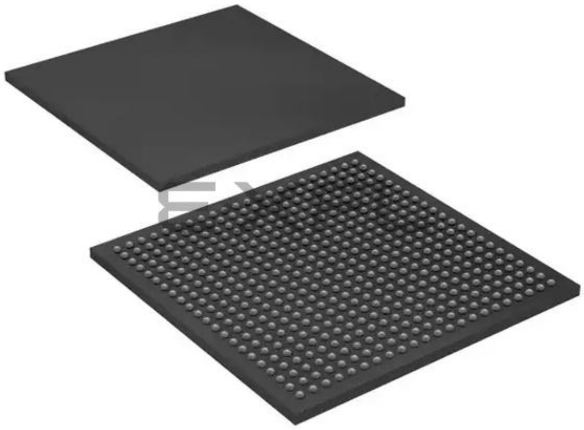
Intel - EP1M120F484C8ES Datasheet



Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4800
Total RAM Bits	49152
Number of I/O	303
Number of Gates	120000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1m120f484c8es

Tables 2 and 3 show the Mercury™ FineLine BGA™ device package sizes, options, and I/O pin counts.

Table 2. Mercury Package Sizes

Feature	484-Pin FineLine BGA	780-Pin FineLine BGA
Pitch (mm)	1.00	1.00
Area (mm^2)	529	841
Length × width (mm × mm)	23 × 23	29 × 29

Table 3. Mercury Package Options & I/O Count

Device	484-Pin FineLine BGA	780-Pin FineLine BGA
EP1M120	303	
EP1M350		486

General Description

Mercury devices integrate high-speed differential transceivers and support for CDR with a speed-optimized PLD architecture. These transceivers are implemented through the dedicated serializer, deserializer, and clock recovery circuitry in the HSDI and incorporate support for the LVDS, LVPECL, and 3.3-V PCML I/O standards. This circuitry, together with enhanced I/O elements (IOEs) and support for numerous I/O standards, allows Mercury devices to meet high-speed interface requirements.

Mercury devices are the first PLDs optimized for core performance. These LUT-based, enhanced memory devices use a network of fast routing resources to achieve optimal performance. These resources are ideal for data-path, register-intensive, mathematical, digital signal processing (DSP), or communications designs.

Mercury devices include other features for performance such as quad-port RAM, CAM, general purpose PLLs, and dedicated circuitry for implementing multiplier circuits. Table 4 shows Mercury performance.

Table 4. Mercury Performance

Application	Resources Used		Performance			
	LEs	ESBs	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Units
16-bit loadable counter *(1)*	16	0	400	400	400	MHz
32-bit loadable counter *(1)*	32	0	400	400	400	MHz
32-bit accumulator *(1)*	32	0	400	400	400	MHz
32-to-1 multiplexer	27	0	1.864	2.466	2.723	ns
32 × 64 asynchronous FIFO	103	2	290	258	242	MHz
8-bit, 37-tap FIR filter	251	1	290	240	205	MSPS

Note to Table 4:

(1) The clock tree supports up to 400 MHz. Although the registered performance for these designs exceed 400 MHz, they are limited by the clock tree limit.

Configuration

The logic, circuitry, and interconnects in the Mercury architecture are configured with CMOS SRAM elements. Mercury devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different ASIC designs; Mercury devices can be configured on the board for the specific functionality required.

Mercury devices are configured at system power-up with data stored in an Altera® serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable configuration devices, which configure Mercury devices via a serial data stream. Mercury devices can be configured in under 70 ms. Moreover, Mercury devices contain an optimized interface that permits microprocessors to configure Mercury devices serially or in parallel, synchronously or asynchronously. This interface also enables microprocessors to treat Mercury devices as memory and to configure the device by writing to a virtual memory location, simplifying reconfiguration.

After a Mercury device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Software

Mercury devices are supported by the Altera Quartus™ II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap™ logic analysis, and device configuration. The Quartus II software also ships with Altera-specific HDL synthesis tools from Exemplar Logic and Synopsys, and Altera-specific Register Transfer Level (RTL) and timing simulation tools from Model Technology. The Quartus II software supports PCs running Windows 98, Windows NT 4.0, and Windows 2000; UNIX workstations running Solaris 2.6, 7, or 8, or HP-UX 10.2 or 11.0; and PCs running Red Hat Linux 7.1.

The Quartus II software provides NativeLink™ interfaces to other industry-standard PC- and UNIX-workstation-based EDA tools. For example, designers can invoke the Quartus II software from within the Mentor Graphics LeonardoSpectrum software, Synplicity's Synplify software, and the Synopsys FPGA *Express* software. The Quartus II software also contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for Mercury devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the Mercury architecture.

For more information on the Quartus II development system, see the *Quartus II Programmable Logic Development System & Software Data Sheet*.

Functional Description

The Mercury architecture contains a row-based logic array to implement general logic and a row-based embedded system array to implement memory and specialized logic functions. Signal interconnections within Mercury devices are provided by a series of row and column interconnects with varying lengths and speeds. The priority FastTrack Interconnect structure is faster than other interconnects; the Quartus II Compiler places design-critical paths on these faster lines to improve design performance.

Mercury devices provide four dedicated clock input pins and six dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on Mercury devices can also feed logic. Dedicated clocks can also be used with the Mercury general purpose PLLs for clock management.

Each I/O row band also provides two additional I/O pins that can drive two row-global signals. Row-global signals can drive register control inputs for the LAB row associated with that particular I/O row band.

High-Speed Differential Interface

The top I/O or HSDI band in Mercury devices contains dedicated circuitry for supporting differential standards at speeds up to 1.25 Gbps. Mercury devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, and 3.3-V PCML I/O standards. Two dedicated high-speed PLLs (separate from the general purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, clock recovery units (CRUs) at each receiver channel enable CDR. EP1M120 devices support eight input channels, eight output channels, and two dedicated clock inputs for feeding the receiver and/or transmitter PLLs. EP1M350 devices support 18 input channels, 18 output channels, and two dedicated clock inputs.

Mercury devices have optional built-in 100-Ω termination resistors on HSDI differential receiver data pins and the `HSDI_CLK1` and `HSDI_CLK2` pins.

Designers can use the HSDI circuitry for the following applications:

- Gigabit Ethernet backplanes
- ATM, SONET
- RapidIO
- POS-PHY Level 4
- Fibre Channel
- SDTV

The HSDI band supports one of two possible modes:

- Source-synchronous mode
- Clock data recovery (CDR) mode

Figure 12. Partial Product Formation

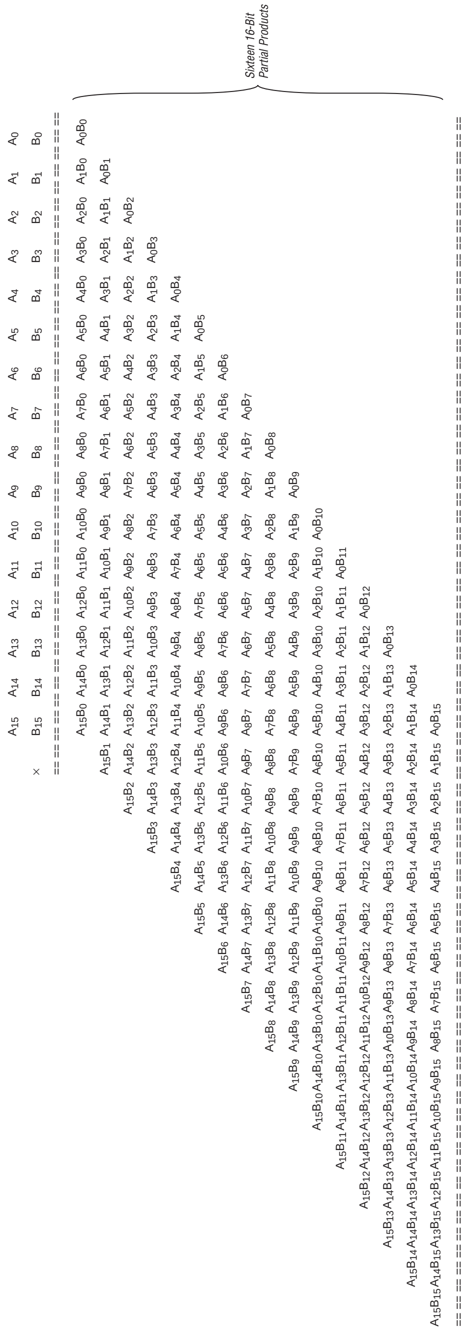
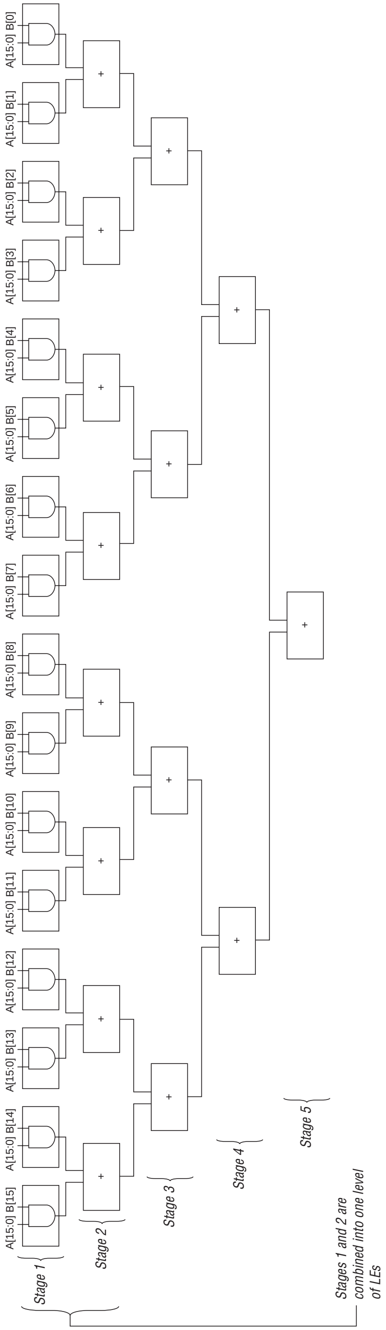


Figure 13. Mercury Binary Tree Implementation



Clear & Preset Logic Control

LAB-wide signals control logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The direct asynchronous preset does not require a NOT-gate push-back technique. Mercury devices support simultaneous preset, or asynchronous load, and clear. Asynchronous clear takes precedence if both signals are asserted simultaneously. Each LAB supports one clear and one preset signal. Two clears are possible in a single LAB by using a NOT-gate push-back technique on the preset port. The Quartus II Compiler automatically performs this second clear emulation.

In addition to the clear and preset ports, Mercury devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals.

Multi-Level FastTrack Interconnect

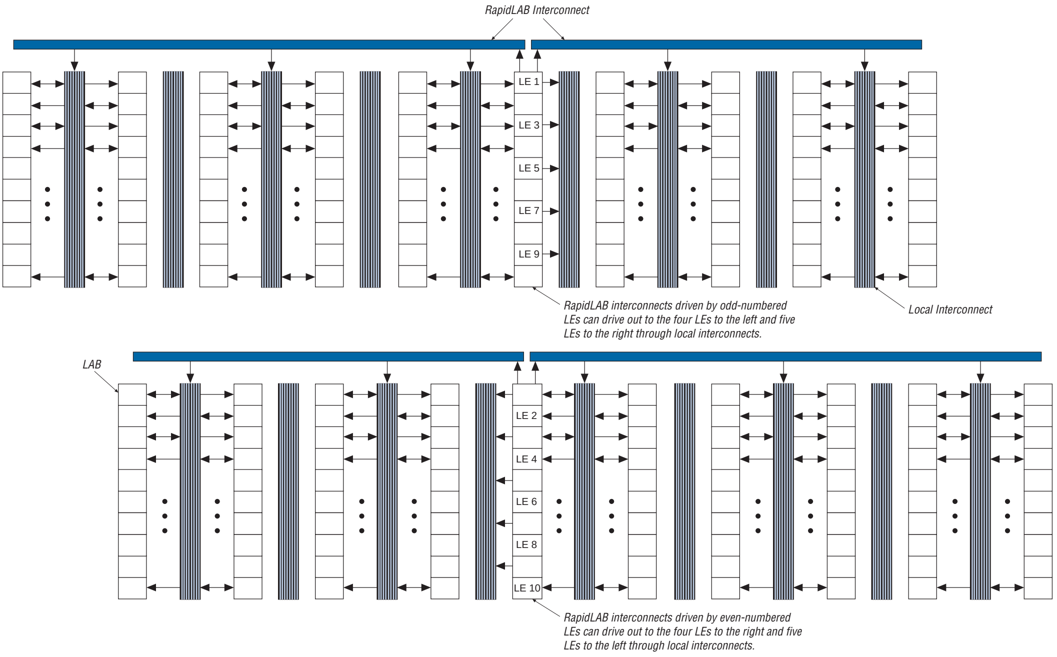
The Mercury architecture provides connections between LEs, ESBs, and device I/O pins via an innovative Multi-Level FastTrack Interconnect structure. The Multi-Level FastTrack Interconnect structure is a series of routing channels that traverse the device, providing a hierarchy of interconnect lines. Regular resources provide efficient and capable connections while priority resources and specialized RapidLAB, leap line, and FastLUT resources enhance performance by accelerating timing on critical paths. The Quartus II Compiler automatically places critical design paths on those faster lines to improve design performance.

This network of routing structures provides predictable performance, even for complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The Multi-Level FastTrack Interconnect consists of regular and priority lines that traverse column and row interconnect channels to span sections and the entire device length. Each row of LABs, ESBs, and I/O bands is served by a dedicated row interconnect, which routes signals to and from LABs, ESBs, and I/O row bands in the same row. These row resources include:

- Row interconnect traversing the entire device from left to right
- Priority row interconnect for high speed access across the length of the device
- RapidLAB interconnect for horizontal routing that traverses a 10-LAB-wide region from a central LAB

Figure 14. RapidLAB Interconnect Connections



RapidLAB interconnects driven by odd-numbered LEs can drive out to the four LEs to the left and five LEs to the right through local interconnects.

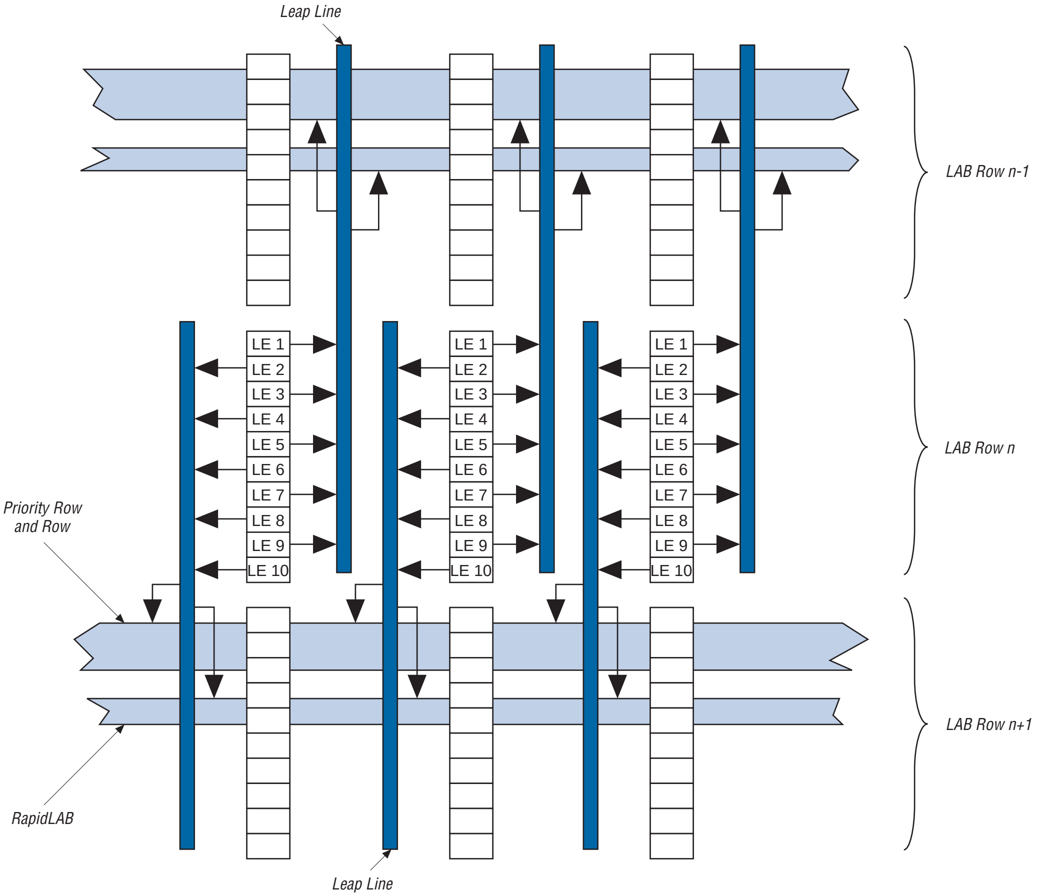
RapidLAB interconnects driven by even-numbered LEs can drive out to the four LEs to the right and five LEs to the left through local interconnects.

The column interconnect vertically routes signals to and from LABs, ESBs, and I/O bands. Each column of LABs is served by a dedicated column interconnect. These column resources include:

- Column interconnect traversing the entire device from top to bottom
- Priority column interconnect for high speed access across the device vertically
- Leap line interconnect for vertical routing between adjacent LAB rows and between adjacent ESP rows and LAB rows.

Leap lines are driven directly by LEs for fast access to adjacent row interconnects. LABs can drive a leap line to the row above and/or below (including ESB rows). The even-numbered LEs in a LAB drive leap lines down, while odd-numbered LEs drive leap lines up. This allows a single LAB to access row and RapidLAB interconnects within a three-row region. Figure 15 shows the leap line interconnect.

Figure 15. Leap Line Interconnect



FastLUT Interconnect

Mercury devices include an enhanced interconnect structure within LABs for faster routing of LE output to LE input connections. The FastLUT connection allows the combinatorial output of an LE to directly drive the fast input of the LE directly below it, bypassing the local interconnect. This resource can be used as a high speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. Figure 16 shows a FastLUT interconnect.

Table 9 summarizes how various elements of the Mercury architecture drive each other.

Table 9. Mercury Routing Scheme

Source	Destination										
	LE	Local Interconnect	IOE	ESB Row Interconnect	ESB	Row	Priority Row	RapidLAB Interconnect	Column	Priority Column	Leap Lines
LE	✓ (1)	✓				✓	✓	✓	✓	✓	✓
Local Interconnect	✓		✓								
IOE		✓ (2)				✓ (3)	✓ (3)		✓	✓	
ESB Row Interconnect					✓						
ESB				✓					✓	✓	✓
Row		✓									
Priority Row		✓									
RapidLAB Interconnect	✓ (4)	✓									
Column				✓		✓	✓		✓		
Priority Column				✓			✓	✓	✓	✓	
Leap Lines				✓		✓	✓	✓	✓		

Notes to Table 9:

(1) This direct connection is possible through the FastLUT connection.
(2) IOEs can connect to the adjacent LAB's local interconnects in the associated LAB row.
(3) IOEs can connect to row and priority row interconnects in the associated LAB row.
(4) This connection is used for multiplier mode.

Embedded System Block

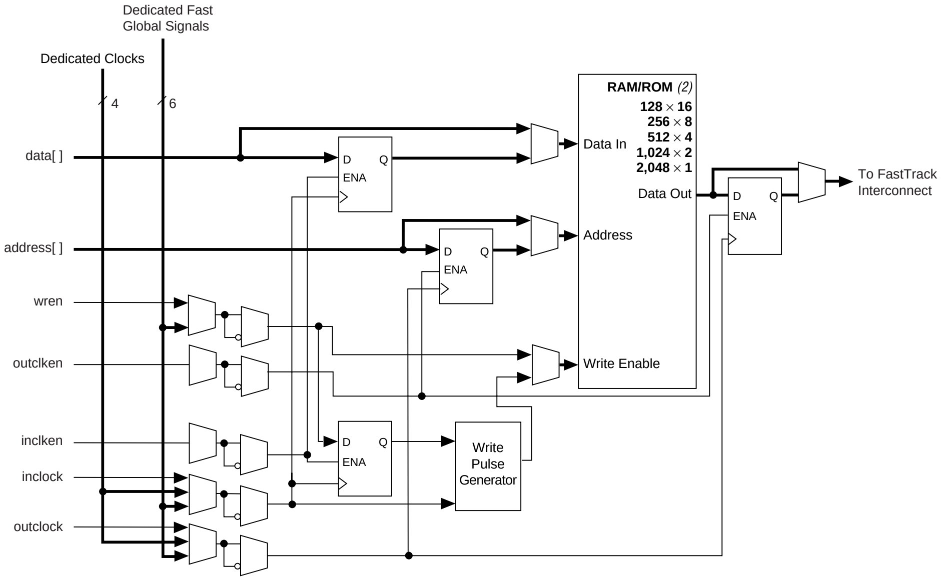
The ESB can implement various types of memory blocks, including quad-port, true dual-port, dual- and single-port RAM, ROM, FIFO, and CAM blocks.

The ESB includes input and output registers; the input registers synchronize reads and/or writes, and the output registers can pipeline designs to further increase system performance. The ESB offers a quad port mode, which supports up to four port operations, two reads and two writes simultaneously, with the ability for a different clock on each of the four ports. Figure 17 shows the ESB quad-port block diagram.

Single-Port Mode

The Mercury device's ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 21. A single ESB can support up to two single-port mode RAMs.

Figure 21. ESB in Single-Port Mode Note (1)



Notes to Figure 21:

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or chip-wide reset.

(2) If there is only one single-port RAM block in an ESB, it can support the following configurations: 4,096 × 1; 2,048 × 2; 1,028 × 4; 512 × 8; 256 × 16; or 128 × 32.

Content-Addressable Memory

Mercury devices can implement CAM in ESBs. CAM can be thought of as the inverse of RAM. RAM stores data in a specific location; when the system submits an address, the RAM block provides the data. Conversely, when the system submits data to CAM, the CAM block provides the address where the data is found. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

Table 12 describes the I/O standards supported by Mercury devices.

Table 12. Mercury Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
3.3-V PCML	Differential	N/A	3.3	3.3
GTL+	Voltage referenced	1.0	N/A	1.5
HSTL class I and II	Voltage referenced	0.75	1.5	0.75
SSTL-2 class I and II	Voltage referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage referenced	1.5	3.3	1.5
AGP	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

Each regular I/O band row contains two I/O banks. The number of I/O banks in a Mercury device depends on the number of I/O band rows. The top I/O band contains four regular I/O banks specifically designed for HSDI. The top I/O band banks and dedicated clock inputs support LVDS, LVPECL, and 3.3-V PCML. 3.3-V PCML is an open-drain standard and therefore requires external termination to 3.3 V. All other standards are supported by all I/O banks. The top I/O banks 1, 2, 3, and 4 only support non-HSDI I/O pins if the design does not use HSDI circuitry. If the design uses any HSDI channel, banks 1, 2, 3, and 4 all do not support regular I/O pins.

Additionally, the EP1M350 device includes the Flexible-LVDS feature, providing support for up to 100 LVDS channels on all regular I/O banks. Regular I/O banks in EP1M350 devices include dedicated LVDS input and output buffers that do not require any external components except for 100-Ω termination resistors on receiver channels.

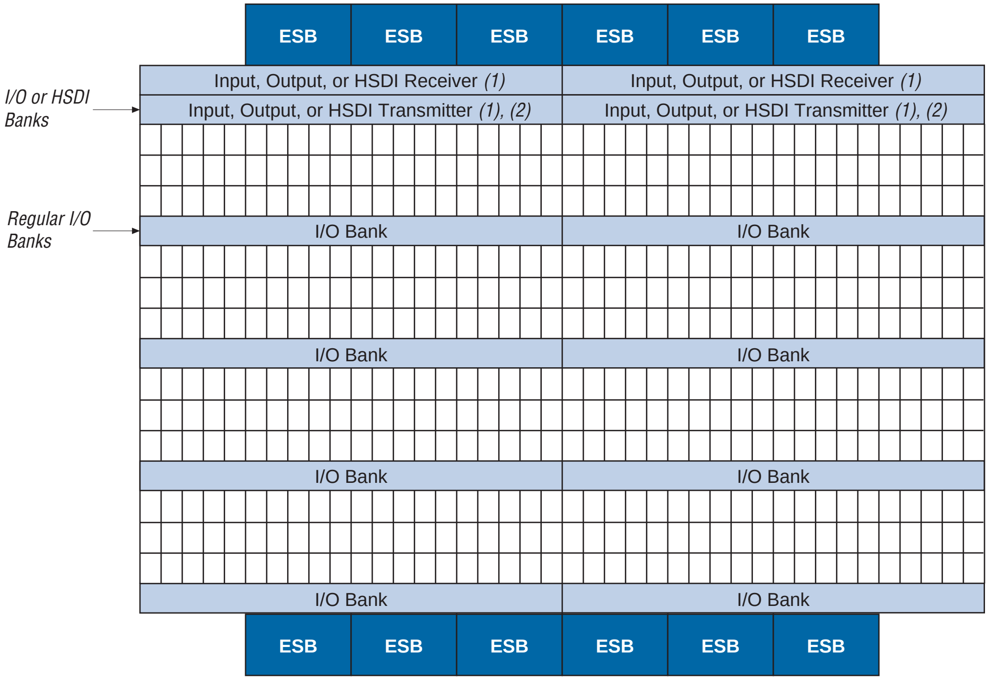
For the HSDI I/O band, half of the dedicated banks support LVDS, 3.3-V PCML or LVPECL, and receiver inputs, while the other half support LVDS, PCML or LVPECL, and transmitter outputs. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a V_{CCIO} standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. A bank can support a single V_{REF} level. Each bank contains a fixed `VREF` pin for voltage referenced standards. This pin can be used as a regular I/O if a V_{REF} standard is not used. Table 13 shows the number of I/O banks in each Mercury device.

Table 13. Number of I/O Banks per Device

Device	Regular I/O Banks	HSDI Band I/O Banks
EP1M120	8	4
EP1M350	12	4

Each bank can support multiple standards with the same V_{CCIO} for output pins. For EP1M120 devices, each bank can support one voltage-referenced I/O standard, but can support multiple I/O standards with the same V_{CCIO} and V_{REF} voltage levels. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs. Figure 30 shows the I/O bank layout for an EP1M120 device. For EP1M350 devices, each bank can support two voltage-reverenced I/O standards; each I/O bank is split into two voltage-referenced sub-banks. When using the two HSDI transmitter banks as regular I/O banks in a non-HSDI mode, those two banks require the same V_{CCIO} level. However, each HSDI transmitter bank supports its own V_{REF} level.

Figure 30. I/O Bank Layout



Notes to Figure 30:

(1) If HSDI I/O channels are not used, the HSDI banks can be used as regular I/O banks.

(2) When used as regular I/O banks, these banks must be set to the same V_{CCIO} level, but can have separate V_{REF} bank settings.

For more information on I/O standards, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

MultiVolt I/O Interface

The Mercury architecture supports the MultiVolt I/O interface feature, which allows Mercury devices in all packages to interface with devices with different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- Jam Programming & Test Language Specification

Generic Testing

Each Mercury device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for Mercury devices are made under conditions equivalent to those shown in Figure 33. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 35. Transmitter Output Waveforms for Differential I/O Standards

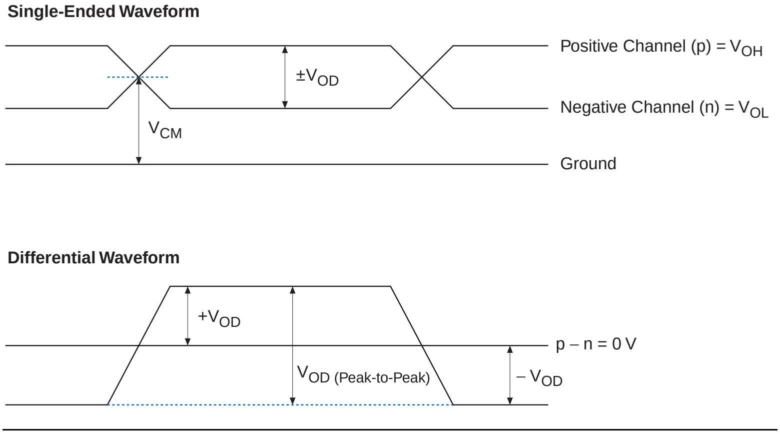


Table 27. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250	510	600	mV
Δ V_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
Δ V_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to Mercury devices)		90	100	110	Ω

Table 30. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.3 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	$I_{OUT} = -500$ µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	$I_{OUT} = 1{,}500$ µA			$0.1 \times V_{CCIO}$	V

Table 31. PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	$I_{OUT} = -500$ µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	$I_{OUT} = 1{,}500$ µA			$0.1 \times V_{CCIO}$	V
L_{PIN}	Pin inductance				15	nH

Table 32. GTL+ I/O Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		$V_{REF} + 0.1$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.1$	V
V_{OL}	Low-level output voltage	$I_{OL} = 34$ mA			0.65	V

Table 36. SSTL-3 Class II Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA			V_{TT} – 0.8	V

Table 37. 3.3-V AGP -2X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		0.39 × V_{CCIO}		0.41 × V_{CCIO}	V
V_{IH}	High-level input voltage *(12)*		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(12)*				0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	0.9 × V_{CCIO}		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			0.1 × V_{CCIO}	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$			±10	µA

Table 38. 3.3-V AGP -1X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(12)*		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(12)*				0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	0.9 × V_{CCIO}		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			0.1 × V_{CCIO}	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$			±10	µA

Table 39. 1.5-V HSTL Class I Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.3		$V_{REF} – 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} – 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = 8$ mA	$V_{CCIO} – 0.4$			V
V_{OL}	Low-level output voltage	$I_{OH} = –8$ mA			0.4	V

Table 40. 1.5-V HSTL Class II Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.3		$V_{REF} – 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} – 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = 16$ mA	$V_{CCIO} – 0.4$			V
V_{OL}	Low-level output voltage	$I_{OH} = –16$ mA			0.4	V

Table 41. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$			V
V_{IL}	Low-level input voltage				$V_{REF} – 0.2$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$			±10	µA
V_{OH}	High-level output voltage	$I_{OH} = –8$ mA	$V_{REF} + 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA			$V_{REF} – 0.4$	V
I_O	Output leakage current (when output is high *Z*)	GND ð V_{OUT} ð V_{CCIO}			±10	µA

Table 51. EP1M350 External Bidirectional Timing Parameters *Note (1)*

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	0.60		0.57		0.71		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	3.95	2.00	3.97	2.00	4.75	ns
$t_{XZBIDIR}$		3.90		3.93		4.70	ns
$t_{ZXBIDIR}$ (2)		3.90		3.93		4.70	ns
$t_{ZXBIDIR}$ (3)		4.10		4.13		4.94	ns
$t_{INSUBIDIRPLL}$	0.69		0.70		0.82		ns
$t_{INHBIDIRPLL}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.23	0.50	2.23	0.50	2.69	ns
$t_{XZBIDIRPLL}$		2.19		2.18		2.63	ns
$t_{ZXBIDIRPLL}$ (2)		2.19		2.18		2.63	ns
$t_{ZXBIDIRPLL}$ (3)		2.39		2.38		2.87	ns

Notes to Tables 46 – 51:

(1) Timing will vary by I/O pin placement. Therefore, use the Quartus II software to determine exact I/O timing for each pin.

(2) This parameter is measured with the **Increase t_{ZX} Delay to Output Pin** option set to **Off**.

(3) This parameter is measured with the **Increase t_{ZX} Delay to Output Pin** option set to **On**.

Power Consumption

Detailed power consumption information for Mercury devices will be released when available.

Configuration & Operation

The Mercury architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The Mercury architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up and before and during configuration. Together, the configuration and initialization processes are called command mode; normal device operation is called user mode.