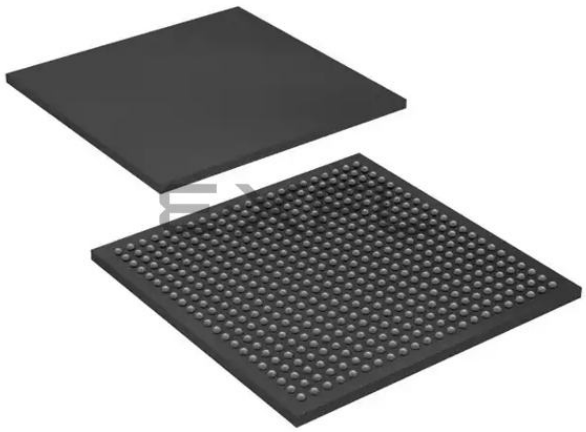

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4800
Total RAM Bits	49152
Number of I/O	303
Number of Gates	120000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1m120f484i6

…and More Features

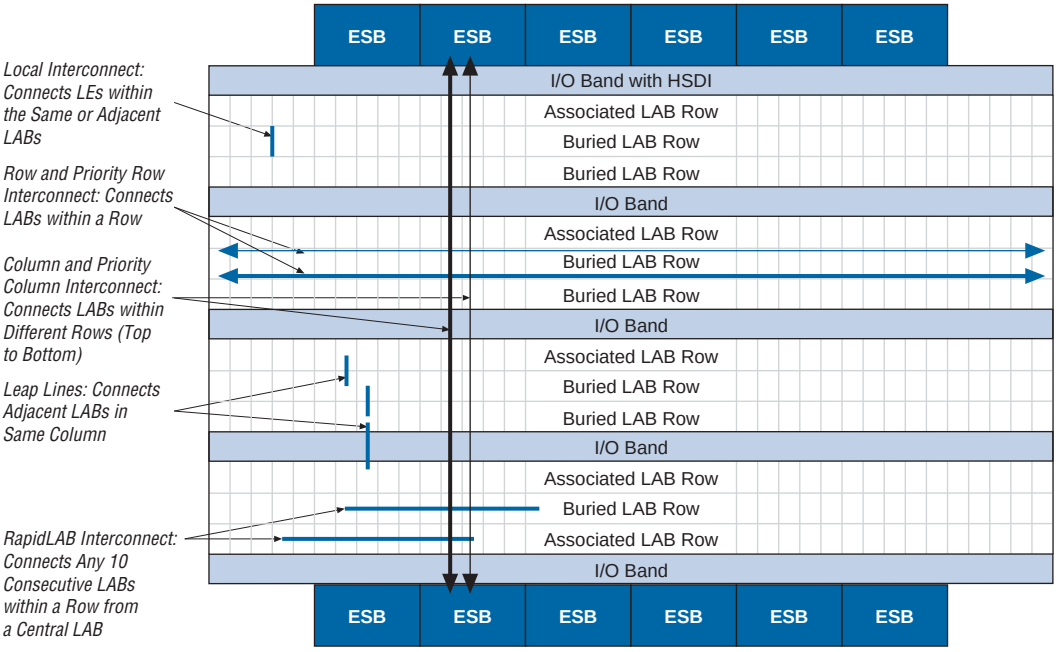
- Advanced high-speed I/O features
  - Robust I/O standard support, including LVTTL, PCI up to 66 MHz, 3.3-V AGP in 1× and 2× modes, 3.3-V SSTL-3 and 2.5-V SSTL-2, GTL+, HSTL, CTT, LVDS, LVPECL, and 3.3-V PCML
  - High-speed differential interface (HSDI) with dedicated circuitry for CDR at up to 1.25 Gbps for LVDS, LVPECL, and 3.3-V PCML
  - Support for source-synchronous True-LVDS™ circuitry up to 840 megabits per second (Mbps) for LVDS, LVPECL, and 3.3-V PCML
  - Up to 18 input and 18 output dedicated differential channels of high-speed LVDS, LVPECL, or 3.3-V PCML
  - Built-in 100-Ω termination resistor on HSDI data and clock differential pairs
  - Flexible-LVDS™ circuitry provides 624-Mbps support on up to 100 channels with the EP1M350 device
  - Versatile three-register I/O element (IOE) supporting double data rate I/O (DDRIO), double data-rate (DDR) SDRAM, zero bus turnaround (ZBT) SRAM, and quad data rate (QDR) SRAM
- Designed for low-power operation
  - 1.8-V internal supply voltage (V_{CCINT})
  - MultiVolt™ I/O interface voltage levels (V_{CCIO}) compatible with 1.5-V, 1.8-V, 2.5-V, and 3.3-V devices
  - 5.0-V tolerant with external resistor
- Advanced interconnect structure
  - Multi-level FastTrack® Interconnect structure providing fast, predictable interconnect delays
  - Optimized high-speed Priority FastTrack Interconnect for routing critical paths in a design
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - FastLUT™ connection allowing high speed direct connection between LEs in the same logic array block (LAB)
  - Leap lines allowing a single LAB to directly drive LEs in adjacent rows
  - The RapidLAB interconnect providing a high-speed connection to a 10-LAB-wide region
  - Dedicated clock and control signal resources, including four dedicated clocks, six dedicated fast global signals, and additional row-global signals

Mercury device I/O pins are evenly distributed across the entire device area; other Altera device families have I/O pins placed on the device periphery. Mercury device I/O pin placement allows for higher I/O count at a given die size; pad size is no longer a limiting issue. Each I/O pin is fed by an IOE. IOEs are grouped in IOE row bands from the top to the bottom of the device. IOE row bands are separated by several LAB rows. LABs from the associated LAB row closest to the I/O row band drive IOEs through the local interconnect. This feature allows fast clock-to-output times when a pin is driven by any of the 10 LEs in the adjacent associated LAB. Each IOE contains a bidirectional buffer along with an input register, output register, output enable (OE) register, and input latch for DDR. When used with a global clock, these dedicated registers provide exceptional bidirectional I/O performance.

IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; 3.3-V, 64-bit, 133-MHz PCI-X compliance; Joint Test Action Group (JTAG) boundary-scan test (BST) support; output drive strength control; slew-rate control; tri-state buffers; bus-hold circuitry; programmable pull-up resisters; programmable input and output delays; and open-drain outputs. Mercury devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, HSTL, LVPECL, 3.3-V PCML, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, CTT, and 3.3-V AGP I/O standards. CDR (up to 1.25 Gbps) and source-synchronous (up to 840 Mbps) transfers are supported with HSDI circuitry for LVDS, LVPECL, and 3.3-V PCML I/O standards.

The ESB can implement a variety of memory functions, including CAM, quad-port RAM, true dual-port RAM, dual- and single-port RAM, ROM, and FIFO functions. ESBs are grouped into two rows: one at the top and one at the bottom of the device. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs, in conjunction with the ability for one ESB to implement two separate memory blocks, ensures that the Mercury device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures the implemention of small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the Mercury device.

Figure 1. Mercury Architecture Block Diagram *Note (1)*



Note to Figure 1:

(1) Figure 1 shows an EP1M120 device. Mercury devices have a varying number of rows, columns, and ESBs, as shown in Table 5.

Table 5 lists the resources available in Mercury devices.

Table 5. Mercury Device Resources

Device	LAB Rows	LAB Columns	I/O Row Bands	ESBs
EP1M120	12	40	5	12
EP1M350	18	80	4	28

Notes to Figure 4:

(1) EP1M350 devices have 18 individual receiver and transmitter channels. EP1M120 devices have 8 individual receiver and transmitter channels. Receiver and transmitter channel numbers in parenthesis are for EP1M350 devices.
(2) *W* = 1 to 12, 14, 16, 18, or 20
J = 3 to 12, 14, 16, 18, or 20
W does not have to equal *J*.
(3) For every receiver channel in EP1M350 and EP1M120 devices, the ÷*J* recovered clock can drive the priority column interconnect for use as a clock.
(4) The two center channels adjacent to the HSDI PLLs (channels 4 and 5 for EP1M120 devices, channels 9 and 10 for EP1M350 devices) can drive the Mercury device's global clocks.
(5) `HSDI_CLK1` and `HSDI_CLK2` pins must be differential. These clock pins drive HSDI PLLs only. They do not drive to the logic array.

The multiplied reference clock is also used to synchronize and serialize at the transmitter side.

Up to two different serial data rates are supported for input channels or output channels. Received data must be non-return-to-zero (NRZ).

Table 7 defines the support for CDR-mode applications. Table 8 shows the supported data rates for each speed grade.

Table 7. CDR-Mode Applications

Data Rate	CDR Mode					
	DC-Coupled LVDS	DC-Coupled LVPECL	DC-Coupled 3.3-V PCML	AC-Coupled LVDS *(1)*	AC-Coupled LVPECL *(1)*	AC-Coupled 3.3-V PCML *(1)*
1.0 to 1.25 Gbps	*(2)*	✓	✓	✓	✓	✓
≤ 1.0 Gbps	✓	✓	✓	✓	✓	✓

Notes to Table 7:

(1) The V_{CM} operating range for AC-coupled applications is from 0 to 0.7 V and from 1.8 to 2.4 V.
(2) Use AC-coupled LVDS or another I/O standard. The DC-coupled LVDS I/O standard provides performance up to 1.0 Gbps.

For more information on CDR, see *AN 130: CDR in Mercury Devices*.

Each LE has two outputs that drive the local, row, and column routing resources. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output, while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

LE Operating Modes

The Mercury LE can operate in one of the following modes:

- Normal
- Arithmetic
- Multiplier

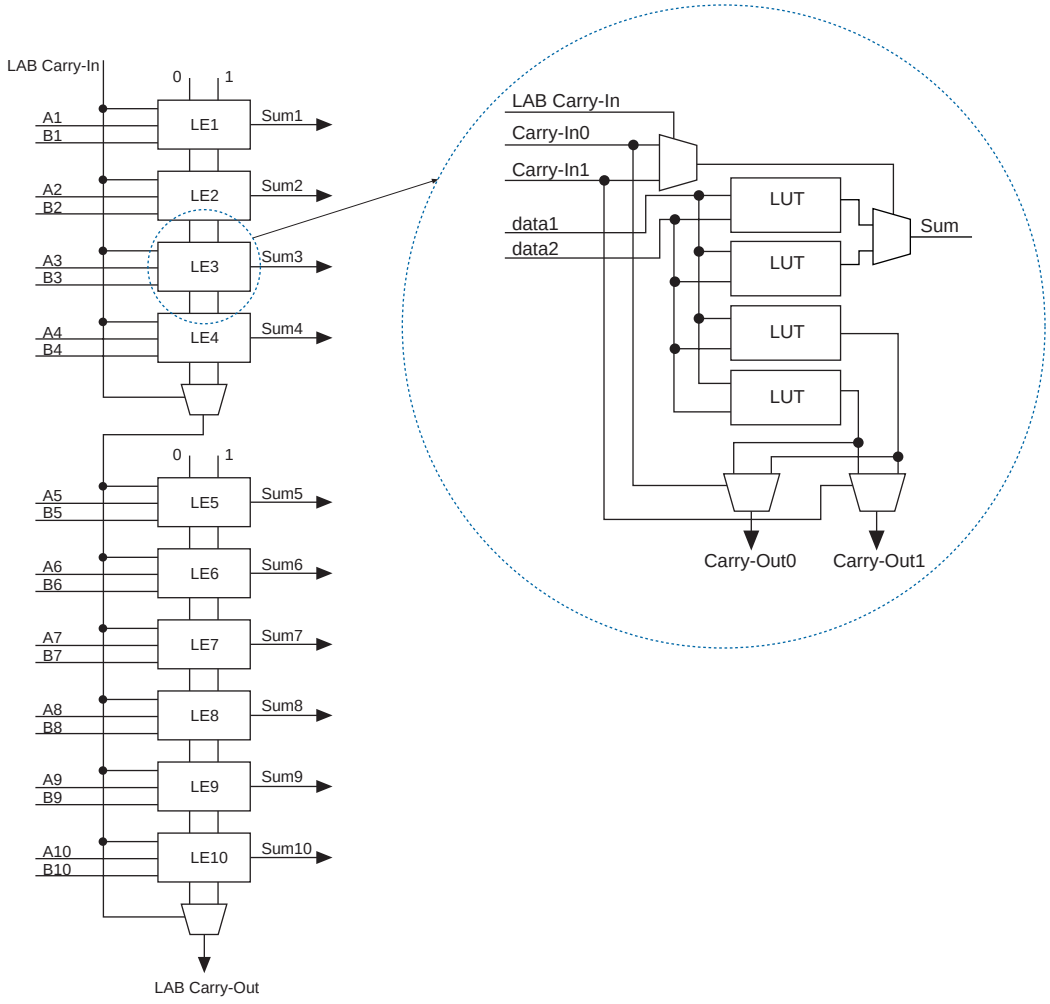
Each operating mode uses LE resources differently. In each operating mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0`, `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain generation; and the FastLUT Connection input from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all normal and arithmetic LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions, such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect and a single carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. The LUT (combinatorial) output can be driven to the FastLUT connection to the next LE in the LAB. LEs in normal mode support packed registers. Figure 8 shows an LE in normal mode.

Figure 10. CSLA Details



The Quartus II Compiler can create CSLA logic automatically during design processing. Alternatively, the designer can create CSLA logic manually during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips intermediate LABs in a row structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in a LAB row carries to the first LE of the third LAB in the same LAB row.

Multiplier Mode

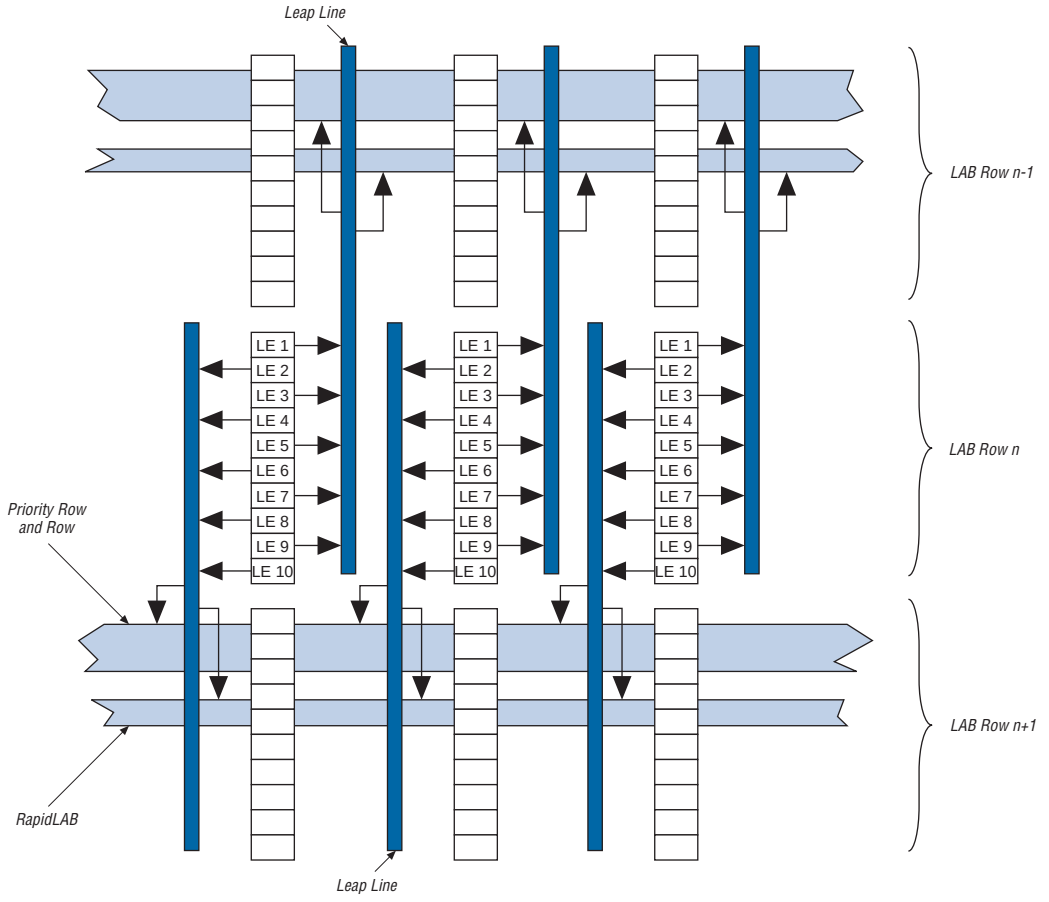
Multiplier mode is used for implementing high-speed multipliers up to 16×16 in size. The LUT implements the partial product formation and summation in a single stage for a $N \times M$-bit multiply operation. A single LE can implement the summation of $A_N B_{M+1} + A_{N+1} B_M$ for the multiplier and multiplicand inputs. To increase the speed of the multiplication, LAB wide signals are used to control the partial product sum generation. These multiplier LAB-wide signals use the LABCLKENA1 and PRESET/ASYNCLOAD resources. The multiplier mode takes advantage of the CSLA circuitry for optimized sum and carry generation in the partial product sum. There is a special CSLA circuitry mode used for the multiplier where the carry chain runs vertically between LABs in the same column. The Quartus II Compiler automatically uses this special mode for dedicated multiplier implementation only. The summation of the multiplier and multiplicand bits is driven out along with the carry-out0 and carry-out1 bits. The combinatorial or registered versions of the sum can be driven out, allowing the multiplier to be pipelined.

The RapidLAB interconnect has dedicated fast connections to the LE inputs in multiplier mode, further increasing the speed of the multiplier. These dedicated connections allow RapidLAB lines to avoid delay incurred by driving onto local interconnects and then into the LE.

The Quartus II software implements parameterized functions that use the multiplier mode automatically when multiply operators are used.

Figure 11 shows a Mercury device LE in multiplier mode.

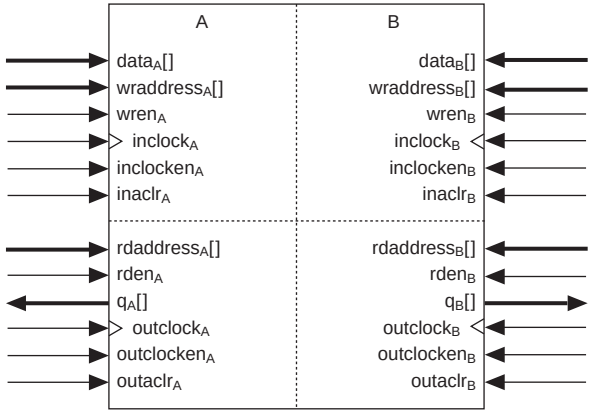
Figure 15. Leap Line Interconnect



FastLUT Interconnect

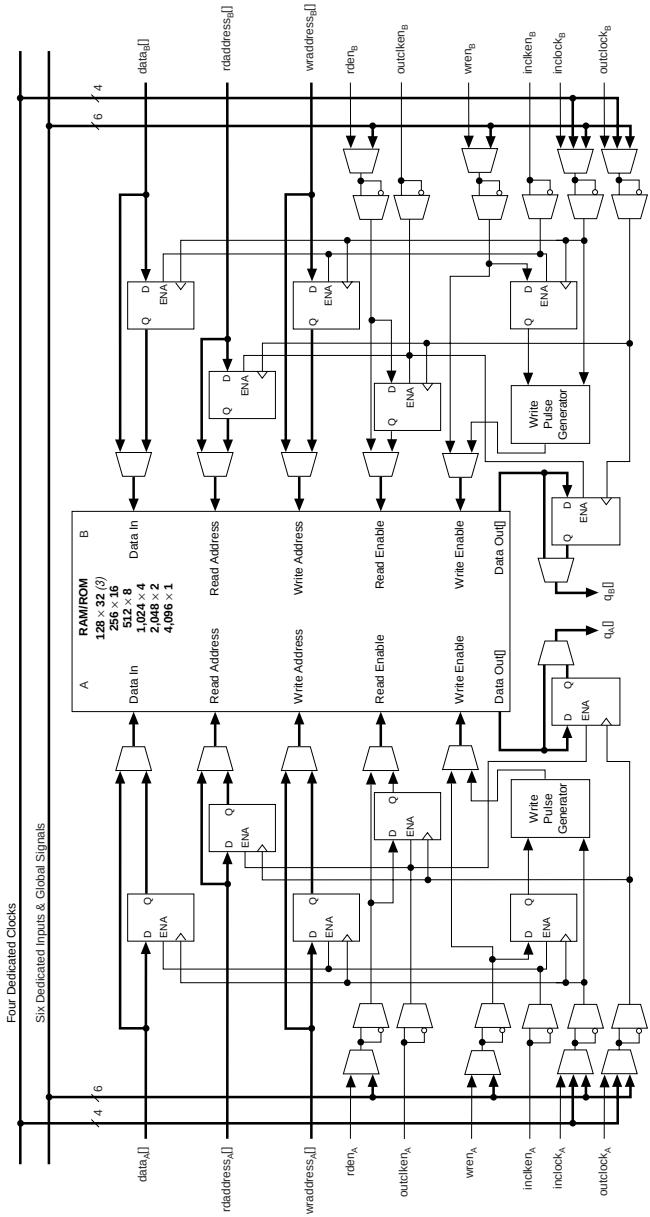
Mercury devices include an enhanced interconnect structure within LABs for faster routing of LE output to LE input connections. The FastLUT connection allows the combinatorial output of an LE to directly drive the fast input of the LE directly below it, bypassing the local interconnect. This resource can be used as a high speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. Figure 16 shows a FastLUT interconnect.

Figure 17. ESB Quad-Port Block Diagram



In addition to quad port memory, the ESB also supports true dual-port, dual-port, and single-port RAM. True dual-port RAM supports any combination of two port operations: two reads, two writes, or one read and one write. Dual-port memory supports a simultaneous read and write. For single-port memory, independent read and write is supported. Figure 18 shows these different RAM memory port configurations for an ESB.

Figure 19. ESB in Read/Write Clock Mode *Notes (1), (2)*



Notes to Figure 19:

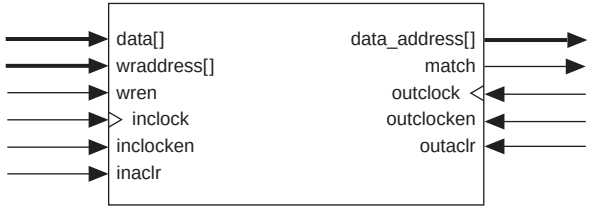
(1) Only half of the ESB, either A or B, is used for dual-port configuration.
(2) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(3) This configuration is supported for dual-port configuration.

Input/Output Clock Mode

An ESB using input/output clock mode can also use up to four clocks. On each of the two ports, A or B, one clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. Each ESB port, A or B, also supports independent read clock enable, write clock enable, and asynchronous clear signals. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 20 shows the ESB in input/output clock mode.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. CAM is ideally suited for applications such as Ethernet address lookup, data compression, pattern recognition, cache tags, fast routing table lookup, and high-bandwidth address filtering. Figure 22 shows the CAM block diagram.

Figure 22. CAM Block Diagram



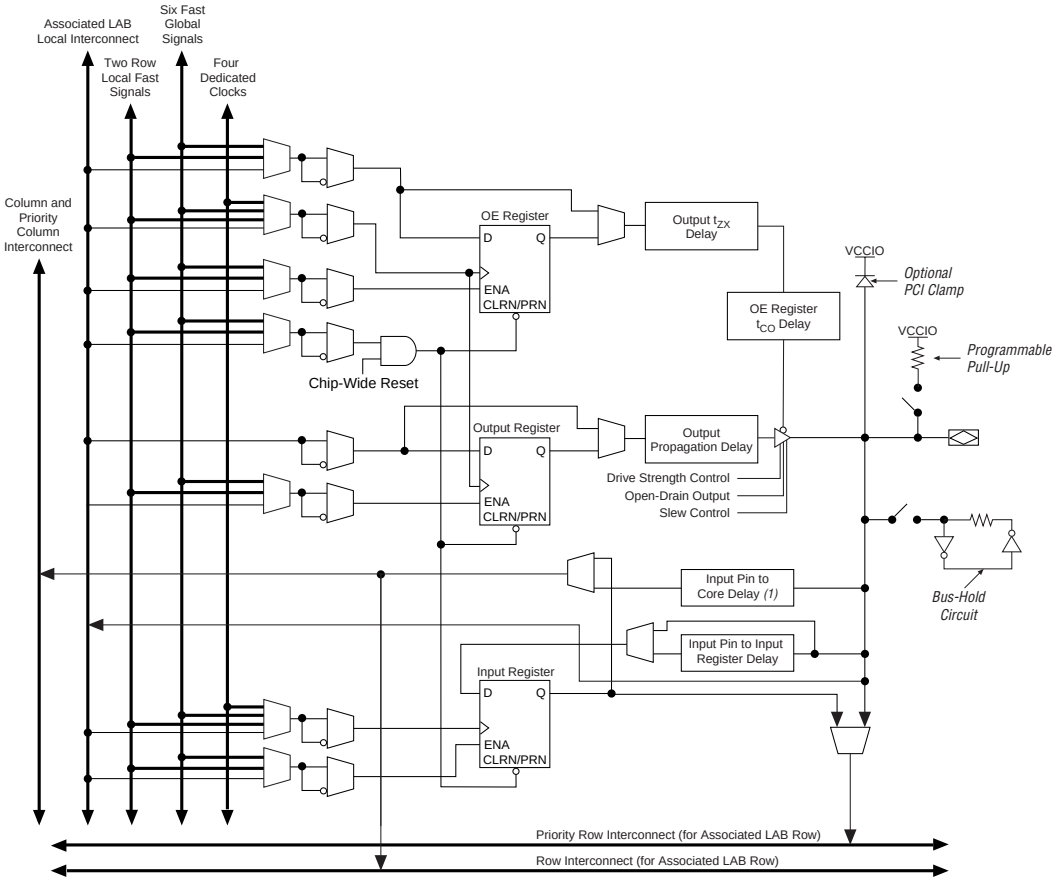
The Mercury on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the Mercury device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements a 32-word, 32-bit CAM. Wider or deeper CAM, such as a 32-word, 64-bit or 128-word, 32-bit block, can be implemented by combining multiple CAM blocks with some ancillary logic implemented in LEs. The Quartus II software automatically combines ESBs and LEs to create larger CAM blocks.

CAM supports writing “don’t care” bits into words of the memory. The don’t-care bit can be used as a mask for CAM comparisons; any bit set to don’t-care has no effect on matches.

CAM can generate outputs in three different modes: single-match mode, multiple-match mode, and fast multiple-match mode. In each mode, the ESB outputs the matched data’s location as an encoded or unencoded address. When encoded, the ESB outputs an encoded address of the data’s location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, each ESB port uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. Figures 22 and 23 show the encoded CAM outputs and unencoded CAM outputs, respectively.

Figure 26. Mercury IOE



Note to Figure 26:
(1) This programmable delay has four settings: off and three levels of delay.

Double Data Rate I/O

Mercury device's have three register IOEs to support the DDRIO feature, which makes double data rate interfaces possible by clocking data on both positive and negative clock edges. The IOE in Mercury devices supports double data rate input and double data rate output modes.

Table 12 describes the I/O standards supported by Mercury devices.

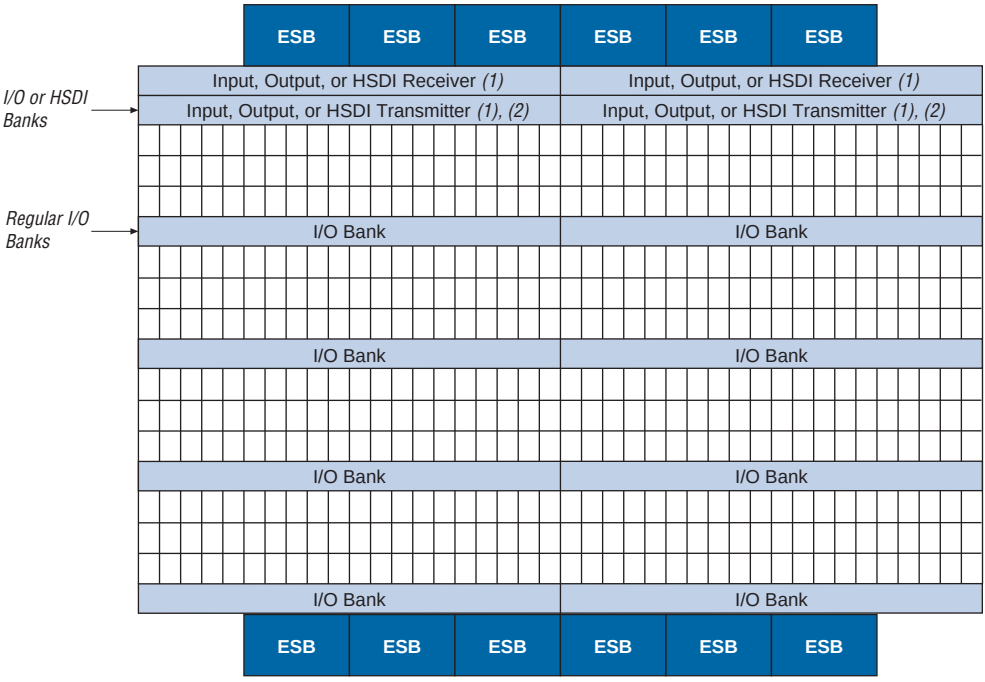
Table 12. Mercury Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
3.3-V PCML	Differential	N/A	3.3	3.3
GTL+	Voltage referenced	1.0	N/A	1.5
HSTL class I and II	Voltage referenced	0.75	1.5	0.75
SSTL-2 class I and II	Voltage referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage referenced	1.5	3.3	1.5
AGP	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

Each regular I/O band row contains two I/O banks. The number of I/O banks in a Mercury device depends on the number of I/O band rows. The top I/O band contains four regular I/O banks specifically designed for HSDI. The top I/O band banks and dedicated clock inputs support LVDS, LVPECL, and 3.3-V PCML. 3.3-V PCML is an open-drain standard and therefore requires external termination to 3.3 V. All other standards are supported by all I/O banks. The top I/O banks 1, 2, 3, and 4 only support non-HSDI I/O pins if the design does not use HSDI circuitry. If the design uses any HSDI channel, banks 1, 2, 3, and 4 all do not support regular I/O pins.

Additionally, the EP1M350 device includes the Flexible-LVDS feature, providing support for up to 100 LVDS channels on all regular I/O banks. Regular I/O banks in EP1M350 devices include dedicated LVDS input and output buffers that do not require any external components except for 100-Ω termination resistors on receiver channels.

Figure 30. I/O Bank Layout



Notes to Figure 30:

(1) If HSDI I/O channels are not used, the HSDI banks can be used as regular I/O banks.

(2) When used as regular I/O banks, these banks must be set to the same V_{CCIO} level, but can have separate V_{REF} bank settings.

For more information on I/O standards, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

MultiVolt I/O Interface

The Mercury architecture supports the MultiVolt I/O interface feature, which allows Mercury devices in all packages to interface with devices with different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The Mercury VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with HSTL systems. When VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 14 summarizes Mercury MultiVolt I/O support.

Table 14. Mercury MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8	✓ *(2)*	✓	✓	✓			✓ *(3)*			
2.5	✓ *(2)*	✓ *(2)*	✓	✓			✓ *(4)*	✓		
3.3	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓	✓ *(6)*			✓ *(5)*	✓	✓

Notes to Table 14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO} unless an external resistor is used.

(2) These input levels are only available if the input standard is set to any V_{REF}-based input standard (SSTL-2, SSTL-3, HSTL, GTL+, AGP 2×). The input buffers are powered from V_{CCINT} when using V_{REF}-based input standards. LVTTL, PCI, PCI-X, AGP 1× input buffers are powered by V_{CCIO}. Therefore, these standards cannot be driven with input levels below the V_{CCIO} setting except for when V_{CCIO} = 3.3 V and the input voltage (V_I) = 2.5 V.

(3) When V_{CCIO} = 1.8 V, the Mercury device can drive a 1.5-V device with 1.8-V tolerant inputs.

(4) When V_{CCIO} = 2.5 V, the Mercury device can drive a 1.8-V device with 2.5-V tolerant inputs.

(5) When V_{CCIO} = 3.3 V, the Mercury device can drive a 2.5-V device with 3.3-V tolerant inputs.

(6) Designers can set Mercury devices to be 5.0-V tolerant by adding an external resistor and enabling the PCI clamping diode.

Power Sequencing & Hot-Socketing

Because Mercury devices can be used in a mixed-voltage environment, the devices are designed specifically to tolerate any possible power-up sequence. Therefore, the VCCIO and VCCINT power supplies may be powered in any order.

Signals can be driven into Mercury devices before and during power-up without damaging the device. In addition, Mercury devices do not drive out during power-up. Once operating conditions are reached and the device is configured, Mercury devices operate as specified by the user.

- Normal Mode: The external clock output pin will have phase delay relative to the clock input pin. If an internal clock is used in this mode, the IOE register clock will be phase aligned to the input clock pin. Multiplication is allowed with the normal mode.

Advanced ClockShift Circuitry

General purpose PLLs in Mercury devices have advanced ClockShift™ circuitry that provides programmable phase shift and fine tune time delay shift. For phase shifting, users can enter a phase shift (in degrees or time units) that affects all PLL outputs. Phase shifts of 90, 180, and 270 can be implemented exactly. Other values of phase shifting, or delay shifting in time units, are allowed with a resolution range of 0.3 ns to 1.0 ns. This resolution varies with frequency input and the user-entered multiplication and division factors. The phase shift ability is only possible on a multiplied or divided clock if the input and output frequency have an integer multiple relationship (i.e., f_{IN} / f_{OUT} or f_{OUT} / f_{IN} must be an integer).

In addition to the phase shift feature that affects all outputs, there is an advanced fine time delay shift control on each of the four PLL outputs. Each PLL output can be shifted in 250-ps increments for a range of –2.0 ns to +2.0 ns. This ability can be used in conjunction with the phase shifting ability that affects all outputs. f_{IN} / f_{OUT} does not need to have an integer relationship for the advanced fine time delay shift control.

Clock Enable Signal

Mercury PLLs have a CLKLK_ENA pin for enabling / disabling all of the device PLLs. When the CLKLK_ENA pin is high, the PLL drives a clock to all its output ports. When the CLKLK_ENA pin is low, the clock0, clock1, clock2 and extclock ports are driven by GND and all of the PLLs go out of lock. When the CLKLK_ENA pin goes high again, the PLL must relock.

The individual enable port for each general purpose PLL is programmable. If more than one general-purpose PLL is instantiated, each one does not have to use the clock enable. To enable / disable the device PLLs with the CLKLK_ENA pin, the inclocken port on the altclklock instance must be connected to the CLKLK_ENA input pin.

Table 33. SSTL-2 Class I Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA			V_{TT} – 0.57	V

Table 34. SSTL-2 Class II Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA			V_{TT} – 0.76	V

Table 35. SSTL-3 Class I Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{TT} – 0.6	V

Table 39. 1.5-V HSTL Class I Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA			0.4	V

Table 40. 1.5-V HSTL Class II Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA			0.4	V

Table 41. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	0 < V_{IN} < V_{CCIO}			±10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ð V_{OUT} ð V_{CCIO}			±10	µA

Revision History

The information contained in the *Mercury Programmable Logic Device Family Data Sheet* version 2.2 supersedes information published in previous versions.

Version 2.2

The following changes were made to the *Mercury Programmable Logic Device Family Data Sheet* version 2.2:

- Updated the condition values (symbols I_I and I_{OZ}) in Table 22.

Version 2.1

The following changes were made to the *Mercury Programmable Logic Device Family Data Sheet* version 2.1:

- Updated Table 8.
- Updated EP1M350 regular I/O banks in Table 13.
- Updated *Note (6)* in Table 14.

Version 2.0

The following changes were made to the *Mercury Programmable Logic Device Family Data Sheet* version 2.0:

- Changed all references to PCML to 3.3-V PCML.
- Updated Table 4.
- Updated "High-Speed Differential Interface" on page 8.
- Added Tables 6 through 8.
- Added Figures 34 and 35.
- Updated I/O specifications in Tables 28 and 29.
- Updated Mercury device capacitance in Table 43.
- Updated EP1M120 device timing in Tables 46 through 49.
- Added EP1M350 device timing in Tables 50 and 51.