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Understanding Embedded - FPGAs (Field Programmable Gate Array)

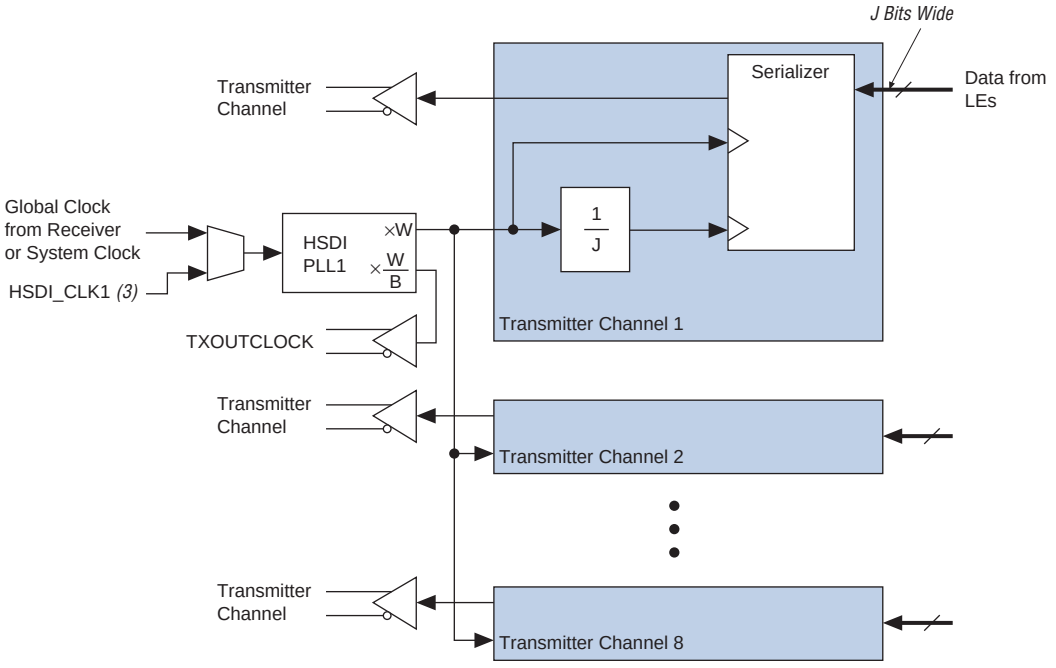
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	486
Number of Gates	-
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1m350f780c6

Figure 3. Transmitter Diagram for Source Synchronous Mode *Notes (1), (2)*



Notes to Figure 3:

(1) EP1M350 devices have 18 individual transmitter channels. EP1M120 devices have 8 individual transmitter channels.

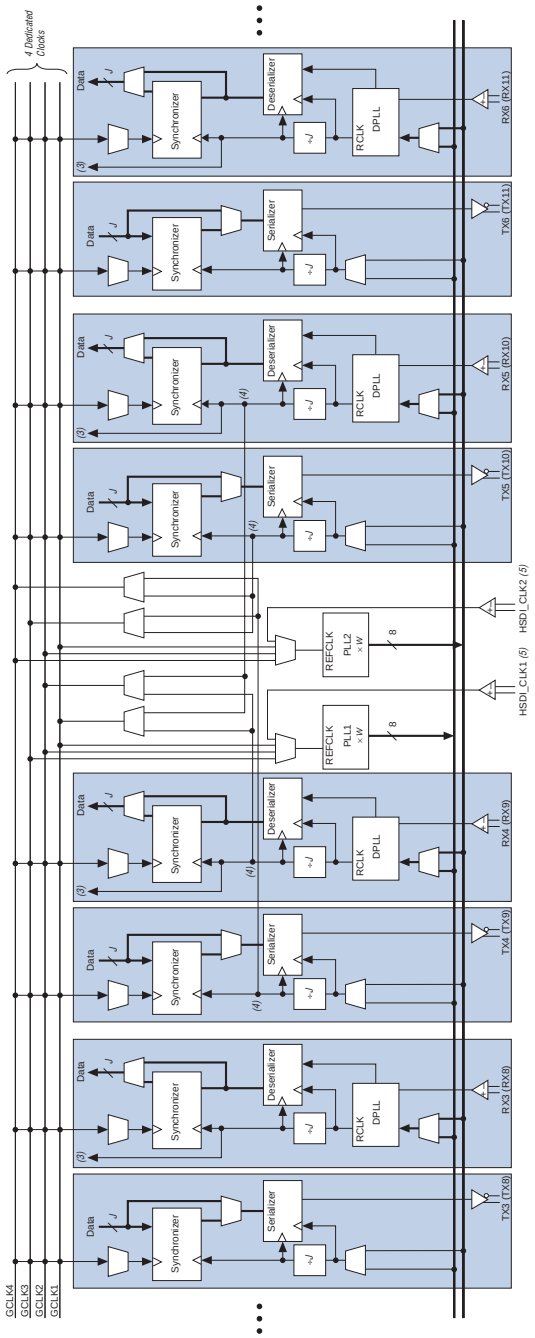
(2) *W* = 1 to 12, 14, 16, 18, or 20
B = 1 to 12, 14, 16, 18, or 20
J = 4, 7, 8, 9 to 12, 14, 16, 18, or 20
W, *B*, and *J* do not have to be equal.

(3) This clock pin drives an HSDI PLL only. It does not drive to the logic array.

The Mercury device's source-synchronous mode also supports the RapidIO interface protocol at up to 500 Mbps using the LVDS I/O standard.

For more information on source synchronous interfacing see *AN 159: Using HSDI in Source-Synchronous Mode in Mercury Devices*.

Figure 4. Receiver & Transmitter Diagrams for CDR Mode *Notes (1), (2)*



Mercury device HSDI performance is finalized for certain speed grades. Also, the industrial-grade CDR specification is the same as the -6 speed grade for commercial-grade CDR specification. See Table 8.

Table 8. CDR & Source-Synchronous Data Rates

Device	Speed Grade	Number of Channels	Maximum CDR Data Rate (Gbps)	Maximum Source-Synchronous Data Rate (Mbps)
EP1M120	-5	8	1.25	840
	-6 *(1)*	8	1.25	840
	-7	8	1.0	840
EP1M350	-5	18	1.25	840
	-6 *(1)*	8 *(2)*	1.25	840
		10 *(2)*	1.0	840
	-7	18	1.0	840

Notes to Table 8:

(1) The -6 speed grade specifications apply for both commercial and industrial devices.

(2) EP1M350 devices can support any 8 channels at 1.25 Gbps. The other 10 channels must run at 1.0 Gbps or less.

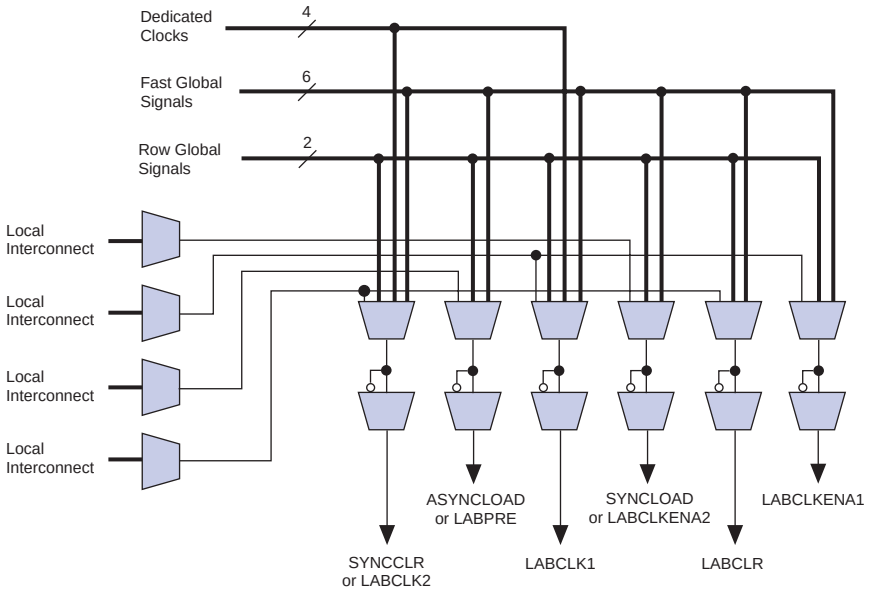
Logic & Interconnect

Mercury device logic is implemented in LEs. LE resources are used differently according to specific operating modes and the type of logic function being implemented. LEs are grouped into LABs in a row-based architecture. The multi-level FastTrack Interconnect structure provides the routing connection between LEs, ESBs, and IOEs.

Logic Array Block

Each LAB consists of 10 LEs, LE carry chains, multiplier circuitry, LAB control signals, local interconnect, and FastLUT connection lines. The local interconnect transfers signals between LEs within the same or adjacent LABs. FastLUT connections transfer the output of one LE to the adjacent LE for ultra-fast sequential LE connections within the same LAB. The Quartus II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of fast local and FastLUT connections for high performance. Figure 5 shows the Mercury LAB structure.

Figure 6. LAB-Wide Control Signals



Logic Element

The LE, the smallest unit of logic in the Mercury architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select look ahead capability. Each LE drives all interconnect types: local interconnect, row and priority row interconnect, column and priority column interconnect, leap lines, and RapidLAB interconnect. Each LE also has the ability to drive its combinatorial output directly to the next LE in the LAB using FastLUT connections. See Figure 7.

Each LE has two outputs that drive the local, row, and column routing resources. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output, while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

LE Operating Modes

The Mercury LE can operate in one of the following modes:

- Normal
- Arithmetic
- Multiplier

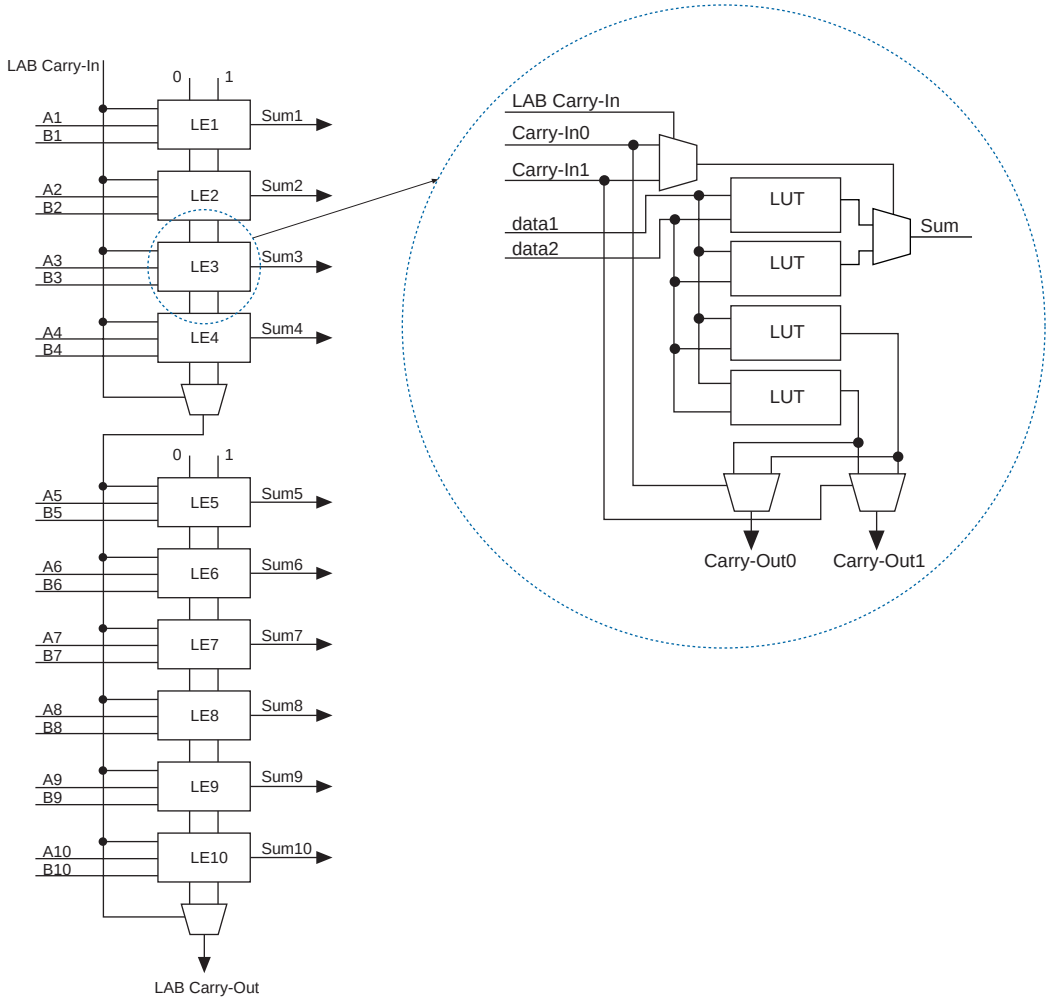
Each operating mode uses LE resources differently. In each operating mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0`, `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain generation; and the FastLUT Connection input from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all normal and arithmetic LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions, such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect and a single carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. The LUT (combinatorial) output can be driven to the FastLUT connection to the next LE in the LAB. LEs in normal mode support packed registers. Figure 8 shows an LE in normal mode.

Figure 10. CSLA Details



The Quartus II Compiler can create CSLA logic automatically during design processing. Alternatively, the designer can create CSLA logic manually during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips intermediate LABs in a row structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in a LAB row carries to the first LE of the third LAB in the same LAB row.

Multiplier Mode

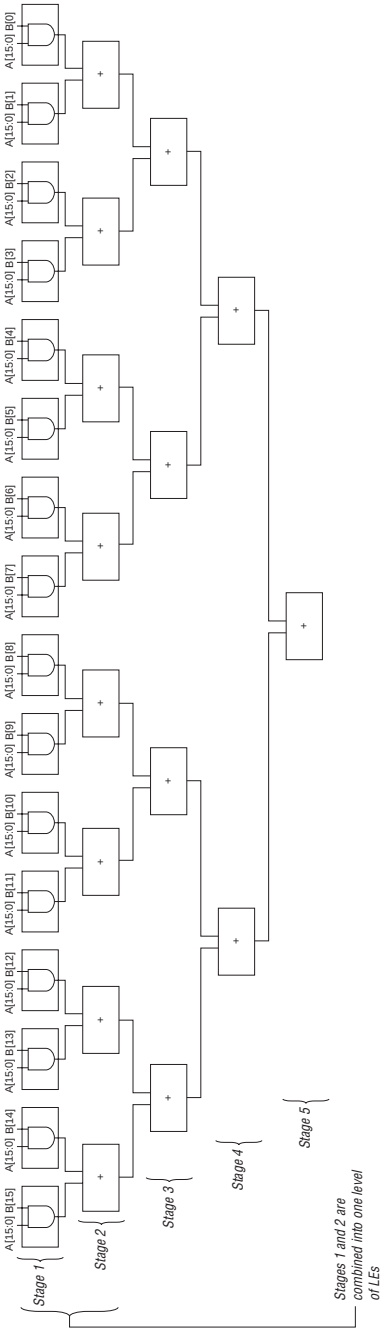
Multiplier mode is used for implementing high-speed multipliers up to 16×16 in size. The LUT implements the partial product formation and summation in a single stage for a $N \times M$-bit multiply operation. A single LE can implement the summation of $A_N B_{M+1} + A_{N+1} B_M$ for the multiplier and multiplicand inputs. To increase the speed of the multiplication, LAB wide signals are used to control the partial product sum generation. These multiplier LAB-wide signals use the LABCLKENA1 and PRESET/ASYNCLOAD resources. The multiplier mode takes advantage of the CSLA circuitry for optimized sum and carry generation in the partial product sum. There is a special CSLA circuitry mode used for the multiplier where the carry chain runs vertically between LABs in the same column. The Quartus II Compiler automatically uses this special mode for dedicated multiplier implementation only. The summation of the multiplier and multiplicand bits is driven out along with the carry-out0 and carry-out1 bits. The combinatorial or registered versions of the sum can be driven out, allowing the multiplier to be pipelined.

The RapidLAB interconnect has dedicated fast connections to the LE inputs in multiplier mode, further increasing the speed of the multiplier. These dedicated connections allow RapidLAB lines to avoid delay incurred by driving onto local interconnects and then into the LE.

The Quartus II software implements parameterized functions that use the multiplier mode automatically when multiply operators are used.

Figure 11 shows a Mercury device LE in multiplier mode.

Figure 13. Mercury Binary Tree Implementation



Clear & Preset Logic Control

LAB-wide signals control logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The direct asynchronous preset does not require a NOT-gate push-back technique. Mercury devices support simultaneous preset, or asynchronous load, and clear. Asynchronous clear takes precedence if both signals are asserted simultaneously. Each LAB supports one clear and one preset signal. Two clears are possible in a single LAB by using a NOT-gate push-back technique on the preset port. The Quartus II Compiler automatically performs this second clear emulation.

In addition to the clear and preset ports, Mercury devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals.

Multi-Level FastTrack Interconnect

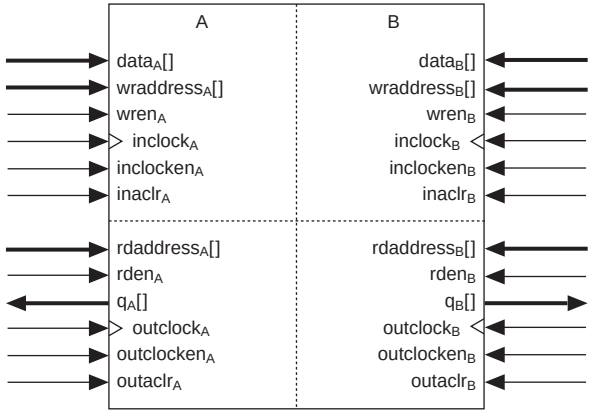
The Mercury architecture provides connections between LEs, ESBs, and device I/O pins via an innovative Multi-Level FastTrack Interconnect structure. The Multi-Level FastTrack Interconnect structure is a series of routing channels that traverse the device, providing a hierarchy of interconnect lines. Regular resources provide efficient and capable connections while priority resources and specialized RapidLAB, leap line, and FastLUT resources enhance performance by accelerating timing on critical paths. The Quartus II Compiler automatically places critical design paths on those faster lines to improve design performance.

This network of routing structures provides predictable performance, even for complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The Multi-Level FastTrack Interconnect consists of regular and priority lines that traverse column and row interconnect channels to span sections and the entire device length. Each row of LABs, ESBs, and I/O bands is served by a dedicated row interconnect, which routes signals to and from LABs, ESBs, and I/O row bands in the same row. These row resources include:

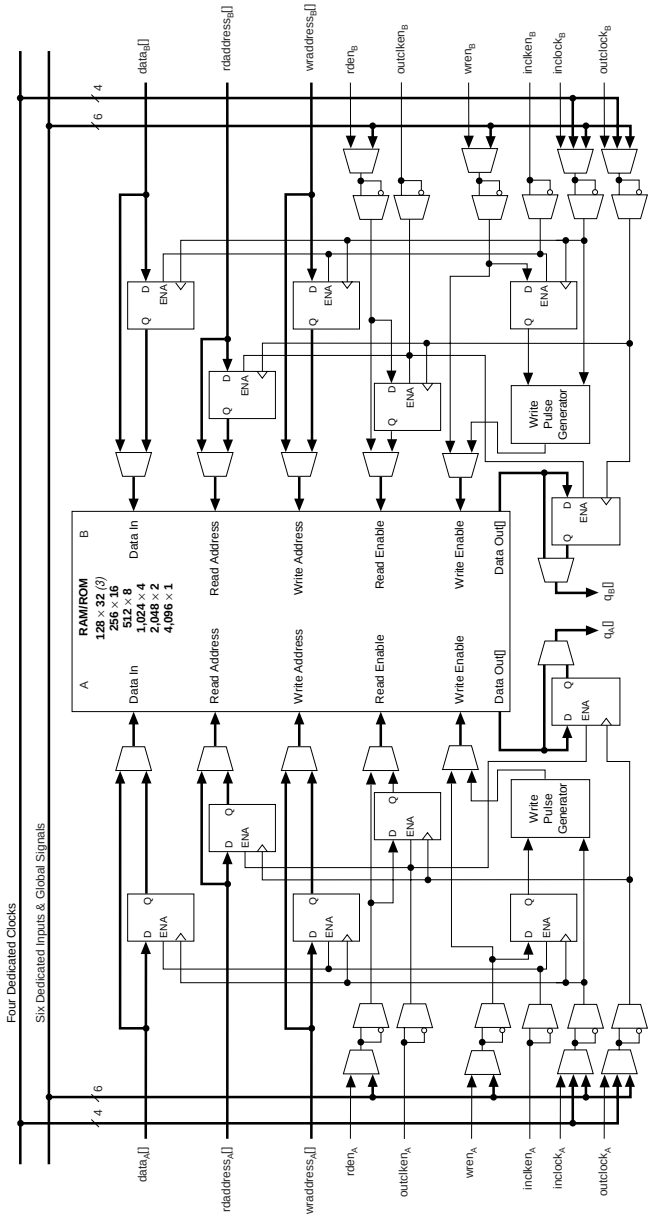
- Row interconnect traversing the entire device from left to right
- Priority row interconnect for high speed access across the length of the device
- RapidLAB interconnect for horizontal routing that traverses a 10-LAB-wide region from a central LAB

Figure 17. ESB Quad-Port Block Diagram



In addition to quad port memory, the ESB also supports true dual-port, dual-port, and single-port RAM. True dual-port RAM supports any combination of two port operations: two reads, two writes, or one read and one write. Dual-port memory supports a simultaneous read and write. For single-port memory, independent read and write is supported. Figure 18 shows these different RAM memory port configurations for an ESB.

Figure 19. ESB in Read/Write Clock Mode *Notes (1), (2)*



Notes to Figure 19:

(1) Only half of the ESB, either A or B, is used for dual-port configuration.
(2) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(3) This configuration is supported for dual-port configuration.

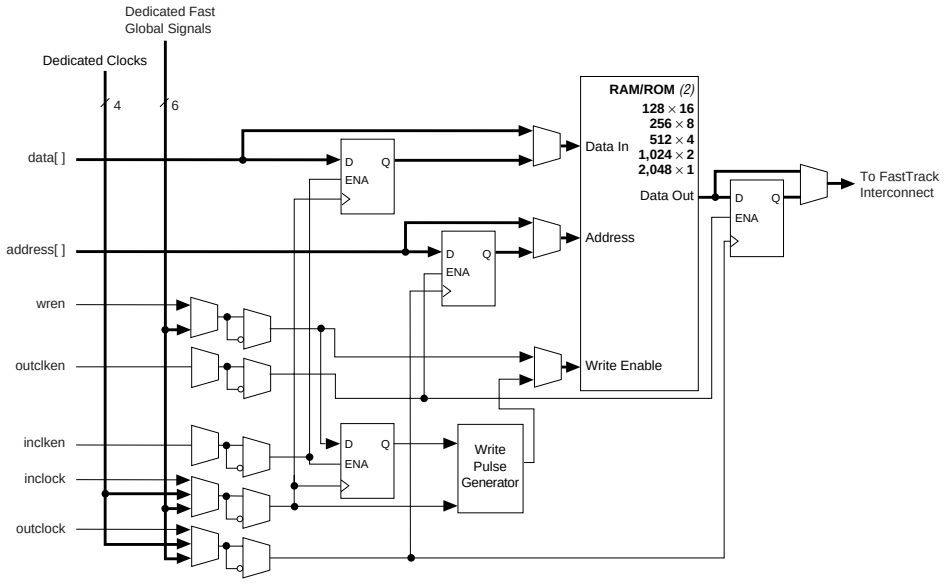
Input/Output Clock Mode

An ESB using input/output clock mode can also use up to four clocks. On each of the two ports, A or B, one clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. Each ESB port, A or B, also supports independent read clock enable, write clock enable, and asynchronous clear signals. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 20 shows the ESB in input/output clock mode.

Single-Port Mode

The Mercury device's ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 21. A single ESB can support up to two single-port mode RAMs.

Figure 21. ESB in Single-Port Mode *Note (1)*



Notes to Figure 21:

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or chip-wide reset.

(2) If there is only one single-port RAM block in an ESB, it can support the following configurations: 4,096 × 1; 2,048 × 2; 1,028 × 4; 512 × 8; 256 × 16; or 128 × 32.

Content-Addressable Memory

Mercury devices can implement CAM in ESBs. CAM can be thought of as the inverse of RAM. RAM stores data in a specific location; when the system submits an address, the RAM block provides the data. Conversely, when the system submits data to CAM, the CAM block provides the address where the data is found. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

Table 12 describes the I/O standards supported by Mercury devices.

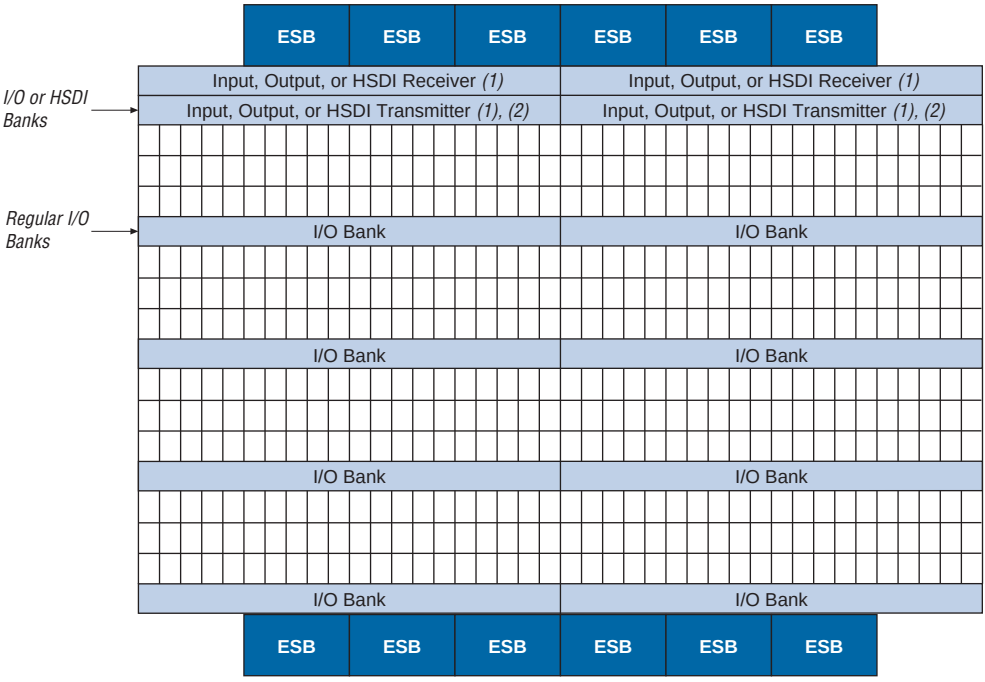
Table 12. Mercury Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
3.3-V PCML	Differential	N/A	3.3	3.3
GTL+	Voltage referenced	1.0	N/A	1.5
HSTL class I and II	Voltage referenced	0.75	1.5	0.75
SSTL-2 class I and II	Voltage referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage referenced	1.5	3.3	1.5
AGP	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

Each regular I/O band row contains two I/O banks. The number of I/O banks in a Mercury device depends on the number of I/O band rows. The top I/O band contains four regular I/O banks specifically designed for HSDI. The top I/O band banks and dedicated clock inputs support LVDS, LVPECL, and 3.3-V PCML. 3.3-V PCML is an open-drain standard and therefore requires external termination to 3.3 V. All other standards are supported by all I/O banks. The top I/O banks 1, 2, 3, and 4 only support non-HSDI I/O pins if the design does not use HSDI circuitry. If the design uses any HSDI channel, banks 1, 2, 3, and 4 all do not support regular I/O pins.

Additionally, the EP1M350 device includes the Flexible-LVDS feature, providing support for up to 100 LVDS channels on all regular I/O banks. Regular I/O banks in EP1M350 devices include dedicated LVDS input and output buffers that do not require any external components except for 100-Ω termination resistors on receiver channels.

Figure 30. I/O Bank Layout



Notes to Figure 30:

(1) If HSDI I/O channels are not used, the HSDI banks can be used as regular I/O banks.

(2) When used as regular I/O banks, these banks must be set to the same V_{CCIO} level, but can have separate V_{REF} bank settings.

For more information on I/O standards, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

MultiVolt I/O Interface

The Mercury architecture supports the MultiVolt I/O interface feature, which allows Mercury devices in all packages to interface with devices with different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

Lock Signals

The Mercury device general purpose PLL circuits support individual LOCK signals. The LOCK signal drives high when the PLL has locked onto the input clock. Lock remains high as long as the input remains within specification. It will go low if the input is out of specification. A LOCK pin is optional for each PLL used in the Mercury devices; when not used, they are I/O pins. This signal is not available internally; if it is used in the core, it must be fed back in with an input pin.

SignalTap Embedded Logic Analyzer

Mercury devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the Mercury device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 JTAG circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All Mercury devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. Mercury devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Standard Test and Programming Language (STAPL) Files (**.jam**) or Jam STAPL Byte-Code Files (**.jbc**). Mercury devices also use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. Mercury devices support the JTAG instructions shown in Table 16.

Table 16. Mercury JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a Mercury device via the JTAG port with a ByteBlasterMV™ download cable, or using a Jam STAPL or Jam Byte-Code file via an embedded processor.
SignalTap Instructions	These instructions monitor internal device operation with the SignalTap embedded logic analyzer.

The Mercury device instruction register length is 10 bits. The Mercury device USERCODE register length is 32 bits. Tables 17 and 18 show the boundary-scan register length and device IDCODE information for Mercury devices.

Table 17. Mercury Boundary-Scan Register Length

Device	Boundary-Scan Register Length (Bits)
EP1M120	1,125
EP1M350	1,695

Table 18. 32-Bit Mercury Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP1M120	0000	0011 0000 0000 0000	000 0110 1110	1
EP1M350	0000	0011 0000 0000 0001	000 0110 1110	1

Notes to Table 18:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 32 shows the timing requirements for the JTAG signals.

Figure 32. Mercury JTAG Waveforms

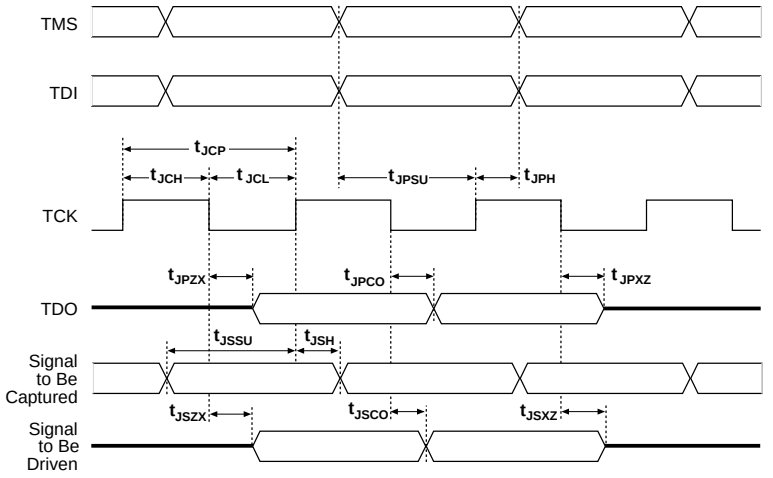


Table 19 shows the JTAG timing parameters and values for Mercury devices.

Table 19. Mercury JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Table 21. Mercury Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*	1.71	1.89	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(3)*	1.4	1.6	V
V_I	Input voltage	*(2)*, *(5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 22. Mercury Device DC Operating Conditions *Note (6)*, *(7)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(5)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(5)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) for EP1M120 devices	For commercial use *(8)*		30		mA
		For Industrial use *(8)*		40		mA
	V_{CC} supply current (standby) for EP1M350 devices	For commercial use *(8)*		50		mA
		For Industrial use *(8)*		60		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Figure 35. Transmitter Output Waveforms for Differential I/O Standards

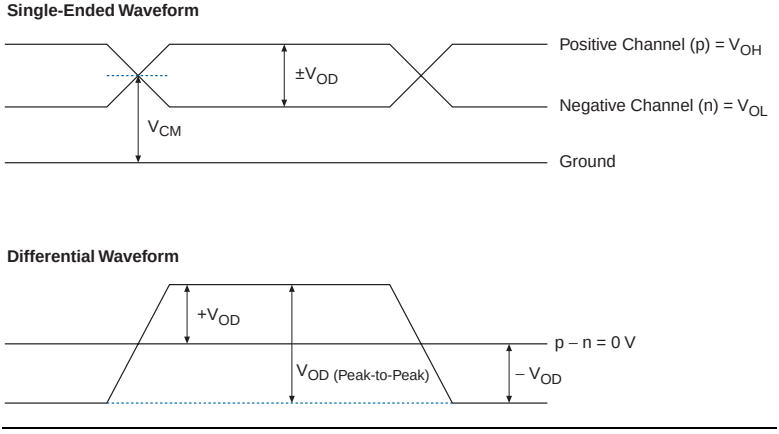


Table 27. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250	510	600	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to Mercury devices)		90	100	110	Ω