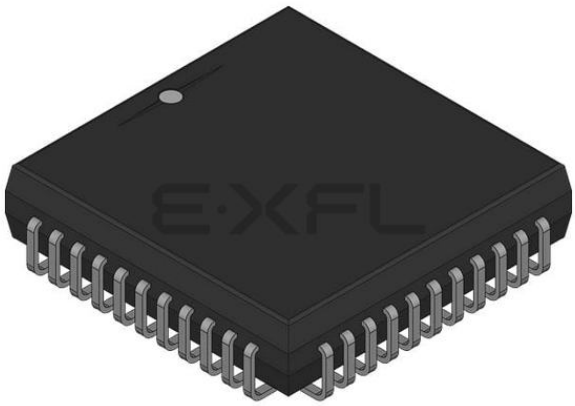

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Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	4.25K x 8
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Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Supplier Device Package	44-PLCC (16.6x16.6)
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automatically tristated when inputting data regardless of the Port 0 configuration. The Port 0 configuration will determine the idle state of Port 0 when not accessing the external memory.

Figure 3-9 and Figure 3-10 show examples of external data memory write and read cycles, respectively. The address on P0 and P2 is stable at the falling edge of ALE. The idle polarity of ALE is controlled by ALES (AUXR.0). When ALES = 0 the idle polarity of ALE is high (active). When ALES = 1 the idle polarity of ALE is low (inactive). The ALE strobe pulse is always active high. Unlike standard 8051s, ALE will not toggle continuously when not accessing external memory. ALES must be zero in order to use P4.4 as a general-purpose I/O. The WS bits in AUXR can extended the $\overline{RD}$ and $\overline{WR}$ strobes by 1, 2 or 3 cycles as shown in Figures 3-11, 3-12 and 3-13. If a longer strobe is required, the application can scale the system clock with the clock divider to meet the requirements (See Section 6.5 on page 32).

Figure 3-9. External Data Memory Write Cycle (WS = 00B)

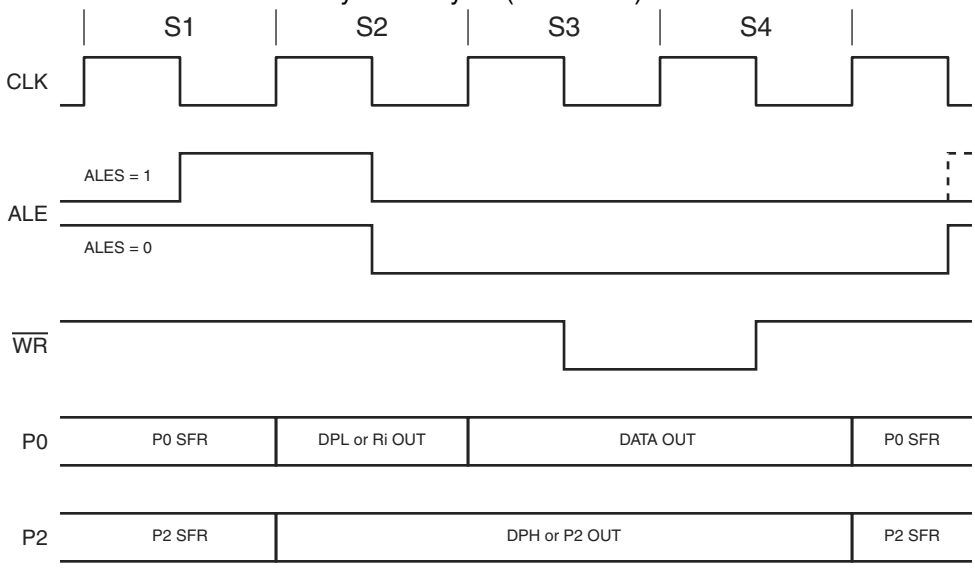


Figure 3-10. External Data Memory Read Cycle (WS = 00B)

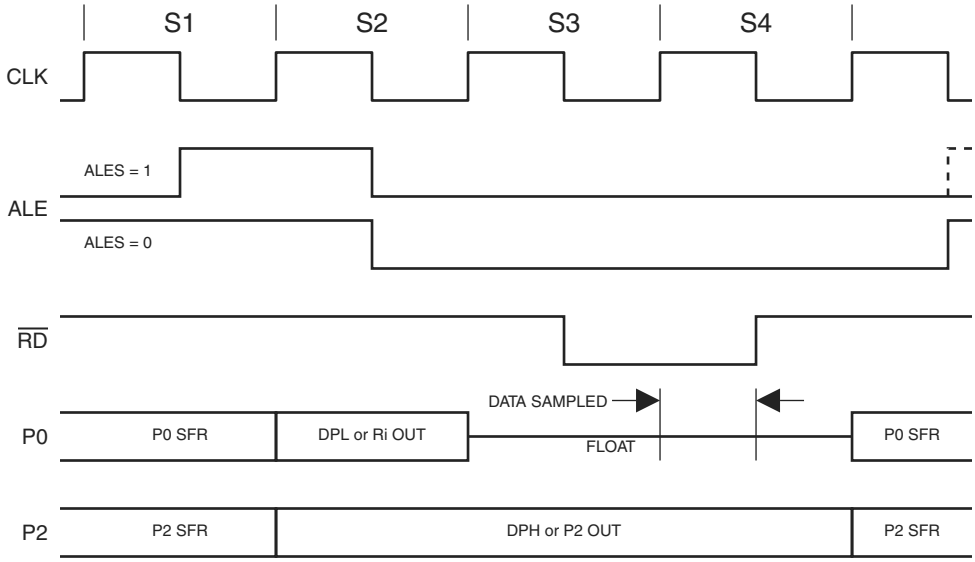


Table 8-1. PCON – Power Control Register

PCON = 87H — Reset Value = 000X 0000B

Not Bit Addressable

	SMOD1	SMOD0	PWDEX	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in Modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 1, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
PWDEX	Power-down Exit Mode. When PWDEX = 1, wake up from Power-down is externally controlled. When PWDEX = 1, wake up from Power-down is internally timed.
POF	Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power-down bit. Setting this bit activates power-down operation. The PD bit is cleared automatically by hardware when waking up from power-down.
IDL	Idle Mode bit. Setting this bit activates Idle mode operation. The IDL bit is cleared automatically by hardware when waking up from idle

8.2 Power-down Mode

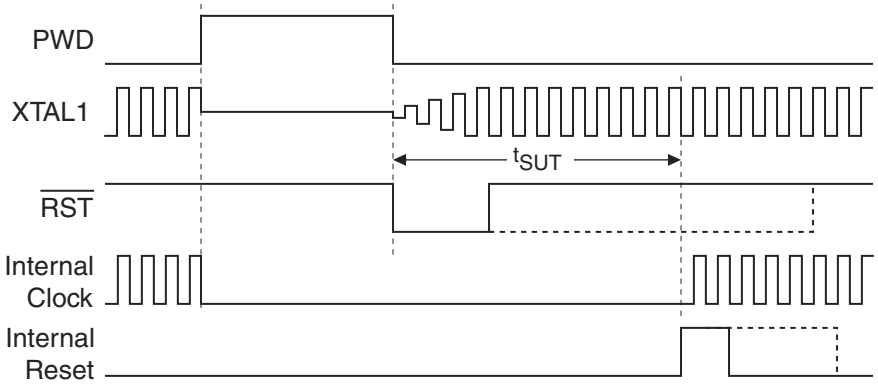
Setting the Power-down (PD) bit in PCON enters Power-down mode. Power-down mode stops the oscillator, disables the BOD and powers down the Flash memory in order to minimize power consumption. Only the power-on circuitry will continue to draw power during Power-down. During Power-down, the power supply voltage may be reduced to the RAM keep-alive voltage. The RAM contents will be retained, but the SFR contents are not guaranteed once V_{DD} has been reduced. Power-down may be exited by external reset, power-on reset, or certain enabled interrupts.

8.2.1 Interrupt Recovery from Power-down

Three external interrupt sources may be configured to terminate Power-down mode: external interrupts $\overline{INT0}$ (P3.2) and $\overline{INT1}$ (P3.3); and the general-purpose interrupts (GPI). To wake up by external interrupt $\overline{INT0}$ or $\overline{INT1}$, that interrupt must be enabled by setting EX0 or EX1 in IE and must be configured for level-sensitive operation by clearing IT0 or IT1. Any General-purpose interrupt on Port 1 (GPI_{7-0}) can also wake up the device. The GPI pin must be enabled in GPIEN and configured for level-sensitive detection, and EGP in IE2 must be set in order to terminate Power-down.

When terminating Power-down by an interrupt, two different wake-up modes are available. When PWDEX in PCON is zero, the wake-up period is internally timed as shown in Figure 8-1. At the falling edge on the interrupt pin, Power-down is exited, the oscillator is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate to the CPU until after the timer has timed out. After the time-out period the interrupt service routine will begin. The time-out period is controlled by the Start-up Timer Fuses (see Table 7-1 on page 35). The interrupt pin need not remain low for the entire time-out period.

Figure 8-3. Reset Recovery from Power-down



8.3.2 Analog Comparators

The comparators will operate during Idle mode if enabled. To save power, the comparators should be disabled before entering Idle mode if possible. When the comparators are turned off and on again, some settling time is required for the analog circuits to stabilize. If the comparators are enabled, they will consume the least power when using an external reference, RFA_{1-0} = 00B and RFB_{1-0} = 00B.

8.3.3 Analog-to-Digital Converter

The DADC will operate during Idle mode if enabled. To save power, the DADC should be disabled before entering Idle mode if possible. When the DADC is turned off and on again, some settling time is required for the analog circuits to stabilize. If the DADC is enabled, it will consume the least power when configured to use the system clock instead of the internal RC oscillator (unless the IRC is the system clock source) and when the internal reference is disabled (IREF = 0). The DADC must always be disabled before entering power-down.

9. Interrupts

The AT89LP3240/6440 provides 12 interrupt sources: two external interrupts, three timer interrupts, a serial port interrupt, an analog comparator interrupt, a general-purpose interrupt, a compare/capture interrupt, a two-wire interrupt, an ADC interrupt and an SPI interrupt. These interrupts and the system reset each have a separate program vector at the start of the program memory space. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IE and IE2. The IE register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP, IPH, IP2 and IP2H. IP and IP2 hold the low order priority bits and IPH and IP2H hold the high priority bits for each interrupt. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the end of an instruction, the request of higher priority level is serviced. If requests of the same priority level are pending at the end of an instruction, an internal polling sequence determines which request is serviced. The polling sequence is based on the vector address; an interrupt with a lower vector address has higher priority than an interrupt with a higher vector address. Note that the polling sequence is only used to resolve pending requests of the same priority level.

The IP*x*D bits located at the seventh bit of IP, IPH, IP2 and IP2H can be used to disable all interrupts of a given priority level, allowing software implementations of more complex interrupt priority handling schemes such as level-based round-robin scheduling.

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can each be either level-activated or edge-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to, hardware clears the flag that generated an external interrupt only if the interrupt was edge-activated. If the interrupt was level activated, then the external requesting source (rather than the on-chip hardware) controls the request flag.

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers (except for Timer 0 in Mode 3). When a timer interrupt is generated, the on-chip hardware clears the flag that generated it when the service routine is vectored to. The Timer 2 Interrupt is generated by a logic OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the CPU vectors to the service routine. The service routine normally must determine whether TF2 or EXF2 generated the interrupt and that bit must be cleared by software.

The Serial Port Interrupt is generated by the logic OR of RI and TI in SCON. Neither of these flags is cleared by hardware when the CPU vectors to the service routine. The service routine normally must determine whether RI or TI generated the interrupt and that bit must be cleared by software.

The Serial Peripheral Interface Interrupt is generated by the logic OR of SPIF, MODF and TXE in SPSR. None of these flags is cleared by hardware when the CPU vectors to the service routine. The service routine normally must determine which bit generated the interrupt and that bit must be cleared by software.

A logic OR of all eight flags in the GPIF register causes the General-purpose Interrupt. None of these flags is cleared by hardware when the service routine is vectored to. The service routine must determine which bit generated the interrupt and that bit must be cleared in software. If the interrupt was level activated, then the external requesting source must de-assert the interrupt before the flag may be cleared by software.

The CFA and CFB bits in ACSRA and ACSRB respectively generate the Comparator Interrupt. The service routine must normally determine whether CFA or CFB generated the interrupt, and the bit must be cleared by software. The DAC/ADC Conversion Interrupt is generated by ADIF in DADC. On-chip hardware clears the ADIF flag when vectoring to the service routine.

A logic OR of the four least significant bits in the T2CCF register causes the Compare/Capture Array Interrupt. None of these flags is cleared by hardware when the service routine is vectored to. The service routine must determine which bit generated the interrupt and that bit must be cleared in software.

The Two-Wire Interface Interrupt is generated by TWIF in TWCR. The flag is not cleared by hardware when the CPU vectors to the service routine. The service routine normally must determine the status in TWSR and respond accordingly before the bit is cleared by software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though they had been set or cleared by hardware. That is, interrupts can be generated and pending interrupts can be canceled in software.

Symbol	Function
PSP	Serial Peripheral Interface Interrupt Priority Low
PCC	Compare/Capture Array Interrupt Priority Low
PGP	General-purpose Interrupt 0 Priority Low

Table 9-6. IPH – Interrupt Priority High Register

IPH = B7H — Reset Value = 0000 0000B

Not Bit Addressable

	IP1D	PCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP1D	Interrupt Priority 1 Disable. Set IP1D to 1 to disable all interrupts with priority level one. Clear to 0 to enable all interrupts with priority level one when EA = 1.
PCH	Comparator Interrupt Priority High
PT2H	Timer 2 Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

Table 9-7. IP2H – Interrupt Priority 2 High Register

IPH = B6H — Reset Value = 0xxx x000B

Not Bit Addressable

	IP3D	–	–	PTWH	PADH	PSPH	PCCH	PGPH
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP3D	Interrupt Priority 3 Disable. Set IP3D to 1 to disable all interrupts with priority level three. Clear to 0 to enable all interrupts with priority level three when EA = 1.
PTWH	Two-Wire Interface Interrupt Priority High
PADH	ADC Interrupt Priority High
PSPH	Serial Peripheral Interface Interrupt Priority High
PCCH	Compare/Capture Array Interrupt Priority High
PGPH	General-purpose Interrupt 0 Priority High

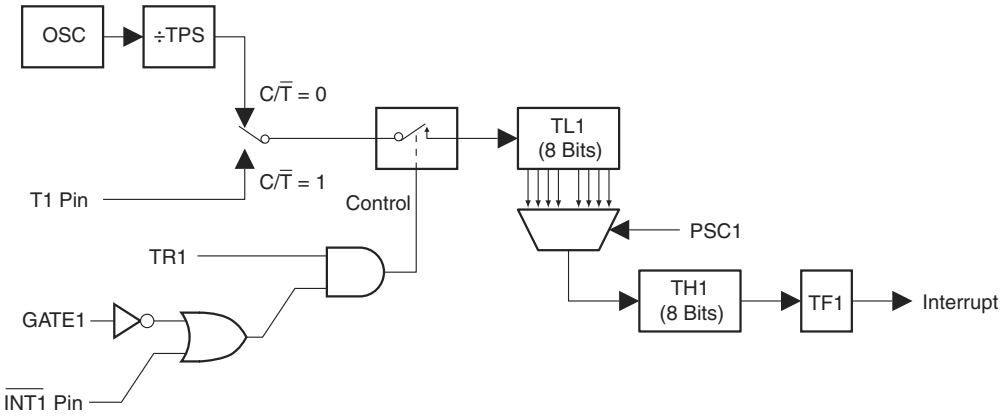
11.1 Mode 0 – Variable Width Timer/Counter

Both Timers in Mode 0 are 8-bit Counters with a variable prescaler. The prescaler may vary from 1 to 8 bits depending on the PSC bits in TCONB, giving the timer a range of 9 to 16 bits. By default the timer is configured as a 13-bit timer compatible to Mode 0 in the standard 8051. Figure 11-1 shows the Mode 0 operation as it applies to Timer 1 in 13-bit mode. As the count rolls over from all “1”s to all “0”s, it sets the Timer interrupt flag TF1. The counter input is enabled to the Timer when TR1 = 1 and either GATE1 = 0 or $\overline{INT1}$ = 1. Setting GATE1 = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements. TR1 is a control bit in the Special Function Register TCON. GATE1 is in TMOD. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.

$$\text{Mode 0:} \qquad \text{Time-out Period} = \frac{256 \times 2^{PSC0+1}}{\text{Oscillator Frequency}} \times (TPS + 1)$$

Note: RH1/RL1 are not required by Timer 1 during Mode 0 and may be used as temporary storage registers.

Figure 11-1. Timer/Counter 1 Mode 0: Variable Width Counter



Mode 0 operation is the same for Timer 0 as for Timer 1, except that TR0, TF0, GATE0 and $\overline{INT0}$ replace the corresponding Timer 1 signals in Figure 11-1. There are two different C/T bits, one for Timer 1 (TMOD.6) and one for Timer 0 (TMOD.2).

11.2 Mode 1 – 16-bit Auto-Reload Timer/Counter

In Mode 1 the Timers are configured for 16-bit auto-reload. The Timer register is run with all 16 bits. The 16-bit reload value is stored in the high and low reload registers (RH1/RL1). The clock is applied to the combined high and low timer registers (TH1/TL1). As clock pulses are received, the timer counts up: 0000H, 0001H, 0002H, etc. An overflow occurs on the FFFFH-to-0000H transition, upon which the timer register is reloaded with the value from RH1/RL1 and the overflow flag bit in TCON is set. See Figure 11-2. The reload registers default to 0000H, which gives the full 16-bit timer period compatible with the standard 8051. Mode 1 operation is the same for Timer/Counter 0.

$$\text{Mode 1:} \qquad \text{Time-out Period} = \frac{(65536 - \{RH0, RL0\})}{\text{Oscillator Frequency}} \times (TPS + 1)$$

to occur at a negative edge, positive edge, or both (toggle). Capture inputs are sampled every clock cycle and a new value must be held for at least 2 clock cycles to be correctly sampled by the device. The maximum achievable capture rate will be determined by how fast the software can retrieve the captured data. There is no protection against capture events overrunning the data register.

Capture events may also be triggered internally by the overflows of Timer 0 or Timer 1, or by an event from the dual analog comparators. Any comparator event which can generate a comparator interrupt may also be used as a capture event. However, Timer 2 should not be selected as the comparator clock source when using the comparator as the capture trigger.

When the DAC output is enabled on P2.2 and P2.3, channels C and D cannot use their external pin capture modes. However, those channels may still use the timer or comparator triggers to capture data. The same applies for all four channels when Port 2 is used for the external memory interface.

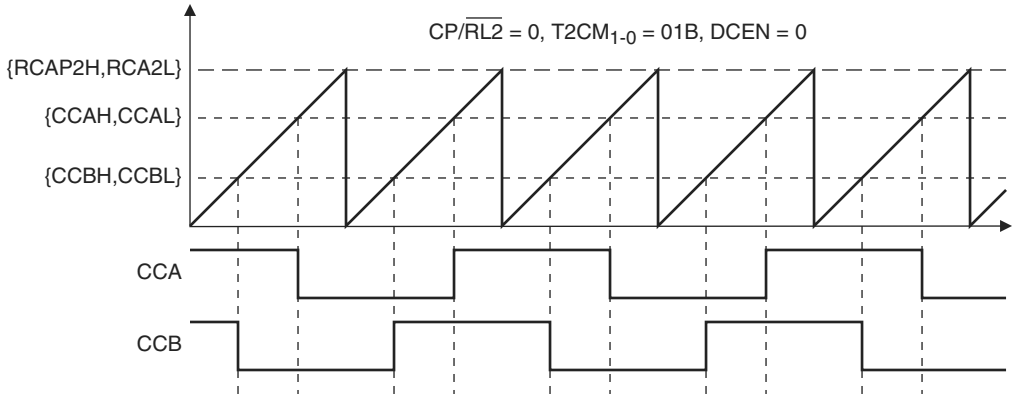
13.2.1 Timer 2 Operation for Capture Mode

Capture channels are intended to work with Timer 2 in capture mode CP/$\overline{RL2}$ = 1. Captures can still occur when Timer 2 operates in other modes; however, the full 16-bit count range may not be available. The TF2 flag can be used to determine if the timer overflowed before the capture occurred. If the timer is operating in dual-slope mode (CP/$\overline{RL2}$ = 0, $T2CM_{1\text{-}0}$ = 1xB), the count direction (Up = 0 and Down = 1) at the time of the event will be captured into the channel's CDIR*x* bit in CCC*x*. CTC*x* must be cleared to 0 for all channels if Timer 2 is operating in Baud Rate mode or errors may occur in the serial communication.

13.3.1.1 Normal Mode

The simplest waveform mode is when CP/$\overline{RL2}$ = 0 and T2CM$\overline{1\text{-}0}$ = 01B. In this mode the frequency of the output is determined by the TOP value stored in RCAP2L and RCAP2H and output edges occur at fractions of the timer period. Figure 13-4 shows an example of outputting two waveforms of the same frequency but different phase by using the toggle on match action. More complex waveforms are achieved by changing the TOP value and the compare values more frequently.

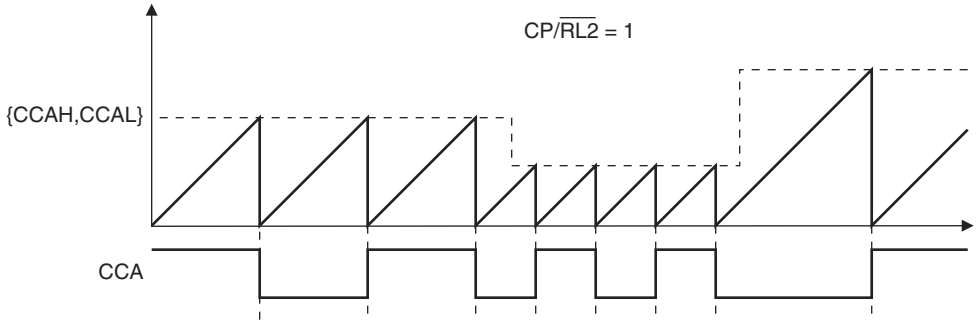
Figure 13-4. Normal Mode Waveform Example



13.3.1.2 Clear-Timer-on-Compare Mode

Clear-Timer-on-Compare (CTC) mode occurs when the CTC*x* bit of a compare channel is set to one. CTC Mode works best when Timer 2 is in capture mode (CP/$\overline{RL2}$ = 1) to allow the full range of compare values. In CTC Mode the compare value defines the interval between output events because the timer is cleared after every compare match. Figure 13-5 shows an example waveform using the toggle on match action in CTC Mode.

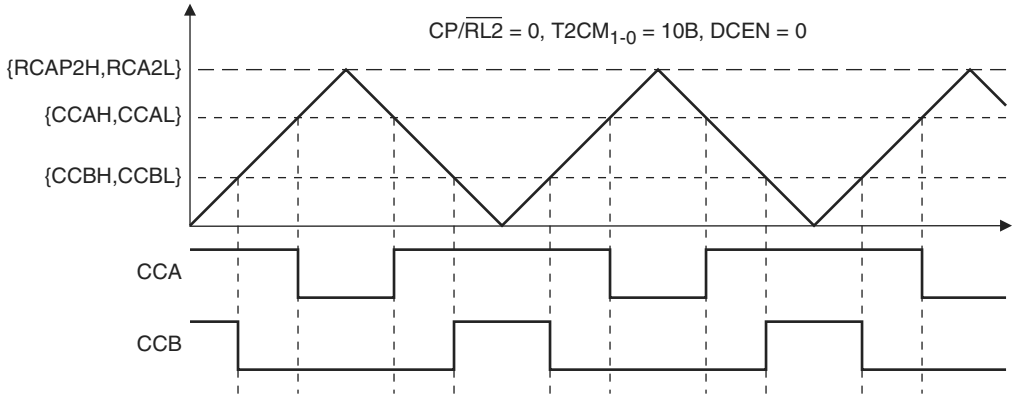
Figure 13-5. CTC Mode Waveform Example



13.3.1.3 Dual-Slope Mode

The dual-slope mode occurs when CP/$\overline{RL2}$ = 0 and T2CM$_{1\text{-}0}$ = 1xB. In this mode the frequency of the output is determined by the TOP value stored in RCAP2L and RCAP2H and output edges occur at fractions of the timer period on both the up and down count. Figure 13-6 shows an example of outputting two symmetrical waveforms using the toggle on match action. More complex waveforms are achieved by changing the TOP value and the compare values more frequently.

Figure 13-6. Dual-Slope Waveform Example



13.3.2 Timer 2 Operation for Compare Mode

Compare channels will work with any Timer 2 operating mode. The full 16-bit compare range may not be available in all modes. In order for a compare output action to take place, the compare values must be within the counting range of Timer 2. CTC*x* must be cleared to 0 for all channels if Timer 2 is operating in Baud Rate mode or errors may occur in the serial communication.

13.4 Pulse Width Modulation Mode

In Pulse Width Modulation (PWM) Mode, a compare channel can output a square wave with programmable frequency and duty cycle. Setting CCMx = 1 and CxM_{2-0} = 10xB enables PWM Mode. PWM Mode is similar to Output Compare Mode except that the compare value is double-buffered. A diagram of a CCA channel in PWM Mode is shown in Figure 13-7. The PWM polarity is selectable between inverting and non-inverting modes. PWM is intended for use with Timer 2 in Auto-Reload Mode (CP/$\overline{RL2}$ = 0, DCEN = 0) using count modes 1, 2 or 3. The PWM can operate in asymmetric (edge-aligned) or symmetric (center-aligned) mode depending on the T2CM selection. The CCA PWM has variable precision from 2 to 16 bits. A trade-off between frequency and precision is made by changing the TOP value of the timer. The CCA PWM always uses the greatest precision allowable for the selected output frequency, as compared to Timer 0 and 1 whose PWMs are fixed at 8-bit precision regardless of frequency.

Figure 13-7. CCA PWM Mode Diagram

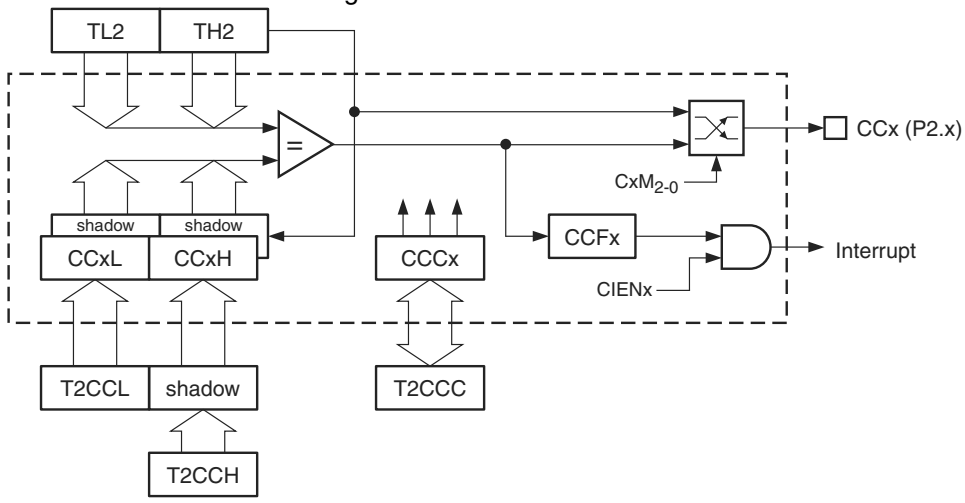


Table 13-6. Summary of Multi-Phasic Modes

PHS_{2-0}	Mode	Behavior	
		PHSD = 0	PHSD = 1
000	Off	Normal Operation (all channels active at all times)	
001	1:2	A →B →A →B	B →A →B →A
010	1:3	A →B →C →A →B →C	C →B →A →C →B →A
011	1:4	A →B →C →D →A →B →C →D	D →C →B →A →D →C →B →A
100	2:4	A →B →A →B C →D →C →D	B →A →B →A D →C →D →C

Figure 13-12. Multi-Phasic PWM Output Stage

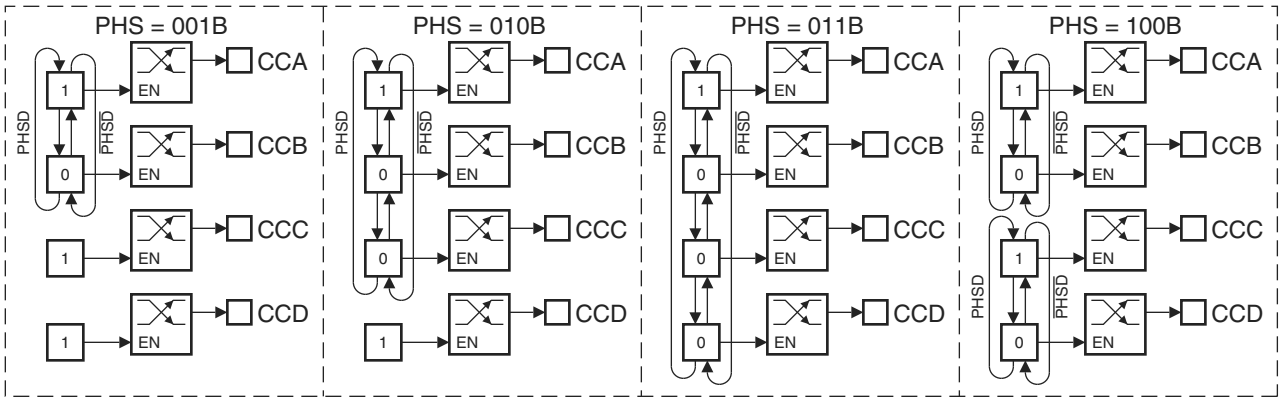
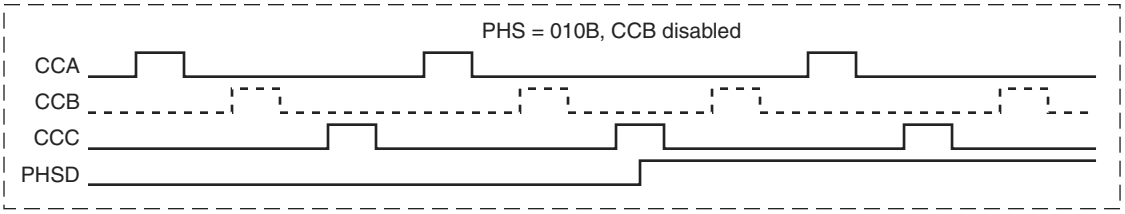


Figure 13-13. Three-Phase Mode with Channel B Disabled



and if the ENH bit in SPSR is set. For multi-byte transfers, TXE may be used to remove any dead time between byte transmissions.

The SPI master can operate in two modes: multi-master mode and single-master mode. By default, multi-master mode is active when SSIG = 0. In this mode, the $\overline{SS}$ input is used to disable a master device when another master is accessing the bus. When $\overline{SS}$ is driven low, the master device becomes a slave by clearing its MSTR bit and a Mode Fault is generated by setting the MODF bit in SPSR. MODF will generate an interrupt if enabled. The MSTR bit must be set in software before the device may become a master again. Single-master mode is enabled by setting SSIG = 1. In this mode $\overline{SS}$ is ignored and the master is always active. $\overline{SS}$ may be used as a general purpose I/O in this mode.

17.2 Slave Operation

When the AT89LP3240/6440 is not configured for master operation, MSTR = 0, it will operate as an SPI slave. In slave mode, bytes are shifted in through MOSI and out through MISO by a master device controlling the serial clock on SCK. When a byte has been transferred, the SPIF flag is set to “1” and an interrupt request is generated, if enabled. The data received from the addressed master device is also transferred from the shift register to the receive buffer. The received data is accessed by reading SPDR. A slave device cannot initiate transfers. Data to be transferred to the master device must be preloaded by writing to SPDR. Writes to SPDR are double-buffered. The transmit buffer is loaded first and if the shift register is empty, the contents of the buffer will be transferred to the shift register.

While the TXE flag is set, the transmit buffer is empty. TXE can be cleared by software or by writing to SPDR. Writing to SPDR will clear TXE and load the transmit buffer. The user may load the buffer while the shift register is busy, i.e. before the current transfer completes. When the current transfer completes, the queued byte in the transmit buffer is moved to the shift register and waits for the master to initiate another transfer. TXE will generate an interrupt if the SPI interrupt is enabled and if the ENH bit in SPSR is set.

The SPI slave can operate in two modes: 4-wire mode and 3-wire mode. By default, 4-wire mode is active when SSIG = 0. In this mode, the $\overline{SS}$ input is used to enable/disable the slave device when addressed by a master. When $\overline{SS}$ is driven low, the slave device is enabled and will shift out data on MISO in response to the serial clock on SCK. While $\overline{SS}$ is high, the SPI slave will remain sleeping with MISO inactive. Three-wire mode is enabled by setting SSIG = 1. In this mode $\overline{SS}$ is ignored and the slave is always active. $\overline{SS}$ may be used as a general purpose I/O in this mode.

The Disable Slave Output bit, DISSO in SPSR, may be used to disable the MISO line of a slave device. DISSO can allow several slave devices to share MISO while operating in 3-wire mode. In this case some protocol other than $\overline{SS}$ may be used to determine which slave is enabled.

17.3 Pin Configuration

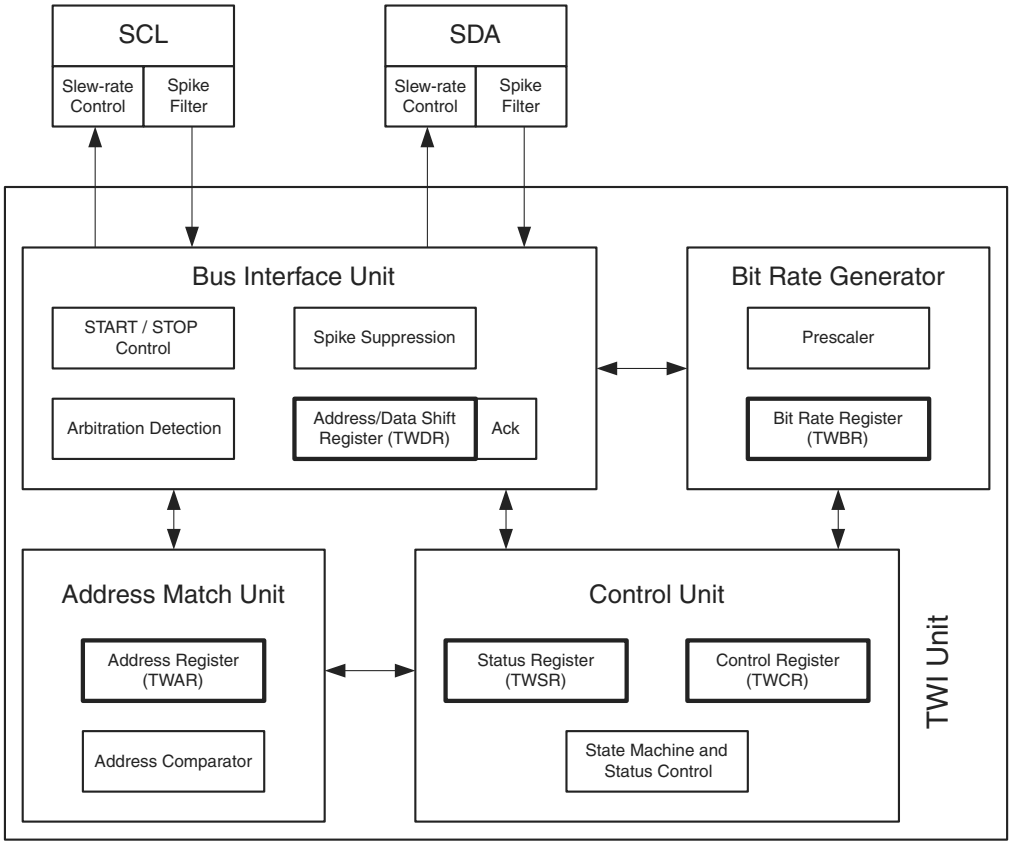
When the SPI is enabled (SPE = 1), the data direction of the MOSI, MISO, SCK, and SS pins is automatically overridden according to the MSTR bit as shown in Table 17-1. The user need not reconfigure the pins when switching from master to slave or vice-versa. For more details on port configuration, refer to “Port Configuration” on page 45.

It is the user software's responsibility to ensure that these illegal arbitration conditions never occur. This implies that in multi-master systems, all data transfers must use the same composition of SLA+R/W and data packets. In other words: All transmissions must contain the same number of data packets, otherwise the result of the arbitration is undefined.

18.3 Overview of the TWI Module

The TWI module is comprised of several submodules, as shown in Figure 18-9. All registers drawn in a thick line are accessible through the AT89LP data bus.

Figure 18-9. Overview of the TWI Module



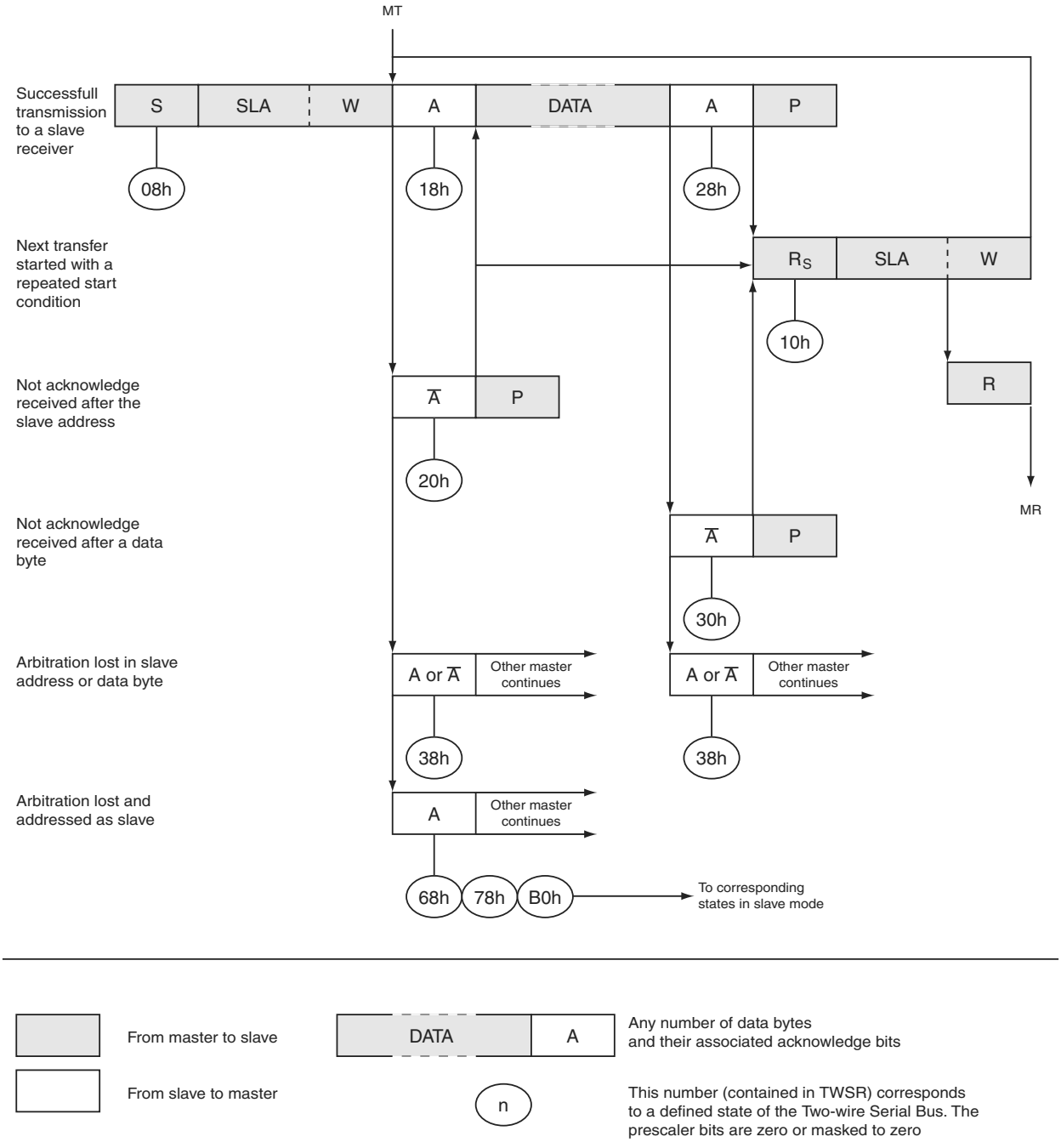
18.3.1 SCL and SDA Pins

These pins interface the AT89LP TWI with the rest of the MCU system. The output drivers contain a slew-rate limiter in order to conform to the TWI specification. The input stages contain a spike suppression unit removing spikes shorter than 50 ns.

18.3.2 Bit Rate Generator Unit

This unit controls the period of SCL when operating in a Master mode. The SCL period is controlled by settings in the TWI Bit Rate Register (TWBR). Slave operation does not depend on the Bit Rate setting, but the CPU clock frequency in the slave must be at least 16 times higher than the SCL frequency. Note that slaves may prolong the SCL low period, thereby reducing the

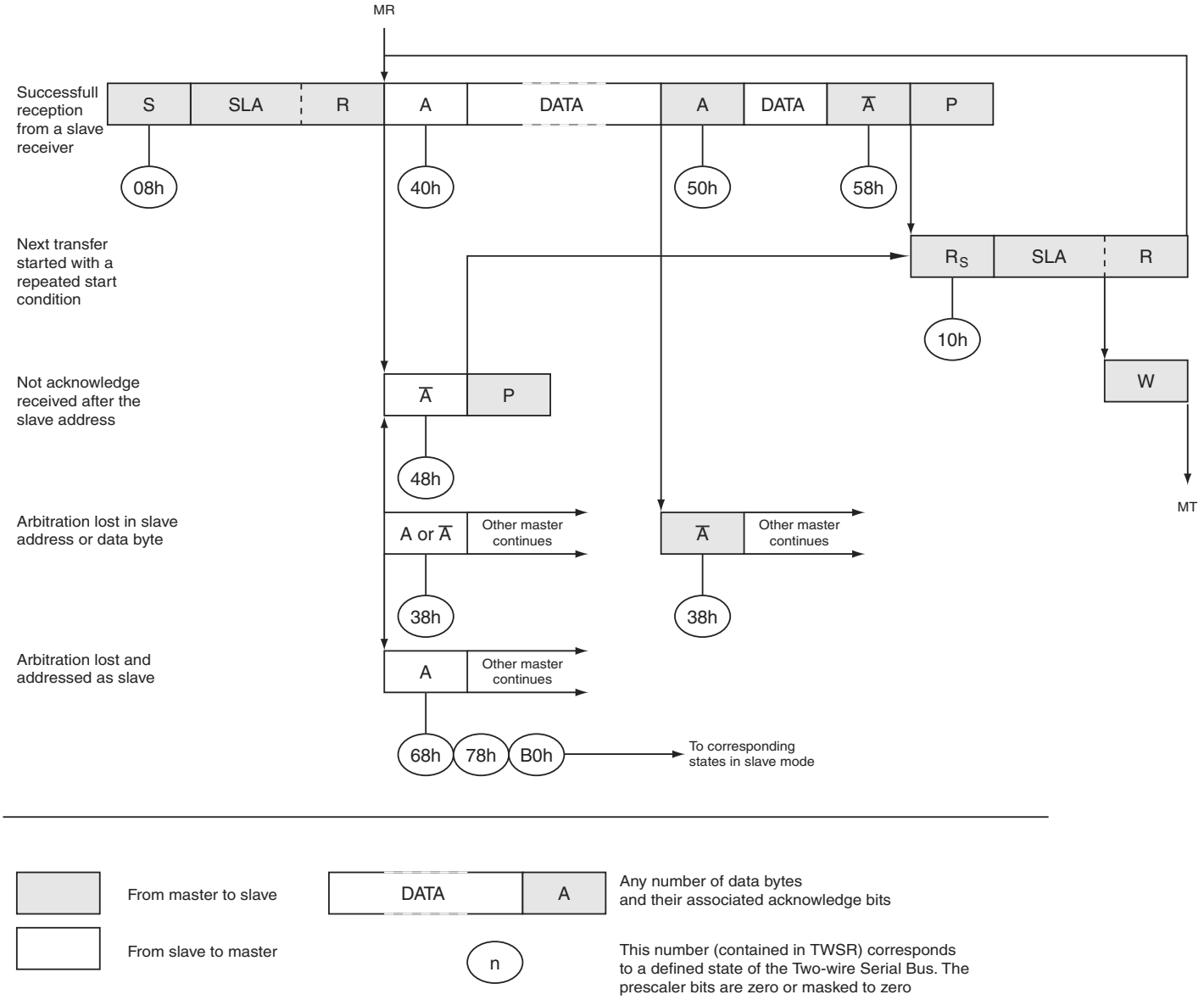
Figure 18-11. Format and States in Master Transmitter Mode



18.6.2 Master Receiver Mode

In the Master Receiver mode, a number of data bytes are received from a slave transmitter. In order to enter a Master mode, a START condition must be transmitted. The format of the following address packet determines whether Master Transmitter or Master Receiver mode is to be entered. If SLA+W is transmitted, MT mode is entered, if SLA+R is transmitted, MR mode is entered.

Figure 18-12. Format and States in Master Receiver Mode



18.6.3 Slave Receiver Mode

In the Slave Receiver mode, a number of data bytes are received from a master transmitter. To initiate the Slave Receiver mode, TWAR and TWCR must be initialized as follows:

TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	GC
Value	Device's own Slave Address							X

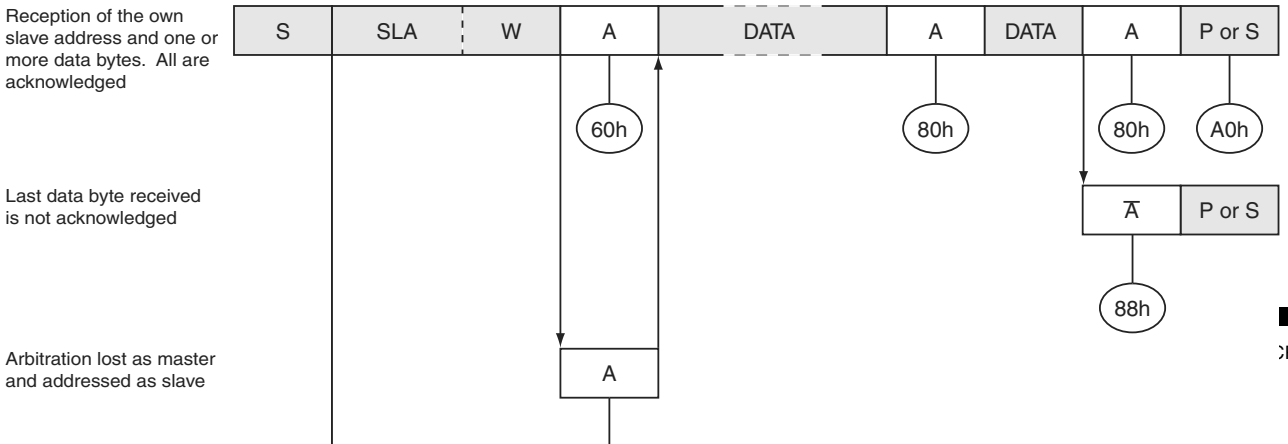
The upper seven bits are the address to which the Two-wire Serial Interface will respond when addressed by a master. If the LSB is set, the TWI will respond to the general call address (00h), otherwise it will ignore the general call address.:

TWCR	–	TWEN	STA	STO	TWIF	AA	–	–
Value	X	1	0	0	0	1	X	X

Table 18-8. Status Codes for Slave Receiver Mode

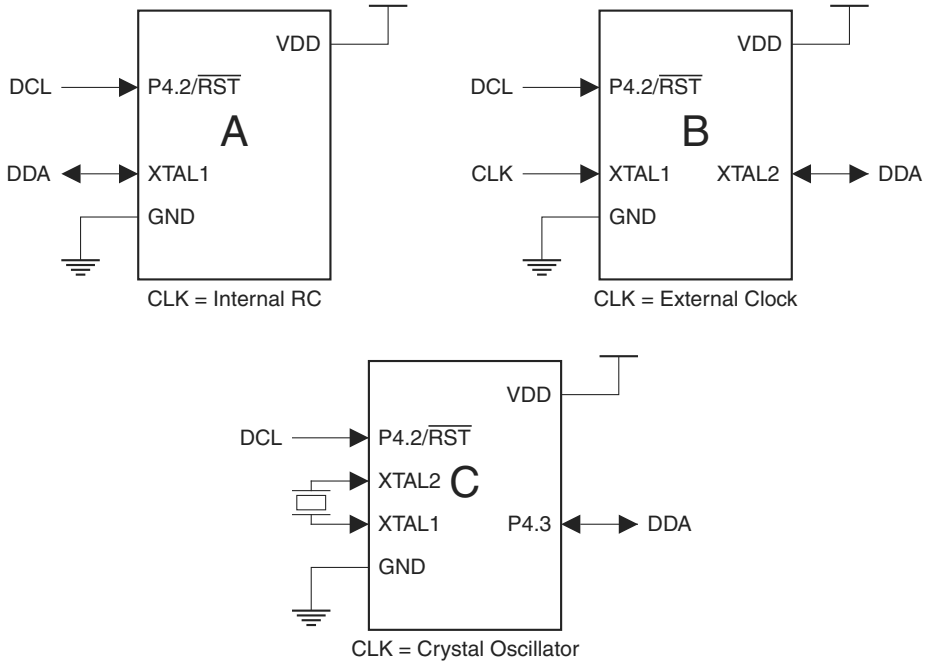
88h	Previously addressed with own SLA+W; data has been received; NOT ACK has been returned	Read data byte	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		Read data byte	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”
		Read data byte	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		Read data byte	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”; a START condition will be transmitted when the bus becomes free
90h	Previously addressed with general call; data has been received; ACK has been returned	Read data byte	X	0	1	0	Data byte will be received and NOT ACK will be returned
		Read data byte	X	0	1	1	Data byte will be received and ACK will be returned
98h	Previously addressed with general call; data has been received; NOT ACK has been returned	Read data byte	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		Read data byte	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”
		Read data byte	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		Read data byte	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”; a START condition will be transmitted when the bus becomes free
A0h	A STOP condition or repeated START condition has been received while still addressed as slave	No Action	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		No Action	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”
		No Action	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		No Action	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”; a START condition will be transmitted when the bus becomes free

Figure 18-13. Format and States in Slave Receiver Mode



- P4.2/$\overline{\text{RST}}$ cannot be connected directly to V_{DD} and any external capacitors connected to $\overline{\text{RST}}$ must be removed.
- All external reset sources must be removed.
- If P4.3 needs to be debugged in systems using the crystal oscillator, the external clock option should be selected. The quartz crystal and any capacitors on XTAL1 or XTAL2 must be removed and an external clock signal must be driven on XTAL1. Some emulator systems may provide a user-configurable clock for this purpose.

Figure 24-1. AT89LP3240/6440 On-Chip Debug Connections



24.2 Software Breakpoints

The AT89LP3240/6440 microcontroller includes a BREAK instruction for implementing program memory breakpoints in software. A software breakpoint can be inserted manually by placing the BREAK instruction in the program code. Some emulator systems may allow for automatic insertion/deletion of software breakpoints. The Flash memory must be re-programmed each time a software breakpoint is changed. Frequent insertions/deletions of software breakpoints will reduce the endurance of the nonvolatile memory. Devices used for debugging purposes should not be shipped to end customers. The BREAK instruction is treated as a two-cycle NOP when OCD is disabled.

24.3 Limitations of On-Chip Debug

The AT89LP3240/6440 is a fully-featured microcontroller that multiplexes several functions on its limited I/O pins. Some device functionality must be sacrificed to provide resources for On-Chip Debugging. The On-Chip Debug System has the following limitations:

- The Debug Clock pin (DCL) is physically located on that same pin as Port Pin P4.2 and the External Reset ($\overline{\text{RST}}$). Therefore, neither P4.2 nor an external reset source may be emulated when OCD is enabled.

- When using the Internal RC Oscillator during debug, DDA is located on the XTAL1/P4.0 pin. The P4.0 I/O function cannot be emulated in this mode.
- When using the External Clock during debug, DDA is located on the XTAL2/P4.1 pin and the system clock drives XTAL1/P4.0. The P4.1 I/O and CLKOUT functions cannot be emulated in this mode.
- When using the Crystal Oscillator during debug, DDA is located on the P4.3 pin and the crystal connects to XTAL1/P4.0 and XTAL2/P4.1. The P4.3 I/O function cannot be emulated in this mode.

25. Programming the Flash Memory

The Atmel AT89LP3240/6440 microcontroller features 64K bytes of on-chip In-System Programmable Flash program memory and 8K bytes of nonvolatile Flash data memory. In-System Programming allows programming and reprogramming of the microcontroller positioned inside the end system. Using a simple 4-wire SPI interface, the programmer communicates serially with the AT89LP3240/6440 microcontroller, reprogramming all nonvolatile memories on the chip. In-System Programming eliminates the need for physical removal of the chips from the system. This will save time and money, both during development in the lab, and when updating the software or parameters in the field. The programming interface of the AT89LP3240/6440 includes the following features:

- Four-wire serial SPI Programming Interface or 11-pin Parallel Interface
- Active-low Reset Entry into Programming
- Slave Select allows multiple devices on same interface
- User Signature Array
- Flexible Page Programming
- Row Erase Capability
- Page Write with Auto-Erase Commands
- Programming Status Register

For more detailed information on In-System Programming, refer to the Application Note entitled “AT89LP In-System Programming Specification”.

25.1 Physical Interface

The AT89LP3240/6440 provides a standard programming command set with two physical interfaces: a bit-serial and a byte-parallel interface. Normal Flash programming utilizes the Serial Peripheral Interface (SPI) pins of an AT89LP3240/6440 microcontroller. The SPI is a full-duplex synchronous serial interface consisting of four wires: Serial Clock (SCK), Master-In/Slave-out (MISO), Master-out/Slave-in (MOSI), and an active-low chip select and frame signal ($\overline{SS}$). When programming an AT89LP3240/6440 device, the programmer always operates as the SPI master, and the target system always operates as the SPI slave. To enter or remain in Programming mode the device’s reset line ($\overline{RST}$) must be held active (low). With the addition of VDD and GND, an AT89LP3240/6440 microcontroller can be programmed with a minimum of seven connections as shown in Figure 25-1.

In addition to being a chip select, the $\overline{SS}$ pin also is used to frame a command packet. $\overline{SS}$ must go low before the start of a command and must return high to complete the command. **$\overline{SS}$ must NOT be tied to ground as this will prevent the interface from recognizing mutiple commands**. $\overline{SS}$ should be connected to the programming master for correct operation.

26.6 Reset Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 3.6V, unless otherwise noted.

Table 26-3. Reset Characteristics

Symbol	Parameter	Condition	Min	Max	Units
$R_{\overline{RST}}$	Reset Pull-up Resistor		50	150	kΩ
V_{POR}	Power-On Reset Threshold		1.3	1.6	V
V_{BOD}	Brown-Out Detector Threshold		1.8	2.0	V
V_{BH}	Brown-Out Detector Hysteresis		200	300	mV
t_{POR}	Power-On Reset Delay		135	150	µs
t_{WDTRST}	Watchdog Reset Pulse Width		$16t_{CLCL}$		ns

26.7 External Data Memory Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 3.6V, unless otherwise noted. Under operating conditions, load capacitance for Port 0 and ALE = 100 pF; load capacitance for all other outputs = 80 pF. Parameters refer to Figure 26-15 and Figure 26-16.

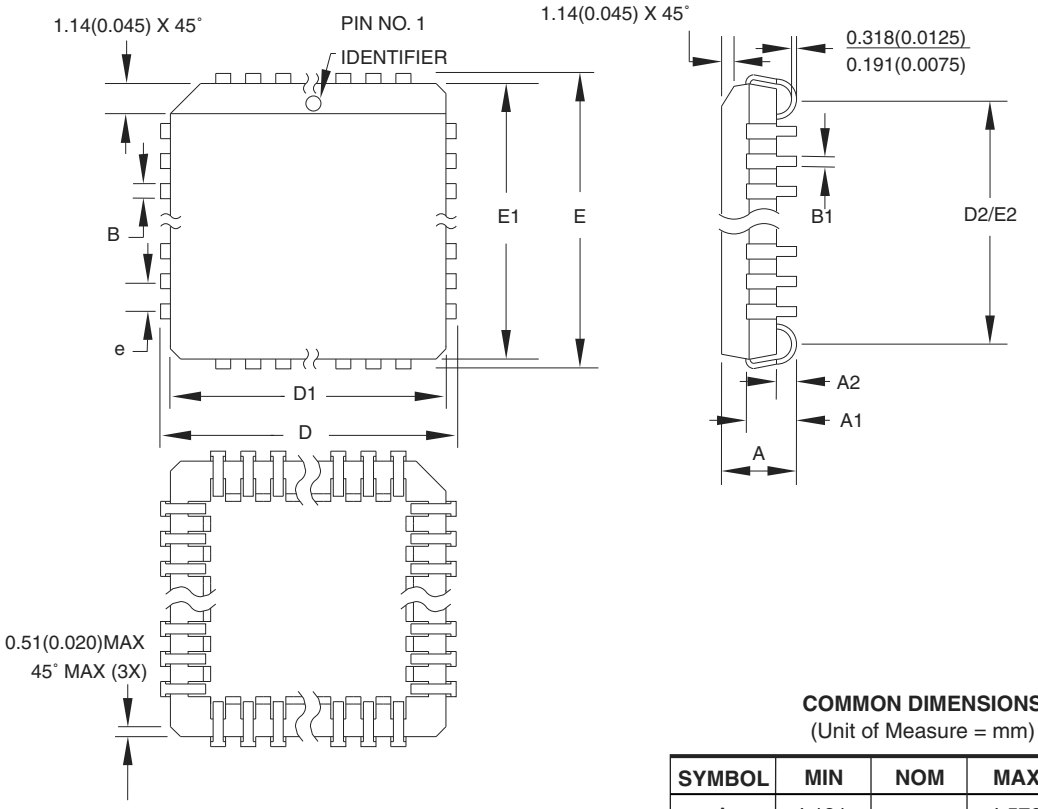
Table 26-4. External Data Memory Characteristics

		Variable Oscillator		
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width(3)	t_{CLCL} - d		ns
t_{AVLL}	Address Valid to ALE Low	$0.5t_{CLCL}$ - d(1)		ns
t_{LLAX}	Address Hold after ALE Low	$0.5t_{CLCL}$ - d(2)		ns
t_{RLRH}	$\overline{RD}$ Pulse Width(4)	t_{CLCL} - d		ns
t_{WLWH}	$\overline{WR}$ Pulse Width(4)	t_{CLCL} - d		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		t_{CLCL} - d	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		t_{CLCL} - d	ns
t_{LLDV}	ALE Low to Valid Data In		$2t_{CLCL}$ - d	ns
t_{AVDV}	Address to Valid Data In		$2.5t_{CLCL}$ - d(1)	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{CLCL} - d	t_{CLCL} + d	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$1.5t_{CLCL}$ - d(1)		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	$0.5t_{CLCL}$ - d(1)		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$1.5t_{CLCL}$ - d(1)		ns
t_{WHQX}	Data Hold after $\overline{WR}$	$0.5t_{CLCL}$ - d(2)		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		$-0.5t_{CLCL}$ + d(1)	ns
t_{WHAX}	Address Hold after $\overline{RD}$ or $\overline{WR}$ High	$0.5t_{CLCL}$ - d(2)		ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High(5)	t_{CLCL} - d	t_{CLCL} + d	ns

Notes: 1. This assumes 50% clock duty cycle. The half period depends on the clock high value t_{CHCX} (high duty cycle).

2. This assumes 50% clock duty cycle. The half period depends on the clock low value t_{CLCX} (low duty cycle).

28.3 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
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